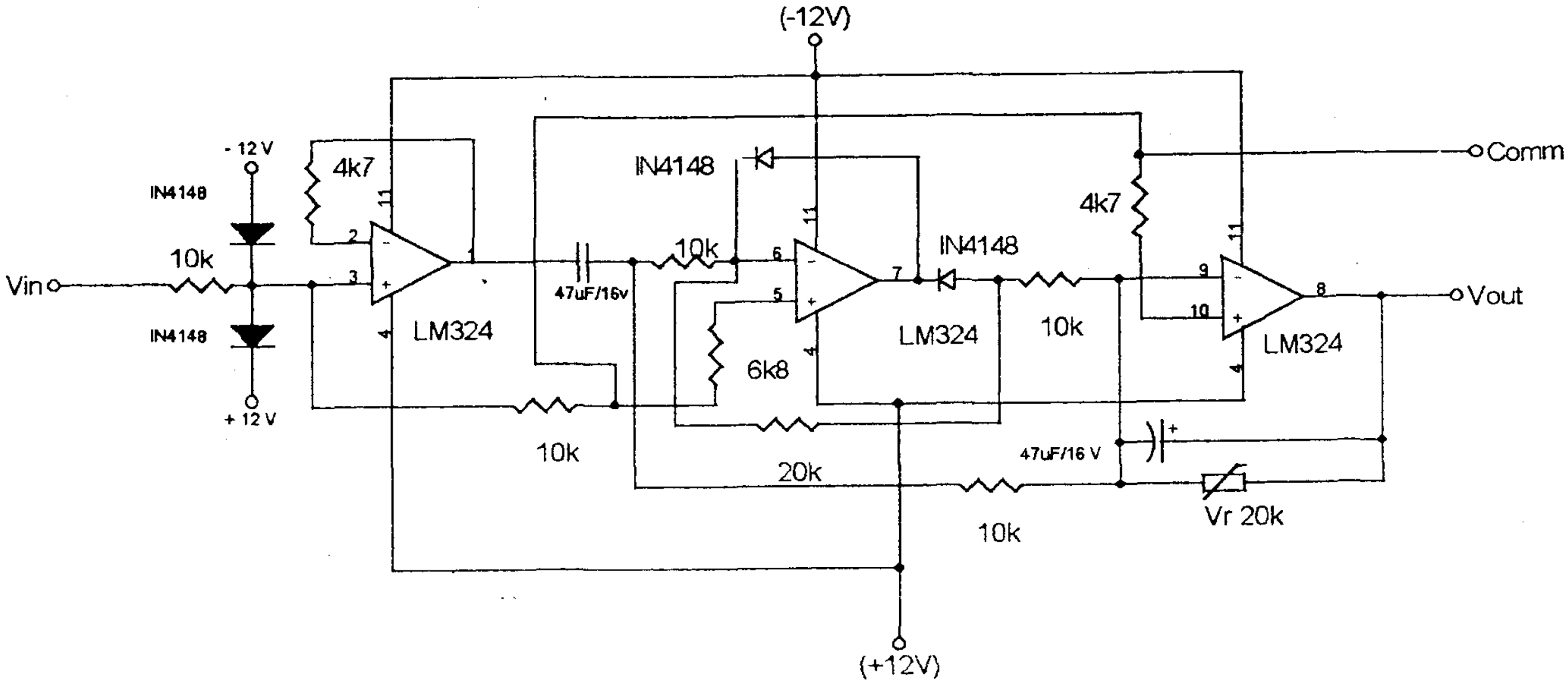
LAMPIRAN



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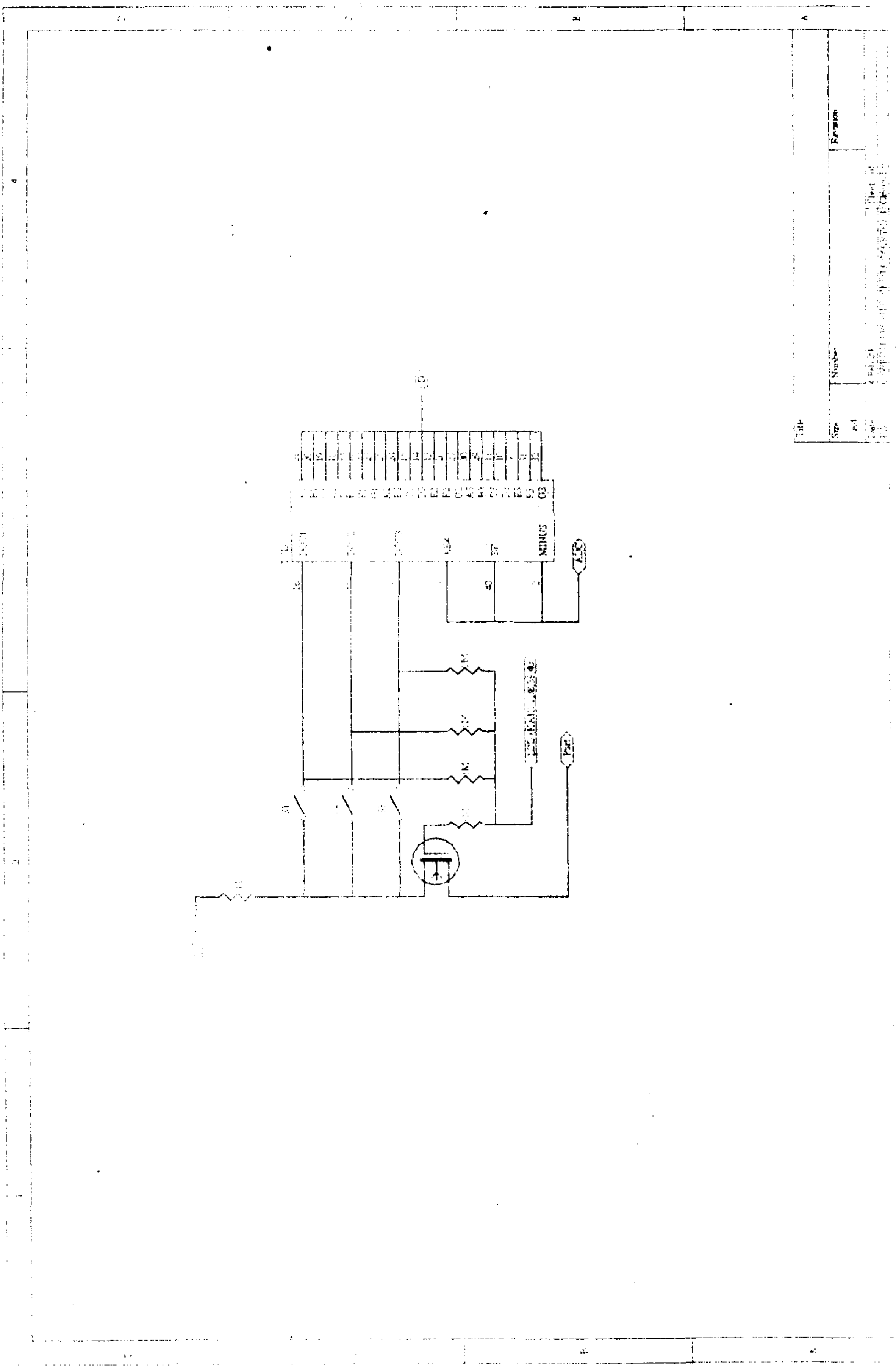
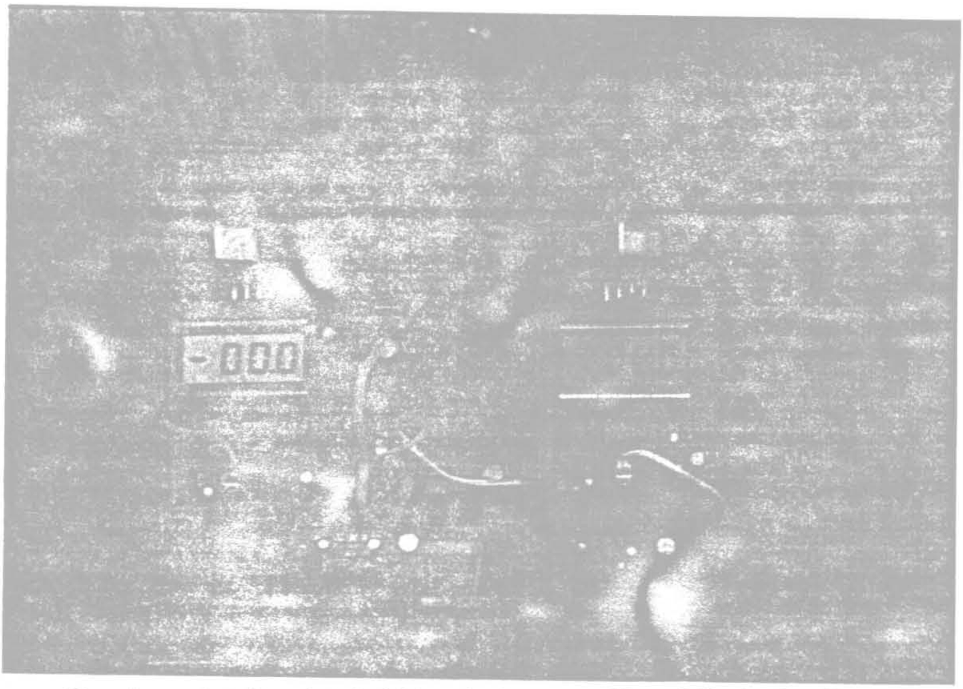
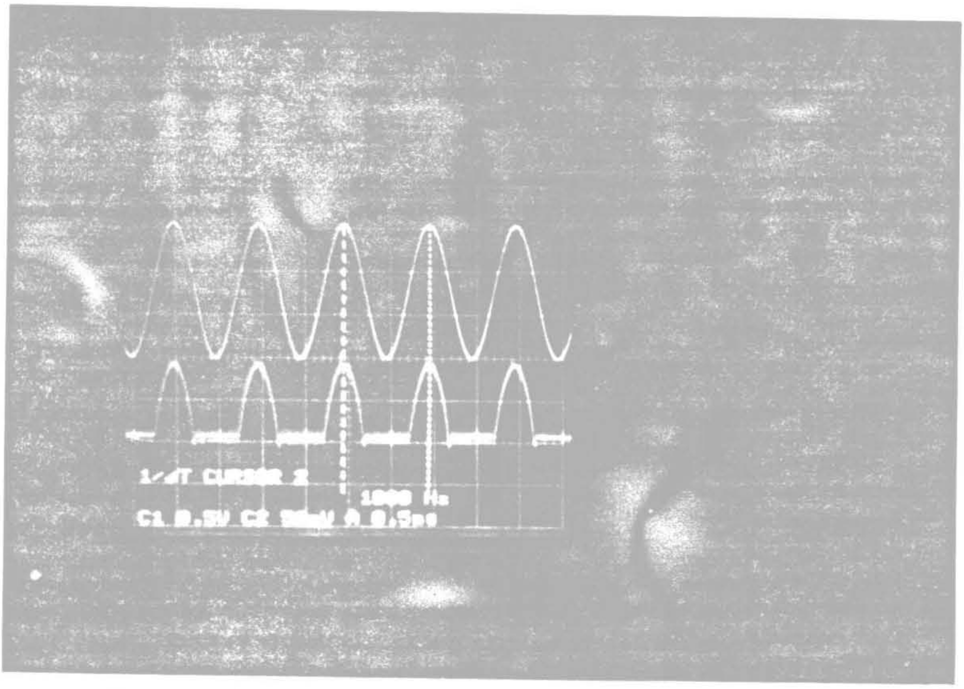


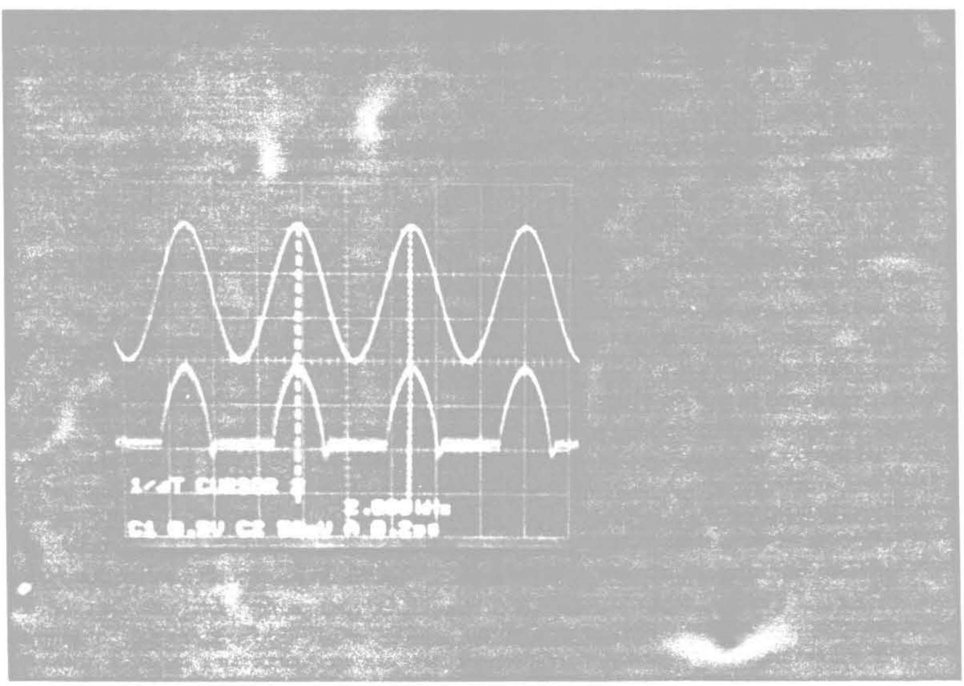


Gambar alat Pendeteksi Keseimbangan Kanal Pada Audio

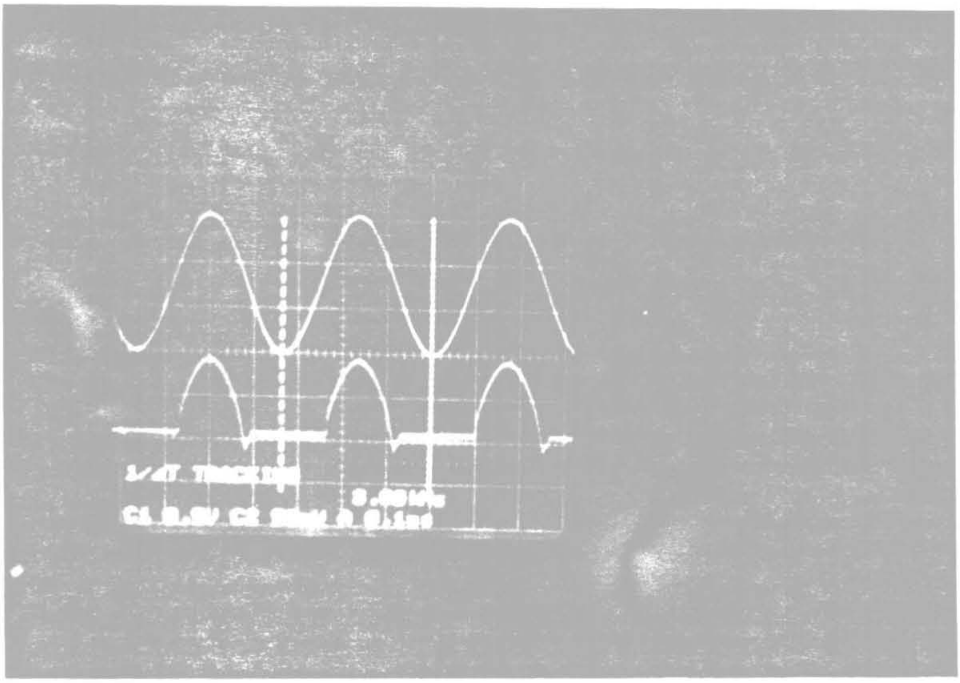
Gambar Alat Pendeteksi Keseimbangan Kanal pada Audio
dengan Indikator LED



Gambar sinyal input /output dengan frekuensi 1KHz



Gambar sinyal input /output dengan frekuensi 2KHz



Gambar sinyal input /output dengan frekuensi 3KHz .

MAXIM

3½ Digit A/D Converter

ICL7106/7107

General Description

The Maxim ICL7106 and ICL7107 are monolithic analog to digital converters. They have very high input impedances and require no external display drive circuitry. On-board active components include polarity and digit drivers, segment decoders, voltage reference and a clock circuit. The ICL7106 will directly drive a non-multiplexed liquid crystal display (LCD) whereas the ICL7107 will directly drive a common anode light emitting diode (LED) display.

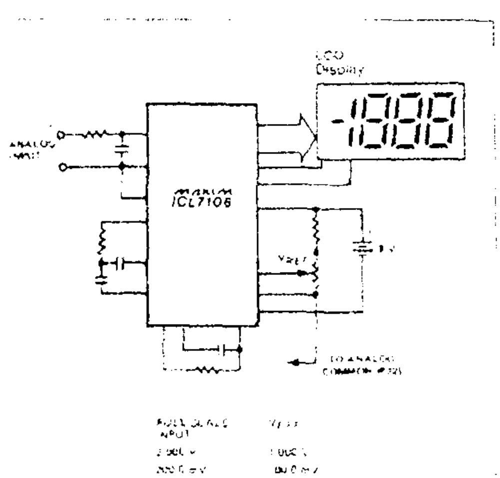
Versatility and accuracy are inherent features of these converters. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. The true differential input and reference are particularly useful when making ratiometric measurements (ohms or bridge transducers). Maxim has added a zero-integrator phase to the ICL7106 and ICL7107, eliminating overrange hangover and hysteresis effects. Finally, these devices offer high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1µV/°C.

Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

Typical Operating Circuit



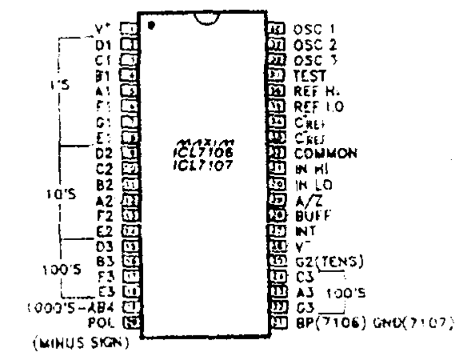
Features

- ♦ Improved 2nd Source! (See 3rd page for "Maxim Advantage™")
- ♦ Guaranteed first reading recovery from overrange
- ♦ On board Display Drive Capability—no external circuitry required
  LCD-ICL7106
  LED-ICL7107
- ♦ High Impedance CMOS Differential Inputs
- ♦ Low Noise (< 15µV p-p) without hysteresis or overrange hangover
- ♦ Clock and Reference On-Chip
- ♦ True Differential Reference and Input
- ♦ True Polarity Indication for Precision Null Applications
- ♦ Monolithic CMOS design

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7106CPL	0°C to + 70°C	40 Lead Plastic DIP
ICL7106CJL	0°C to + 70°C	40 Lead CERDIP
ICL7106CQH	0°C to + 70°C	44 Lead Plastic Chip Carrier
ICL7106C/D	0°C to + 70°C	Dice
ICL7107CPL	0°C to + 70°C	40 Lead Plastic DIP
ICL7107CJL	0°C to + 70°C	40 Lead CERDIP
ICL7107CQH	0°C to + 70°C	44 Lead Plastic Chip Carrier
ICL7107C/D	0°C to + 70°C	Dice

Pin Configuration



See last page for Plastic Chip Carrier Pin Configuration

*The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

ICL7106/7107

3½ Digit A/D Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- ICL7106, V^+ to V^- ... 15V
- ICL7107, V^+ to GND ... +6V
- ICL7107, V^- to GND ... −9V

Analog Input Voltage (either input)(Note 1) ... V^+ to V^-
Reference Input Voltage (either input) ... V^+ to V^-
Clock Input
- ICL7106 ... TEST to V^+
- ICL7107 ... GND to V^+

Power Dissipation (Note 2)
- Plastic Package ... 1000mW

Operating Temperature ... 0°C to +70°C
Storage Temperature ... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ... +300°C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100µA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF} V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ ≈ 200.0mV	−1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		50		µV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		µV
Input Leakage Current	V_{IN} = 0		1	10	pA
Zero Reading Drift	V_{IN} = 0 0° < T_A < 70°C		0.2	1	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° < T_A < 70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7107)	V_{IN} = 0		0.8	1.8	mA
V^- supply current 7107 only			0.6	1.8	mA
Analog Common Voltage (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply		80		ppm/°C
7106 ONLY Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
7107 ONLY Segment Sinking Current (Except Pin 19)	V^+ = 5.0V Segment voltage = 3V	5	8.0		mA
(Pin 19 only)		10	16		mA

Note 3: Unless otherwise noted, specifications apply to both the 7106 and 7107 at T_A = 25°C, f_{CLOCK} = 48kHz. 7106 is tested in the circuit of Figure 1. 7107 is tested in the circuit of Figure 2.

Note 4: Refer to "Differential Input" discussion.

Note 5: Backplane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

MAXIM

MAXIM

3½ Digit A/D Converter

ICL7106/7107

- Guaranteed Overload Recovery Time
- Significantly Improved ESD Protection (Note 7)
- Low Noise
- Key Parameters Guaranteed over Temperature
- Negligible Hysteresis
- Maxim Quality and Reliability
- Increased Maximum Rating for Input Current (Note 8)

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page

ELECTRICAL CHARACTERISTICS: Specifications below satisfy or exceed all "tested" parameters on adjacent page.
(V = 9V, T_A = 25°C, f_{CLOCK} = 48kHz (test circuit - Figure 1) unless noted)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV T_A = 25°C (Note 6) **0° ≤ T_A ≤ 70°C (Note 10)**	000.0 **−000.0**	±000.0 **±000.0**	+000.0 **+000.0**	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV T_A = 25°C (Note 6) **0° ≤ T_A ≤ 70°C (Note 10)**	999 **998**	999/1000 **999/1000**	1000 **1001**	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	−V_{IN} = +V_{IN} ≈ 200.0mV T_A = 25°C (Note 6) 0° ≤ T_A ≤ 70°C (Note 10)	−1	±.2 ±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Input Leakage Current	V_{IN} = 0 T_A = 25°C (Note 6) **0° ≤ T_A ≤ 70°C**		1 **20**	10 **200**	pA
Zero Reading Drift	V_{IN} = 0 0° ≤ T_A ≤ 70°C (Note 6)		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° ≤ T_A ≤ 70°C (Ext. Ref. 0ppm/°C) (Note 6)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7107)	V_{IN} = 0 T_A = 25°C **0° ≤ T_A ≤ 70°C**		0.6	1.8 **2**	mA
V^- Supply Current (7107 only)			0.6	1.8	mA
Analog Common Voltage (with respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	25kΩ between Common & Pos. Supply		75		ppm/°C
7106 Only (Note 5) Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V
7107 Only—Segment Sinking Current (Except Pin 19) (Pin 19 only)	V^+ = 5.0V Segment Voltage = 3V	5 10	8.0 16		mA mA
7106 Only—Test Pin Voltage	**With Respect to V^+**	**4**	**5**	**6**	**V**
Overload Recovery Time (Note 9)	**V_{IN} changing from ±10V to 0V**		**0**	**1**	**Measurement Cycles**

Note 6: Test condition is V_{IN} applied between pin IN-HI and IN-LO through a 1MΩ series resistor as shown in Figures 1 and 2.

Note 7: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil Std 883, Method 3015.1)

Note 8: Input voltages may exceed the supply voltage provided the input current is limited to ±1mA (This revises Note 1 on adjacent page).

Note 9: Number of measurement cycles for display to give accurate reading.

Note 10: 1MΩ resistor is removed in Figures 1 and 2.

3½ Digit A/D Converter

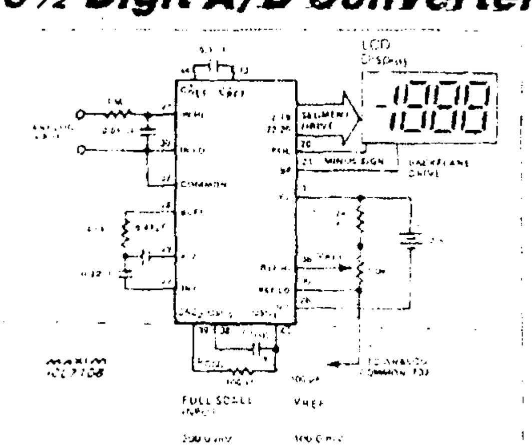


Figure 1. Maxim ICL7106 Typical Operating Circuit

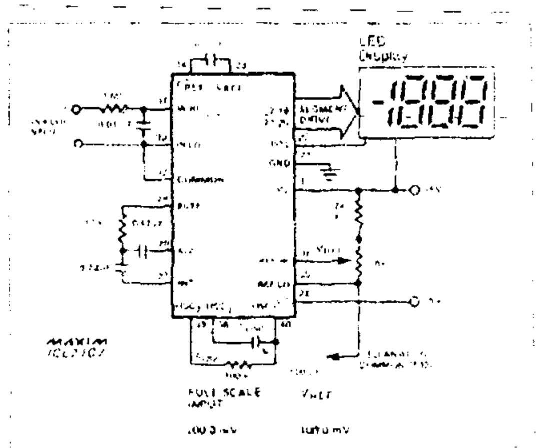


Figure 2. Maxim ICL7107 Typical Operating Circuit

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the ICL7136. Each measurement cycle is divided into four phases:

1. Auto-Zero (A-Z)
2. Signal Integrate (INT)
3. Reference De-Integrate (DI)
4. Zero Integrator (ZI)

Auto-Zero Phase

Three events occur during auto-zero. The inputs, IN-HI and IN-LO, are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. And lastly, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the comparator, buffer amplifier and integrator. The inherent noise of the system determines the A-Z accuracy.

Signal Integrate Phase

The internal input high (IN-HI) and input low (IN-LO) are connected to the external pins, the internal short is removed and the auto-zero loop is opened. The converter then integrates the differential voltage between IN-HI and IN-LO for a fixed time. This differential voltage can be within a wide common-mode range (within one volt of either supply). If, however, the input signal has no return with respect to the converter power supply, IN-LO can be tied to analog common to establish the correct common-mode voltage. The polarity of the integrated signal is determined at the end of this phase.

Reference De-Integrate

IN-HI is connected across the previously charged reference capacitor and IN-LO is internally connected to analog common. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The input signal determines the time required for the output to return to zero. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Zero Integrator Phase

Input low is shorted to analog COMMON and the reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to input high, causing the integrator output to return to zero. This phase normally lasts between 11 and 140 clock pulses but is extended to 740 clock pulses after a "heavy" overrange conversion.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a rollover voltage. This is caused by the reference capacitor losing or gaining charge to stray capacitance on its nodes. The reference capacitor can gain charge (increase voltage) if there is a large common-mode voltage. This happens during de-integration of a positive signal. In contrast, the reference capacitor will lose charge (decrease voltage) when de-integrating a negative input signal. Rollover error is caused by this difference in reference for positive or negative input voltages. This error can be held to less than half a count for the worst-case condition by selecting a reference capacitor that is large enough in comparison to the stray capacitance. (See component value selection.)

Differential Input

Differential voltages anywhere within the common-mode range of the input amplifier can be accepted by the input (specifically from 1V below the positive supply to 1.5V above the negative supply). The system has a CMRR of 86dB (typ) in this range. Care must be exercised, however, to ensure that the integrator output does not saturate, since the integrator follows the common-mode voltage. A large positive common-mode voltage with a near full-scale negative differential input voltage is a worst-case condition. When most of the integrator output swing has been used up by the positive common-mode voltage, the negative input signal drives the integrator more positive. The integrator swing can be reduced to less than the recommended 2V full-scale swing with no loss of accuracy in these critical

3½ Digit A/D Converter

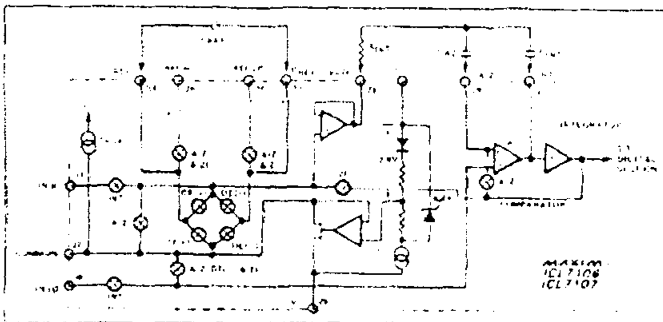


Figure 3. Analog Section of ICL7106/ICL7107

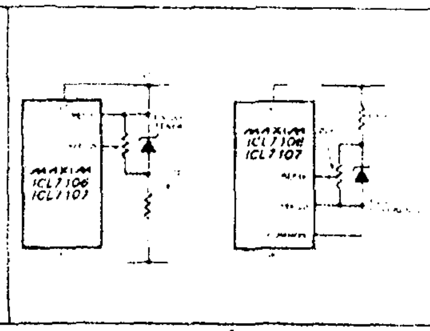


Figure 4. Using an External Reference

applications. The integrator output can swing within 0.3V of either supply without loss of linearity.

Analog Common

The primary purpose of this pin is to set the common-mode voltage for battery operation. This is useful when using the ICL7106, or for any system where the input signals are floating with respect to the power supply. A voltage of approximately 2.8V less than the positive supply is set by this pin. The analog common has some of the attributes of a reference voltage. If the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low output impedance (approximately 15Ω), a temperature coefficient of typically 80ppm/°C, and a low voltage coefficient (.001%).

The internal heating of the ICL7107 by the LED display drivers degrades the stability of Analog Common. The power dissipated by the LED display drivers changes with the displayed count, thereby changing the temperature of the die, which in turn results in a small change in the Analog Common voltage. This combination of variable power dissipation, thermal resistance, and temperature coefficient causes a 25–80µV increase in noise near full scale. Another effect of LED display driver power dissipation can be seen at the transition between a full scale reading and an overload condition. Overload is a low power dissipation condition since the three least significant digits are blanked in overload. On the other hand, a near full scale reading such as 1999 has many segments turned on and is a high power dissipation condition. The difference in power dissipation between overload and full scale may cause a ICL7107 with a negative temperature coefficient reference to cycle between overload and a near full scale display as the die alternately heats and cools. An ICL7107 with a positive TC reference will exhibit hysteresis under these conditions: once put into overload by a voltage just barely more than full scale, the voltage must be reduced by several counts before the ICL7107 will come out of overload.

None of the above problems are encountered when using an external reference. The ICL7106, with its low power dissipation, has none of these problems with either an external reference or when using Analog Common as a reference.

During auto-zero and reference integrate the internal input low is connected to Analog Common. If IN-LO is different from analog-common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. In some applications, however, IN-LO will be set at a fixed known voltage (e.g., power supply common). Whenever possible analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If convenient, REF-LO should be connected to analog common. This will remove the common-mode voltage from the reference system.

Analog Common is internally tied to an N-channel FET that can sink 30mA or more of current. This will hold the Analog Common voltage 2.8V below the positive supply (when a source is trying to pull the common line positive). There is only 10µA of source current, however, so COMMON may easily be tied to a more negative voltage, thus over-riding the internal reference.

Test

Two functions are performed by the test pin. The first is using this pin as the negative supply for externally generated segment drivers or any other annunciators the user may want to include on the LCD. This pin is coupled to the internally generated digital supply through a 500Ω resistor. This application is illustrated in Figures 5 & 6.

A lamp test is the second function. All segments will be turned on and the display should read −1888, when TEST is pulled high (V+).

Caution: In the lamp test mode, the segments have a constant dc voltage (no square wave). This can burn the LCD if left in this mode for several minutes.

3½ Digit A/D Converter

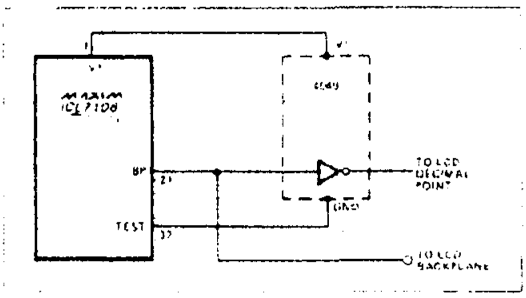


Figure 5A. Fixed Decimal Point Drivers

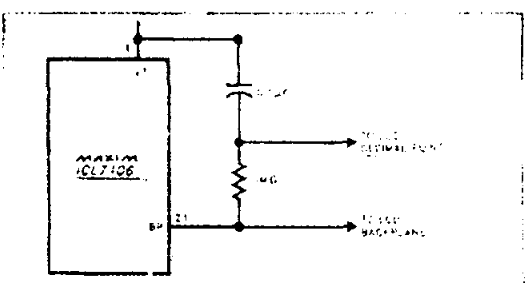


Figure 5B. Fixed Decimal Point Drivers

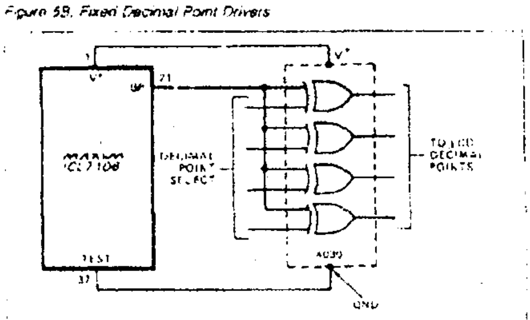


Figure 6. Exclusive 'OR' Gate for Decimal Point Drive

Digital Section

The digital section for the ICL7106 and ICL7107 is illustrated in Figures 8 and 9. In Figure 8, an internal digital ground is generated from a 6V zener diode and a large P-channel source follower. This supply is made stiff to absorb the large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is calculated by dividing the clock frequency by 800. For example, with a clock frequency of 48kHz (3 readings per second), the backplane will be a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude. Note that these are out-of-phase when the segment is ON and in-phase when OFF. Negligible dc voltage exists across the segments in either case.

The ICL7107 is identical to the ICL7106 except that the backplane and drivers have been replaced by N-channel segment drivers. The ICL7107 is designed to drive common anode LED's with a typical segment current of 8mA. Pin 19 (thousands digit output) sinks current from two LED segments, and has a 16mA drive capability.

The polarity indication is "on" for negative analog inputs, for both the ICL7106 and ICL7107. If desired IN-HI and IN-LO can be reversed giving a "on" for positive analog inputs.

System Timing

The clocking circuitry for the ICL7106 and ICL7107 is illustrated in Figure 7. Three approaches can be used:

1. A crystal between pins 39 and 40.
2. An external oscillator connected to pin 40
3. An RC oscillator using all three pins.

The decade counters are driven by the clock frequency divided by four. This frequency is then further divided to form the four convert-cycle phases, namely: signal integrate (1000 counts), reference de-integrate (0 to 2000 counts), auto-zero (260 to 2989 counts) and zero integrator (11 to 740).

The signal integration should be a multiple of 60Hz to achieve a maximum rejection of 60Hz pickup. Oscillator frequencies of 30kHz, 40kHz, 48kHz, 60kHz, 80kHz, 120kHz, 240kHz, etc., should be selected. Similiarly, for 50Hz rejection, oscillator frequencies of 200kHz, 100kHz, 66⅔kHz, 50kHz, 40kHz, etc., are appropriate. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

Auto-zero receives the unused portion of reference deintegrate for signals less than full-scale. A complete measurement cycle is 4,000 counts (16,000 clock pulses), independent of input voltage. As an example, an oscillator frequency of 48kHz would be used to obtain three readings per second.

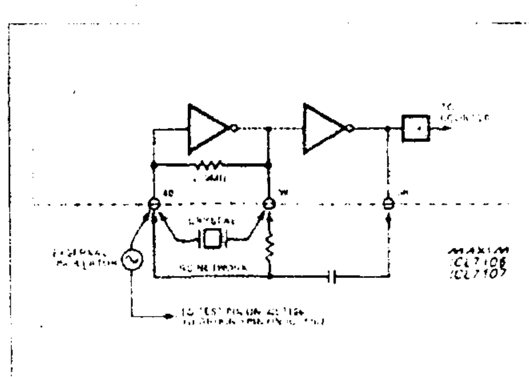


Figure 7. Clock Circuits

3½ Digit A/D Converter

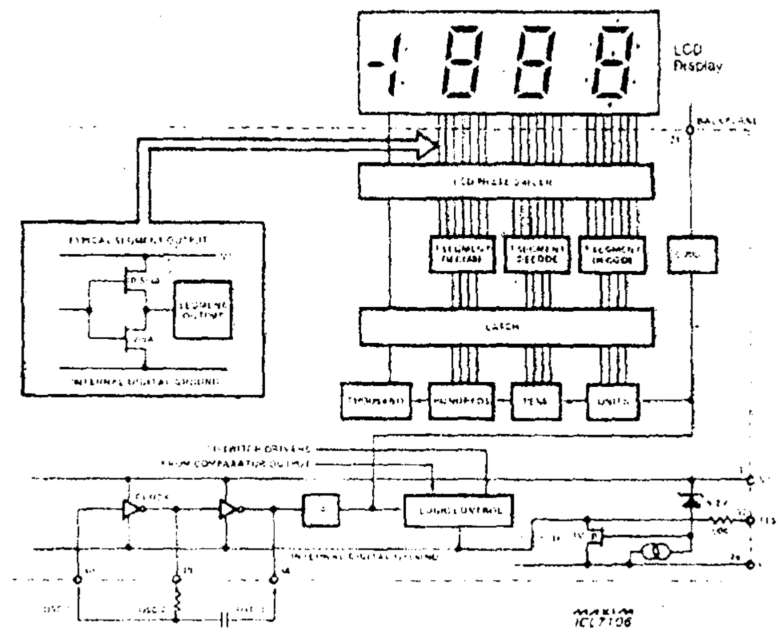


Figure 8. ICL7106 Digital Section

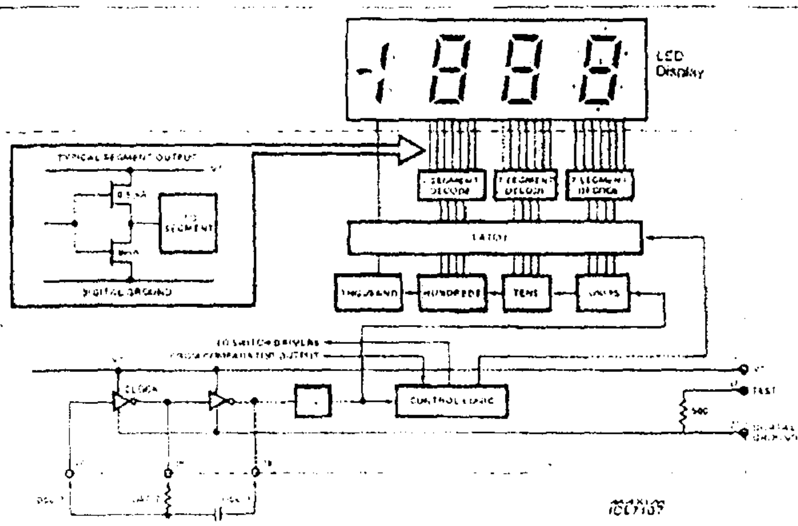


Figure 9. ICL7107 Digital Section

3½ Digit A/D Converter

ICL7106/7107

Component Value Selection

Auto-Zero Capacitor

The noise of the system is influenced by the auto-zero capacitor. For the 2V scale, a 0.047μF capacitor is adequate. A capacitor size of 0.47μF is recommended for 200mV full scale where low noise operation is very important. Due to the ZI phase of Maxim's ICL7106/7, noise can be reduced by using a larger auto-zero capacitor without causing hysteresis or overrange hangover problems seen in other manufacturers' ICL7106/7 which do not have the ZI phase.

Reference Capacitor

For most applications, a 0.1μF capacitor is acceptable. However, a large value is needed to prevent rollover error where a large common-mode voltage exists (i.e., the REF-LO pin is not at analog common) and a 200mV scale is used. Generally, the roll over error will be held half a count by using a 1.0μF capacitor.

Integrating Capacitor

To ensure that the integrator will not saturate (at approximately 0.3V from either supply), an appropriate integrating capacitor must be selected. A nominal ±2V full-scale integrator swing is acceptable for the ICL7106 or ICL7107 when the analog common is used as a reference. A nominal ±3.5 to 4 volt swing is acceptable for the ICL7107 with a ±5V supply and analog common tied to supply ground. The nominal values for C_{INT} is 0.22μF for three readings per second. (48kHz clock). These values should be changed in inverse proportion to maintain the same output swing if different oscillator frequencies are used.

The integrating capacitor must have low dielectric absorption to minimize linearity errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

The integrator and the buffer amplifier both have a class A output stage with 100μA of quiescent current. 20μA of drive current can be supplied with negligible non-linearity. This resistor should be large enough to maintain the amplifiers in the linear region over the entire input voltage range. The resistor value, however, should be low enough that undue leakage requirements are not placed on the PC boards. For a 200mV scale, a 47KΩ resistor is recommended; (2V scale 470KΩ).

Oscillator Components

A 100KΩ resistor is recommended for all ranges of frequency. By using the equation f = 0.45/RC, the capacitor value can be calculated. For 48kHz clock, (3 readings/second), the oscillator capacitor plus stray capacitance should equal 100pF.

Reference Voltage

An analog input voltage of V_{IN} equal to 2 (V_{REF}) is required to generate full scale output of 2000 counts. Thus, for 2V and 200mV scales, V_{REF} should equal 1V and 100mV respectively. However, there will exist a scale factor other than unity between the input voltage and the digital reading in many applications where the A/D is connected to a transducer.

As an example, the designer may like to have a full scale reading in a weighing system when the voltage from the transducer is 0.682V. The designer should use the input voltage directly and select V_{REF} at 0.341V instead of dividing the input down to 200mV. Suitable values of the capacitor and integrating resistor would be 0.22μF and 120KΩ. This provides for a slightly quieter system and also avoids a divider network on the input. The ICL7107 can accept input signals up to ±3.5V with ±5V supplies. Another advantage of this system occurs when the digital reading of zero is desired for $V_{IN} \neq$ zero. Examples are temperature and weighing systems with variable tare. By connecting the voltage transducer between V_{IN} positive and common, and the variable (or fixed) offset voltage between common and V_{IN} negative, the offset reading can be conveniently generated.

ICL7107 Power Supplies

The ICL7107 is designed to operate from ±5V supplies. However, when a negative supply is not available it can be generated from a clock output with two diodes, two capacitors, and an inexpensive IC. Refer to Figure 10. Alternatively a −5V supply can be generated using Maxim's ICL7660 and two capacitors.

A negative supply is not required in selected applications. The conditions to use a single +5V supply are:

- An external reference is used.
- The signal is less than ±1.5V.
- The input signal can be referenced to the center of the common-mode range of the converter.

See Figure 18.

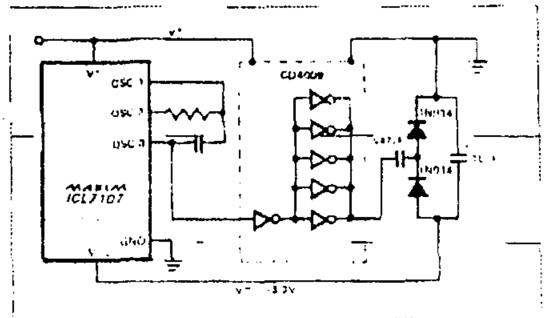


Figure 10. Generating Negative Supply from +5V

3½ Digit A/D Converter

Applications Information

Heat is generated within the ICL7107 IC package due to the sinking of LED display current. Fluctuating chip temperature can cause a display to change reading if the internal voltage reference is used. By reducing the power being dissipated such variations can be reduced. The ICL7107 power dissipation is reduced by reducing the LED common anode voltage. The curve tracer illustration showing the relationship between the output current and the output voltage for typical ICL7107 is seen in Figure 11. Note that the typical ICL7107 output is 3.2V (point A), since the typical LED has 1.8V across it (8mA drive current) and its common anode is connected to +5V. Maximum power dissipation is:

8.1mA × 3.2V × 24 segments = 622mW

Once the ICL7107 output voltage is above 2V, the LED current is essentially constant as output voltage increases. Point B illustrates that reducing the output voltage by 0.7V results in 7.7mA of LED current, (only 5% reduction). The maximum power dissipation is a reduction of 26% as calculated by:

7.7mA × 2.5V × 24 segments = 462mW

As illustrated in Figure 12, reduced power dissipation is easy to obtain. This can be accomplished by placing either a 5.1Ω resistor or a 1 amp diode in series with the display (but not in series with the ICL7107). Point C of Figure 18 illustrates that a resistor will reduce the ICL7107 output voltage when all 24 segments are "On". The output voltage will increase when segments are turned "Off". On the other hand, the diode will result in a relatively steady output voltage, around Point B. The resistor not only reduces the change in power dissipation as the display changes, but also limits the maximum power dissipation. This is due to the fact that as fewer segments are "On", each "On" output drops more voltage and current. The resistor circuit will change about 230mW when changing from the best case of six segments, a "111" display, to worst-case of a "1888" display. If the resistor is removed, the power dissipation change will be 470mW. The resistor, therefore, will reduce the effect of display dissipation on reference voltage drift by about 50%.

As more segments are turned off, the change in LED brightness caused by the resistor is almost unnoticeable. A diode may be used instead of the resistor if it is important to maintain a steady level of display brightness.

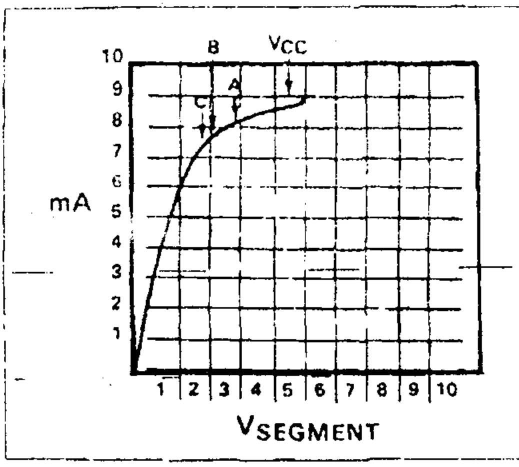


Figure 11. ICL7107 Output Current vs. Output Voltage

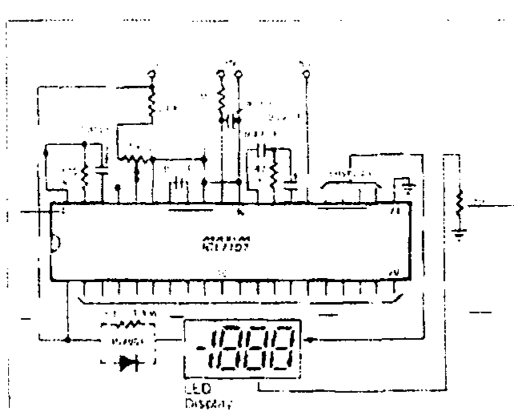


Figure 12. Diode or Resistor Limits Package Power Dissipation

3½ Digit A/D Converter

Typical Applications

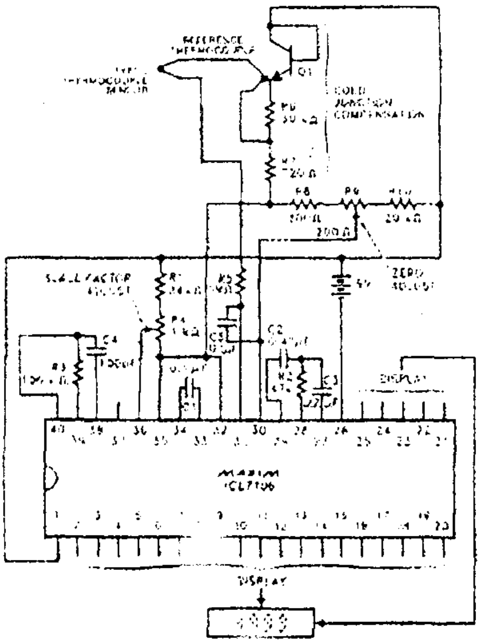


Figure 19. Thermocouple Thermometer. This circuit operates with approximately 50mV reference, so the 50.4μV/°C output of a Type J thermocouple results in 1 count/°C.

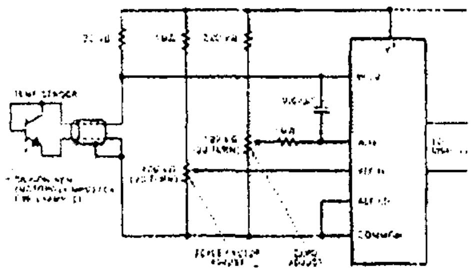
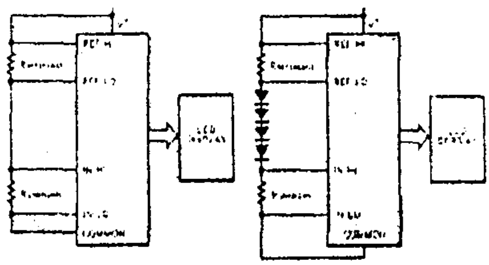


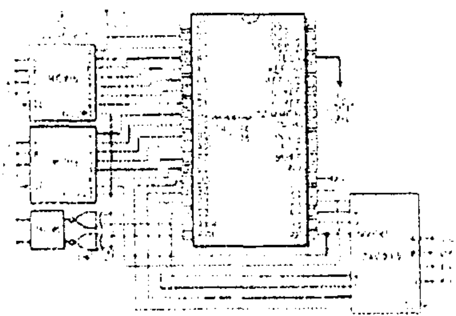
Figure 20. Digital Thermometer



ICL7106 system setup for 2V reference

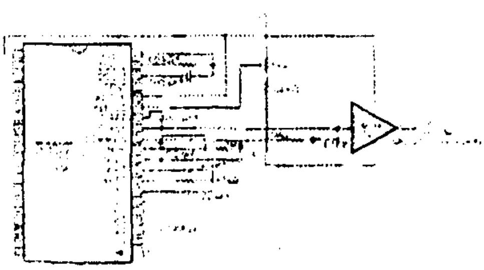
ICL7106 system setup for 200mV reference

Figure 22. Ratiometric Ohms Measurement



* For ICL7107, tie "INVERT" high, and omit EX-NOR gates.

Figure 21. BCD Output from 7-Segment Drivers



* ICL7106/7 only. See data sheet for values for other parts.

Figure 23. Simple End-of-Conversion Detector

3½ Digit A/D Converter

Typical Applications

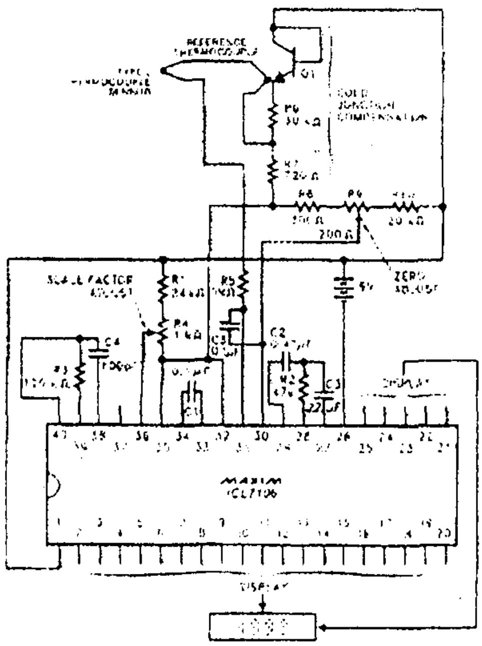


Figure 19. Thermocouple Thermometer. This circuit operates with approximately 50mV reference, so the 52.4µV/°C output of a Type J thermocouple results in 1 count/°C.

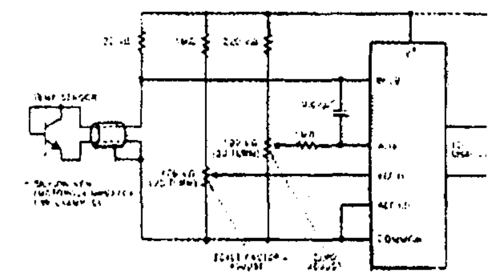
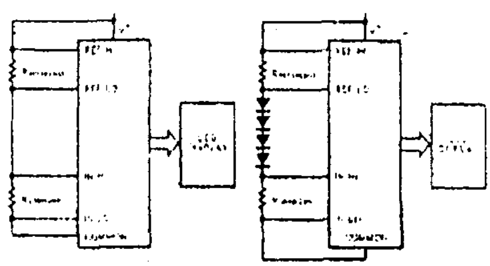


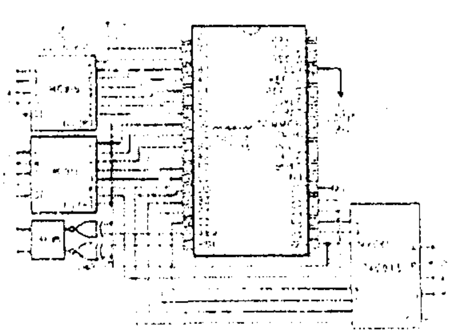
Figure 20. Digital Thermometer



ICL7106 system setup for 2V reference

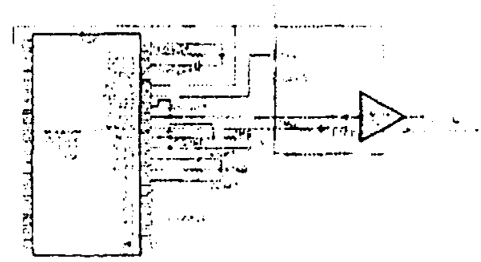
ICL7106 system setup for 200mV reference

Figure 22. Ratiometric Ohms Measurement



* For ICL7107, tie "INVERT" high, and omit EX-NOR gates.

Figure 21. BCD Output from 7-Segment Drivers



* ICL7106/7 only. See data sheet for values for other parts.

Figure 23. Simple End-of-Conversion Detector

3½ Digit A/D Converter

ICL7106/7107

Typical Applications

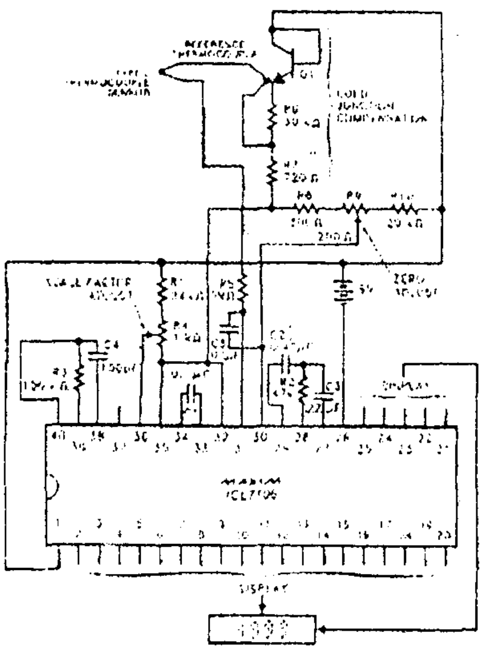


Figure 19. Thermocouple Thermometer. This circuit operates with approximately 50mV reference, so the 50.4μV/°C output of a Type J thermocouple results in 1 count/°C.

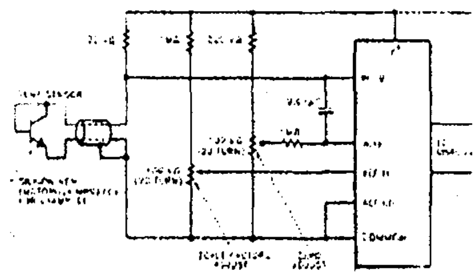
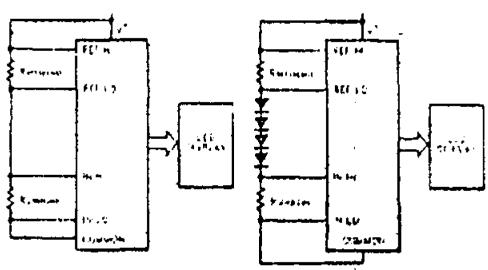


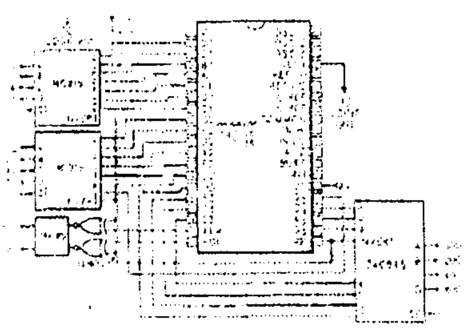
Figure 20. Digital Thermometer



ICL7106 system setup for 2V reference

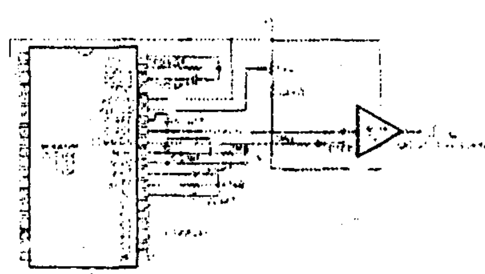
ICL7106 system setup for 200mV reference

Figure 22. Ratiometric Ohms Measurement



* For ICL7107, tie "INVERT" high, and omit EX-NOR gates.

Figure 21. BCD Output from 7-Segment Drivers



* ICL7106/7 only. See data sheet for values for other parts.

Figure 23. Simple End-of-Conversion Detector

3½ Digit A/D Converter

Typical Applications

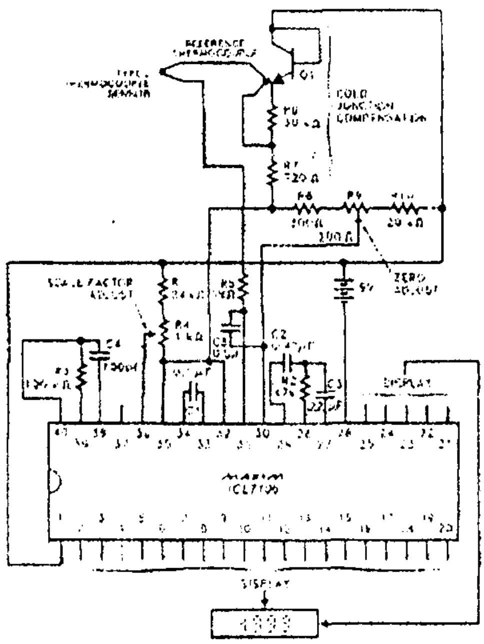


Figure 19. Thermocouple Thermometer. This circuit operates with approximately 50mV reference, so the 50.4μV/°C output of a Type J thermocouple results in 1 count/°C.

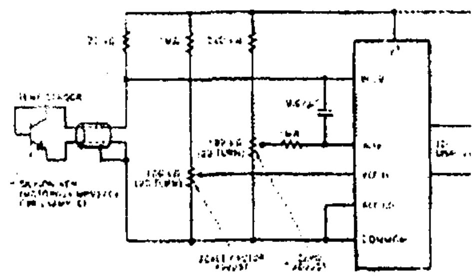
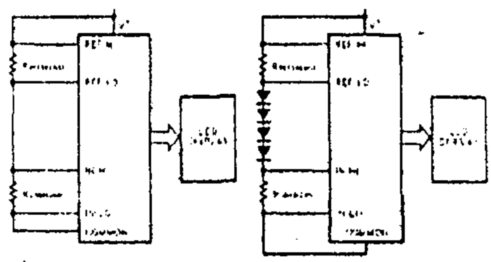


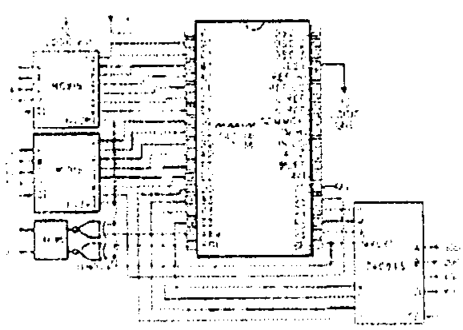
Figure 20. Digital Thermometer



ICL7106 system setup for 2V reference

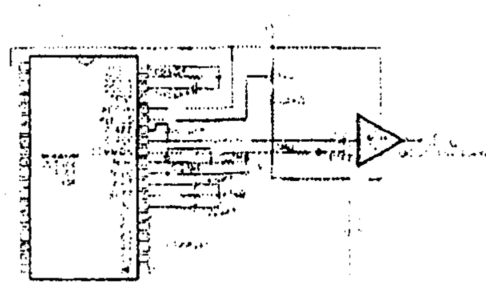
ICL7106 system setup for 200mV reference

Figure 22. Ratiometric Ohms Measurement



* For ICL7107, tie "INVERT" high, and omit EX-NOR gates.

Figure 21. BCD Output from 7-Segment Drivers



* ICL7106/7 only. See data sheet for values for other parts.

Figure 23. Simple End-of-Conversion Detector

3½ Digit A/D Converter

ICL7106/7107

Typical Applications

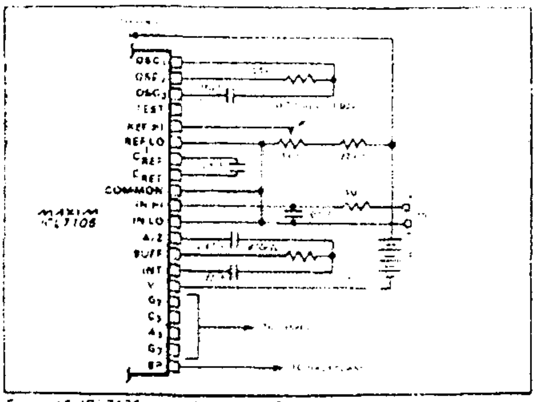


Figure 13. ICL7106 using the Internal Reference. 2V Full Scale, 3 Readings per Second

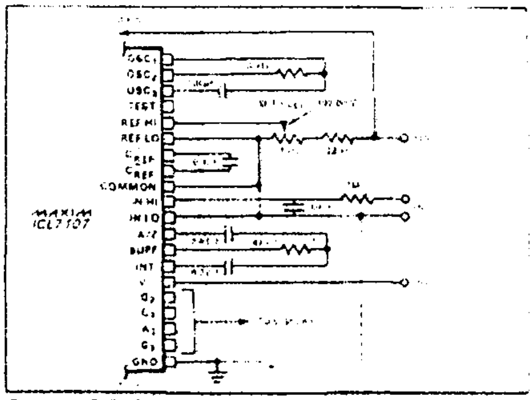


Figure 14. ICL7107 Internal Reference. 200mV Full Scale, 3 Readings per Second. V_{IN} Tied to GND for Single Ended Inputs. (See discussion under "Analog Common".)

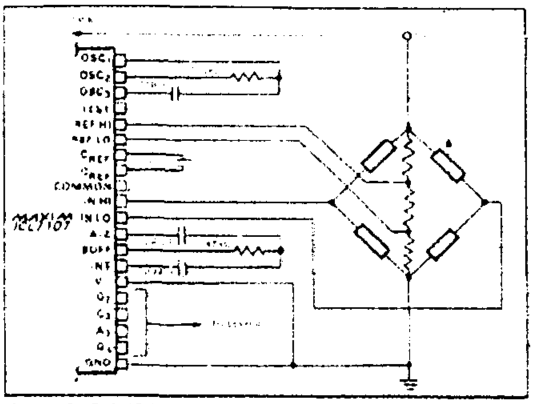


Figure 15. ICL7107 Measuring Ratiometric Values of a Load Cell. Desired Sensitivity is Determined by Resistor Values Within the Bridge.

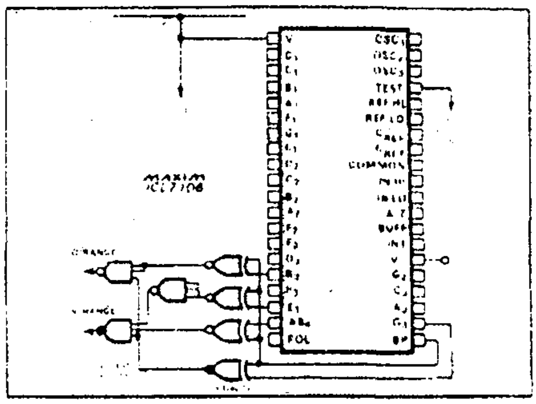


Figure 16. Circuit for Developing Under Range and Over Range Signals from ICL7106 Outputs.

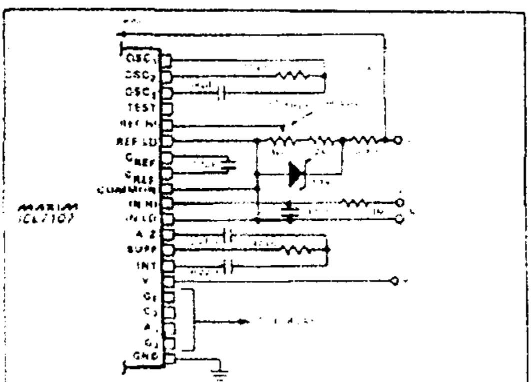


Figure 17. ICL7107 with a 1.2V External Band Gap Reference. V_{IN} Tied to Common

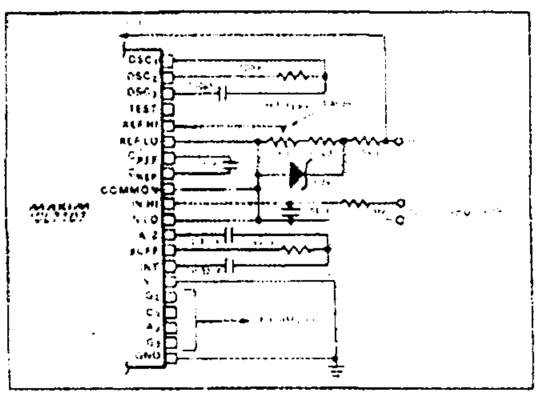
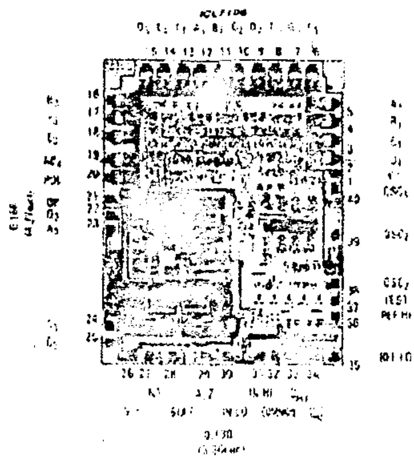


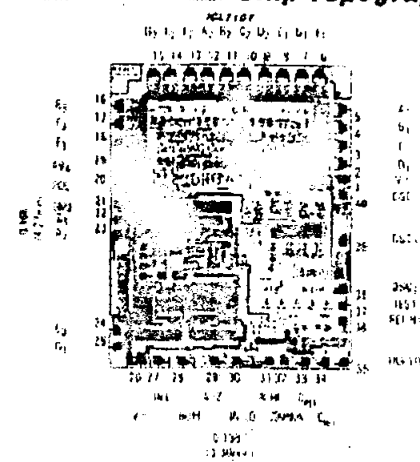
Figure 18. ICL7107 Operated from Single +5V Supply. An External Reference must be used in this application.

3½ Digit A/D Converter

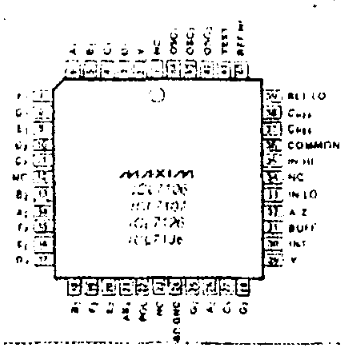
ICL7106/7107

Chip Topographies





Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pack)

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