LAMPIRAN A
KETERANGAN:
Rangkaian di atas menduga berkepanjangan rute:
A. Rangkaian Power Supply
B. Rangkaian Input Level (Limit Switch)
Features
- Compatible with MCS-51™ Products
- 4K Bytes of In-System Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

Description
The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash Programmable and Erasable Read Only Memory (PEROM). The device is manufactured using Atmel’s high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

Pin Configurations
(continued)
Block Diagram

Vcc
GND

RAM ADDR.
REGISTER

RAM

PORT 0 LATCH

PORT 0 DRIVERS

PORT 2 LATCH

PORT 2 DRIVERS

B REGISTER

ACC

STACK POINTER

PROGRAM
ADDRESS
REGISTER

TMP2

TMP1

ALU

INTERRUPT, SERIAL PORT, AND TIMER BLOCKS

PSW

PORT 1 LATCH

PORT 1 DRIVERS

PORT 3 LATCH

PORT 3 DRIVERS

OSC

PSEN

ALE/PROG

EA / Vpp

RST

4-30

AT89C51
The AT89C51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

**Pin Description**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc</td>
<td>Supply voltage.</td>
</tr>
<tr>
<td>GND</td>
<td>Ground.</td>
</tr>
</tbody>
</table>

**Port 0**

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

**Port 1**

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (Ih) because of the internal pullups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

**Port 2**

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (Ih) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

**Port 3**

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (Ih) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

<table>
<thead>
<tr>
<th>Port Pin</th>
<th>Alternate Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>P3.0</td>
<td>RXD (serial input port)</td>
</tr>
<tr>
<td>P3.1</td>
<td>TXD (serial output port)</td>
</tr>
<tr>
<td>P3.2</td>
<td>INT0 (external interrupt 0)</td>
</tr>
<tr>
<td>P3.3</td>
<td>INT1 (external interrupt 1)</td>
</tr>
<tr>
<td>P3.4</td>
<td>T0 (timer 0 external input)</td>
</tr>
<tr>
<td>P3.5</td>
<td>T1 (timer 1 external input)</td>
</tr>
<tr>
<td>P3.6</td>
<td>WR (external data memory write strobe)</td>
</tr>
<tr>
<td>P3.7</td>
<td>RD (external data memory read strobe)</td>
</tr>
</tbody>
</table>

Port 3 also receives some control signals for Flash programming and verification.

**RST**

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

**ALE/PROG**

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

**PSEN**

Program Store Enable is the read strobe to external program memory.
When the AT89C51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

**EA/Vpp**
External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset.

EA should be strapped to VCC for internal program executions.

This pin also receives the 12-volt programming enable voltage (Vpp) during Flash programming, for parts that require 12-volt Vpp.

**XTAL1**
Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

**XTAL2**
Output from the inverting oscillator amplifier.

**Oscillator Characteristics**
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

**Idle Mode**
In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

**Status of External Pins During Idle and Power Down Modes**

<table>
<thead>
<tr>
<th>Mode</th>
<th>Program Memory</th>
<th>ALE</th>
<th>PSEN</th>
<th>PORT0</th>
<th>PORT1</th>
<th>PORT2</th>
<th>PORT3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Idle</td>
<td>Internal</td>
<td>1</td>
<td>1</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
<tr>
<td>Idle</td>
<td>External</td>
<td>1</td>
<td>1</td>
<td>Float</td>
<td>Data</td>
<td>Address</td>
<td>Data</td>
</tr>
<tr>
<td>Power Down</td>
<td>Internal</td>
<td>0</td>
<td>0</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
<tr>
<td>Power Down</td>
<td>External</td>
<td>0</td>
<td>0</td>
<td>Float</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
</tbody>
</table>

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

**Figure 1. Oscillator Connections**

![Figure 1. Oscillator Connections](image1.png)

**Figure 2. External Clock Drive Configuration**

![Figure 2. External Clock Drive Configuration](image2.png)

Note: C1, C2 = 30 pF ± 10 pF for Crystals
      = 40 pF ± 10 pF for Ceramic Resonators
Power Down Mode

In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before VCC is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Lock Bit Protection Modes

<table>
<thead>
<tr>
<th>Program Lock Bits</th>
<th>Protection Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>LB1</td>
<td>LB2</td>
</tr>
<tr>
<td>1</td>
<td>U</td>
</tr>
<tr>
<td>2</td>
<td>P</td>
</tr>
<tr>
<td>3</td>
<td>P</td>
</tr>
<tr>
<td>4</td>
<td>P</td>
</tr>
</tbody>
</table>

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below.

When lock bit 1 is programmed, the logic level at the EA pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of EA be in agreement with the current logic level at that pin in order for the device to function properly.

Programming the Flash

The AT89C51 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage (VCC) program enable signal. The low voltage programming mode provides a convenient way to program the AT89C51 inside the user's system, while the high-voltage programming mode is compatible with conventional third party Flash or EPROM programmers.

The AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

<table>
<thead>
<tr>
<th>Top-Side Mark</th>
<th>VPP = 12V</th>
<th>VPP = 5V</th>
</tr>
</thead>
<tbody>
<tr>
<td>AT89C51</td>
<td>AT89C51</td>
<td>AT89C51</td>
</tr>
<tr>
<td>xxxx</td>
<td>xxxx-5</td>
<td>yyyy</td>
</tr>
<tr>
<td>yyww</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Signature</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(030H)=1EH</td>
<td>(030H)=1EH</td>
<td></td>
</tr>
<tr>
<td>(031H)=51H</td>
<td>(031H)=51H</td>
<td></td>
</tr>
<tr>
<td>(032H)=FFH</td>
<td>(032H)=05H</td>
<td></td>
</tr>
</tbody>
</table>

The AT89C51 code memory array is programmed byte-by-byte in either programming mode. To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.

Programming Algorithm: Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figures 3 and 4. To program the AT89C51, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise EA/Vpp to 12V for the high-voltage programming mode.
5. Pulse ALE/PROG once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89C51 features Data Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/BSY output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.
Programming Interface
Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

<table>
<thead>
<tr>
<th>Mode</th>
<th>RST</th>
<th>PSEN</th>
<th>ALE/PROG</th>
<th>$E\overline{A}/V_{PP}$</th>
<th>P2.6</th>
<th>P2.7</th>
<th>P3.6</th>
<th>P3.7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write Code Data</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>Read Code Data</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>Write Lock</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit - 1</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>Bit - 2</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>Bit - 3</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>Chip Erase</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>Read Signature Byte</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
</tbody>
</table>

Note: 1. Chip Erase requires a 10-ms PROG pulse.

(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/PROG low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.
Flash Programming and Verification Characteristics

\[ T_A = 0^\circ \text{C} \text{ to } 70^\circ \text{C}, \quad V_{\text{CC}} = 5.0 \pm 10\% \]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( v_{\text{PP}}^{(1)} )</td>
<td>Programming Enable Voltage</td>
<td>11.5</td>
<td>12.5</td>
<td>V</td>
</tr>
<tr>
<td>( i_{\text{PE}}^{(1)} )</td>
<td>Programming Enable Current</td>
<td></td>
<td>1.0</td>
<td>mA</td>
</tr>
<tr>
<td>( 1/\text{CL CL} )</td>
<td>Oscillator Frequency</td>
<td>3</td>
<td>24</td>
<td>MHz</td>
</tr>
<tr>
<td>( t_{\text{AVGL}} )</td>
<td>Address Setup to PROG Low</td>
<td>( 48t_{\text{CL CL}} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{\text{GHAX}} )</td>
<td>Address Hold After PROG</td>
<td>( 48t_{\text{CL CL}} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{\text{AVGL}} )</td>
<td>Data Setup to PROG Low</td>
<td>( 48t_{\text{CL CL}} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{\text{GHDX}} )</td>
<td>Data Hold After PROG</td>
<td>( 48t_{\text{CL CL}} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{\text{EHSH}} )</td>
<td>P2.7 (ENABLE) High to ( v_{\text{PP}} )</td>
<td>( 48t_{\text{CL CL}} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{\text{SHGL}} )</td>
<td>( v_{\text{PP}} ) Setup to PROG Low</td>
<td>10</td>
<td></td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td>( t_{\text{GHSL}}^{(1)} )</td>
<td>( v_{\text{PP}} ) Hold After PROG</td>
<td>10</td>
<td></td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td>( t_{\text{GLGH}} )</td>
<td>PROG Width</td>
<td>1</td>
<td>110</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td>( t_{\text{AQV}} )</td>
<td>Address to Data Valid</td>
<td>( 48t_{\text{CL CL}} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{\text{ELQV}} )</td>
<td>ENABLE Low to Data Valid</td>
<td>( 48t_{\text{CL CL}} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{\text{GHQZ}} )</td>
<td>Data Float After ENABLE</td>
<td>0</td>
<td>( 48t_{\text{CL CL}} )</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{GHSBL}} )</td>
<td>PROG High to BUSY Low</td>
<td>1.0</td>
<td></td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td>( t_{\text{WC}} )</td>
<td>Byte Write Cycle Time</td>
<td>2.0</td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>

Note: 1. Only used in 12-volt programming mode.
Flash Programming and Verification Waveforms - High Voltage Mode ($V_{PP} = 12V$)

- P1.0 - P1.7
- P2.0 - P2.3

PORT 0
- PROGRAMMING ADDRESS
- DATA IN
- t_{AVGL} t_{GHDX} t_{GHAH}

ALE/PROG
- t_{SHG} t_{GHS} t_{GHS}

EA/V_{PP}
- V_{PP} LOGIC 1
- LOGIC 0

P2.7
- (ENABLE)

P3.4
- (RDY/BSY)

Flash Programming and Verification Waveforms - Low Voltage Mode ($V_{PP} = 5V$)

- P1.0 - P1.7
- P2.0 - P2.3

PORT 0
- PROGRAMMING ADDRESS
- DATA IN
- t_{AVGL} t_{GHDX} t_{GHAH}

ALE/PROG
- t_{SHG} t_{GHS} t_{GHS}

EA/V_{PP}
- LOGIC 1
- LOGIC 0

P2.7
- (ENABLE)

P3.4
- (RDY/BSY)

READY
Absolute Maximum Ratings*

Operating Temperature: -55°C to +125°C
Storage Temperature: -65°C to +150°C
Voltage on Any Pin with Respect to Ground: -1.0V to +7.0V
Maximum Operating Voltage: 6.6V
DC Output Current: 15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

\( TA = -40°C \) to 85°C, \( V_{CC} = 5.0V \pm 20\% \) (unless otherwise noted)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IL} )</td>
<td>Input Low Voltage (Except EA)</td>
<td>-0.5</td>
<td>0.2 ( V_{CC} ) - 0.1</td>
<td>( V )</td>
<td></td>
</tr>
<tr>
<td>( V_{IL1} )</td>
<td>Input Low Voltage (EA)</td>
<td>-0.5</td>
<td>0.2 ( V_{CC} ) - 0.3</td>
<td>( V )</td>
<td></td>
</tr>
<tr>
<td>( V_{IH} )</td>
<td>Input High Voltage (Except XTAL1, RST)</td>
<td>0.2 ( V_{CC} ) + 0.9</td>
<td>( V_{CC} ) + 0.5</td>
<td>( V )</td>
<td></td>
</tr>
<tr>
<td>( V_{IH1} )</td>
<td>Input High Voltage (XTAL1, RST)</td>
<td>0.7 ( V_{CC} )</td>
<td>( V_{CC} ) + 0.5</td>
<td>( V )</td>
<td></td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Output Low Voltage(1) (Ports 1, 2, 3)</td>
<td>( I_{OL} = 1.6 \text{ mA} )</td>
<td>0.45</td>
<td>( V )</td>
<td></td>
</tr>
<tr>
<td>( V_{OL1} )</td>
<td>Output Low Voltage(1) (Port 0, ALE, PSEN)</td>
<td>( I_{OL} = 3.2 \text{ mA} )</td>
<td>0.45</td>
<td>( V )</td>
<td></td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>Output High Voltage (Ports 1, 2, 3, ALE, PSEN)</td>
<td>( I_{OH} = -60 \mu A, V_{CC} = 5V \pm 10% )</td>
<td>2.4</td>
<td>( V )</td>
<td></td>
</tr>
<tr>
<td> </td>
<td> </td>
<td>( I_{OH} = -25 \mu A )</td>
<td>0.75 ( V_{CC} )</td>
<td>( V )</td>
<td></td>
</tr>
<tr>
<td> </td>
<td> </td>
<td>( I_{OH} = -10 \mu A )</td>
<td>0.9 ( V_{CC} )</td>
<td>( V )</td>
<td></td>
</tr>
<tr>
<td>( V_{OHI} )</td>
<td>Output High Voltage (Port 0 in External Bus Mode)</td>
<td>( I_{OH} = -800 \mu A, V_{CC} = 5V \pm 10% )</td>
<td>2.4</td>
<td>( V )</td>
<td></td>
</tr>
<tr>
<td> </td>
<td> </td>
<td>( I_{OH} = -300 \mu A )</td>
<td>0.75 ( V_{CC} )</td>
<td>( V )</td>
<td></td>
</tr>
<tr>
<td> </td>
<td> </td>
<td>( I_{OH} = -80 \mu A )</td>
<td>0.9 ( V_{CC} )</td>
<td>( V )</td>
<td></td>
</tr>
<tr>
<td>( I_{IL} )</td>
<td>Logical 0 Input Current (Ports 1, 2, 3)</td>
<td>( V_{IN} = 0.45V )</td>
<td>-50</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( I_{HL} )</td>
<td>Logical 1 to 0 Transition Current (Ports 1, 2, 3)</td>
<td>( V_{IN} = 2V, V_{CC} = 5V \pm 10% )</td>
<td>650</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( I_{LU} )</td>
<td>Input Leakage Current (Port 0, EA)</td>
<td>( 0.45 &lt; V_{IN} &lt; V_{CC} )</td>
<td>±10</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( R_{RST} )</td>
<td>Reset Pulldown Resistor</td>
<td> </td>
<td>50</td>
<td>300</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>( C_{IO} )</td>
<td>Pin Capacitance</td>
<td>Test Freq. = 1 MHz, ( TA = 25°C )</td>
<td>10</td>
<td>( pF )</td>
<td></td>
</tr>
<tr>
<td>( I_{CC} )</td>
<td>Power Supply Current</td>
<td>Active Mode, 12 MHz</td>
<td>20</td>
<td>( mA )</td>
<td></td>
</tr>
<tr>
<td> </td>
<td> </td>
<td>Idle Mode, 12 MHz</td>
<td>5</td>
<td>( mA )</td>
<td></td>
</tr>
<tr>
<td> </td>
<td>Power Down Mode(2)</td>
<td>( V_{CC} = 6V )</td>
<td>100</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td> </td>
<td> </td>
<td>( V_{CC} = 3V )</td>
<td>40</td>
<td>( \mu A )</td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. Under steady state (non-transient) conditions, \( I_{OL} \) must be externally limited as follows:
   - Maximum \( I_{OL} \) per port pin: 10 mA
   - Maximum \( I_{OL} \) per 8-bit port: Port 0: 26 mA
     Ports 1, 2, 3: 15 mA
   - Maximum total \( I_{OL} \) for all output pins: 71 mA
   If \( I_{OL} \) exceeds the test condition, \( V_{OL} \) may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum \( V_{CC} \) for Power Down is 2V.
AC Characteristics
(Under Operating Conditions; Load Capacitance for Port 0, ALE/PROG, and PSEN = 100 pF; Load Capacitance for all other outputs = 80 pF)

External Program and Data Memory Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>12 MHz Oscillator</th>
<th>16 to 24 MHz Oscillator</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td></td>
</tr>
<tr>
<td>t1CLCL</td>
<td>Oscillator Frequency</td>
<td>0</td>
<td>24</td>
<td>MHz</td>
</tr>
<tr>
<td>tAHLL</td>
<td>ALE Pulse Width</td>
<td>127</td>
<td>2tCLCL-40</td>
<td>ns</td>
</tr>
<tr>
<td>tAVLL</td>
<td>Address Valid to ALE Low</td>
<td>43</td>
<td>tCLCL-13</td>
<td>ns</td>
</tr>
<tr>
<td>tOLAX</td>
<td>Address Hold After ALE Low</td>
<td>48</td>
<td>tCLCL-20</td>
<td>ns</td>
</tr>
<tr>
<td>tILIV</td>
<td>ALE Low to Valid Instruction In</td>
<td>233</td>
<td>4tCLCL-65</td>
<td>ns</td>
</tr>
<tr>
<td>tILPL</td>
<td>ALE Low to PSEN Low</td>
<td>43</td>
<td>tCLCL-13</td>
<td>ns</td>
</tr>
<tr>
<td>tPLPH</td>
<td>PSEN Pulse Width</td>
<td>205</td>
<td>3tCLCL-20</td>
<td>ns</td>
</tr>
<tr>
<td>tLIV</td>
<td>PSEN Low to Valid Instruction In</td>
<td>145</td>
<td>3tCLCL-45</td>
<td>ns</td>
</tr>
<tr>
<td>tFXX</td>
<td>Input Instruction Hold After PSEN</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>tFXZ</td>
<td>Input Instruction Float After PSEN</td>
<td>59</td>
<td>tCLCL-10</td>
<td>ns</td>
</tr>
<tr>
<td>tFXAV</td>
<td>PSEN to Address Valid</td>
<td>75</td>
<td>tCLCL-8</td>
<td>ns</td>
</tr>
<tr>
<td>tAVIV</td>
<td>Address to Valid Instruction In</td>
<td>312</td>
<td>5tCLCL-55</td>
<td>ns</td>
</tr>
<tr>
<td>tPLAZ</td>
<td>PSEN Low to Address Float</td>
<td>10</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>tIRH4</td>
<td>RD Pulse Width</td>
<td>400</td>
<td>6tCLCL-100</td>
<td>ns</td>
</tr>
<tr>
<td>tWLWH</td>
<td>WR Pulse Width</td>
<td>400</td>
<td>6tCLCL-100</td>
<td>ns</td>
</tr>
<tr>
<td>tRDLV</td>
<td>RD Low to Valid Data In</td>
<td>252</td>
<td>5tCLCL-90</td>
<td>ns</td>
</tr>
<tr>
<td>tRHDX</td>
<td>Data Hold After RD</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>tRHDZ</td>
<td>Data Float After RD</td>
<td>97</td>
<td>2tCLCL-28</td>
<td>ns</td>
</tr>
<tr>
<td>tILODV</td>
<td>ALE Low to Valid Data In</td>
<td>517</td>
<td>8tCLCL-150</td>
<td>ns</td>
</tr>
<tr>
<td>tAVDV</td>
<td>Address to Valid Data In</td>
<td>585</td>
<td>8tCLCL-165</td>
<td>ns</td>
</tr>
<tr>
<td>tIWNL</td>
<td>ALE Low to RD or WR Low</td>
<td>200</td>
<td>3tCLCL-50</td>
<td>ns</td>
</tr>
<tr>
<td>tAWNL</td>
<td>Address to RD or WR Low</td>
<td>203</td>
<td>4tCLCL-75</td>
<td>ns</td>
</tr>
<tr>
<td>tDVWX</td>
<td>Data Valid to WR Transition</td>
<td>23</td>
<td>tCLCL-20</td>
<td>ns</td>
</tr>
<tr>
<td>tDVWH</td>
<td>Data Valid to WR High</td>
<td>433</td>
<td>7tCLCL-120</td>
<td>ns</td>
</tr>
<tr>
<td>tWHOX</td>
<td>Data Hold After WR</td>
<td>33</td>
<td>tCLCL-20</td>
<td>ns</td>
</tr>
<tr>
<td>tRRAZ</td>
<td>RD Low to Address Float</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>tWMH</td>
<td>RD or WR High to ALE High</td>
<td>43</td>
<td>tCLCL-20</td>
<td>ns</td>
</tr>
</tbody>
</table>
External Program Memory Read Cycle

External Data Memory Read Cycle
External Data Memory Write Cycle

External Clock Drive Waveforms

External Clock Drive

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tCLCL</td>
<td>Oscillator Frequency</td>
<td>0</td>
<td>24</td>
<td>MHz</td>
</tr>
<tr>
<td>tCLCL</td>
<td>Clock Period</td>
<td>41.6</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCHCX</td>
<td>High Time</td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCLCX</td>
<td>Low Time</td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCLCH</td>
<td>Rise Time</td>
<td></td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>tCHCL</td>
<td>Fall Time</td>
<td></td>
<td>20</td>
<td>ns</td>
</tr>
</tbody>
</table>
Serial Port Timing: Shift Register Mode Test Conditions
($V_{CC} = 5.0 \, \text{V} \pm 20\% ; \text{Load Capacitance} = 80 \, \text{pF}$)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>12 MHz Osc</th>
<th>Variable Oscillator</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{XULX}$</td>
<td>Serial Port Clock Cycle Time</td>
<td>$1.0 , \mu s$</td>
<td>$12t_{CLCL}$</td>
<td></td>
</tr>
<tr>
<td>$t_{QVXH}$</td>
<td>Output Data Setup to Clock Rising Edge</td>
<td>$700 , \text{ns}$</td>
<td>$10t_{CLCL}-133$</td>
<td></td>
</tr>
<tr>
<td>$t_{XHQX}$</td>
<td>Output Data Hold After Clock Rising Edge</td>
<td>$50 , \text{ns}$</td>
<td>$2t_{CLCL}-117$</td>
<td></td>
</tr>
<tr>
<td>$t_{XHDX}$</td>
<td>Input Data Hold After Clock Rising Edge</td>
<td>$0 , \text{ns}$</td>
<td>$0$</td>
<td></td>
</tr>
<tr>
<td>$t_{XHCOV}$</td>
<td>Clock Rising Edge to Input Data Valid</td>
<td>$700 , \text{ns}$</td>
<td>$10t_{CLCL}-133$</td>
<td></td>
</tr>
</tbody>
</table>

**Shift Register Mode Timing Waveforms**

**AC Testing Input/Output Waveforms**

*Note: 1. AC Inputs during testing are driven at $V_{CC} - 0.5\, \text{V}$ for a logic 1 and $0.45\, \text{V}$ for a logic 0. Timing measurements are made at $V_{IH} \, \text{min.}$ for a logic 1 and $V_{IL} \, \text{max.}$ for a logic 0.*

**Float Waveforms**

*Note: 1. For timing purposes, a port pin is no longer floating when a $100 \, \text{mV}$ change from load voltage occurs. A port pin begins to float when $100 \, \text{mV}$ change from the loaded $V_{OH}/V_{OL} \, \text{level}$ occurs.*
<table>
<thead>
<tr>
<th>Speed (MHz)</th>
<th>Power Supply</th>
<th>Ordering Code</th>
<th>Package</th>
<th>Operation Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>5V ± 20%</td>
<td>AT89C51-12AC</td>
<td>44A</td>
<td>Commercial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12JC</td>
<td>44J</td>
<td>(0°C to 70°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12PC</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12QC</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12AI</td>
<td>44A</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12AJ</td>
<td>44J</td>
<td>(-40°C to 85°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12PI</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12QI</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12AA</td>
<td>44A</td>
<td>Automotive</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12JA</td>
<td>44J</td>
<td>(-40°C to 105°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12PA</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12QA</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>5V ± 20%</td>
<td>AT89C51-16AC</td>
<td>44A</td>
<td>Commercial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16JC</td>
<td>44J</td>
<td>(0°C to 70°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16PC</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16QC</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16AI</td>
<td>44A</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16AJ</td>
<td>44J</td>
<td>(-40°C to 85°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16PI</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16QI</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16AA</td>
<td>44A</td>
<td>Automotive</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16JA</td>
<td>44J</td>
<td>(-40°C to 105°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16PA</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16QA</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>5V ± 20%</td>
<td>AT89C51-20AC</td>
<td>44A</td>
<td>Commercial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20JC</td>
<td>44J</td>
<td>(0°C to 70°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20PC</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20QC</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20AI</td>
<td>44A</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20AJ</td>
<td>44J</td>
<td>(-40°C to 85°C)</td>
</tr>
</tbody>
</table>
## Ordering Information

<table>
<thead>
<tr>
<th>Speed (MHz)</th>
<th>Power Supply</th>
<th>Ordering Code</th>
<th>Package</th>
<th>Operation Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>5V ± 20%</td>
<td>AT89C51-24AC</td>
<td>44A</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24JC</td>
<td>44J</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24PC</td>
<td>44P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24QC</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24AI</td>
<td>44A</td>
<td>Commercial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24JI</td>
<td>44J</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24PI</td>
<td>44P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24QI</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(-40°C to 85°C)</td>
</tr>
</tbody>
</table>

### Package Type

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>44A</td>
<td>44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)</td>
</tr>
<tr>
<td>44J</td>
<td>44 Lead, Plastic J-Leaded Chip Carrier (PLCC)</td>
</tr>
<tr>
<td>40P6</td>
<td>40 Lead, 0.600&quot; Wide, Plastic Dual Inline Package (PDIP)</td>
</tr>
<tr>
<td>44Q</td>
<td>44 Lead, Plastic Gull Wing Quad Flatpack (PQFP)</td>
</tr>
</tbody>
</table>
**LM124/LM224/LM324/LM2902**

**Low Power Quad Operational Amplifiers**

**General Description**

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

**Unique Characteristics**

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage
- The unity gain cross frequency is temperature compensated
- The input bias current is also temperature compensated

**Advantages**

- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and VOUT also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

**Features**

- Internally frequency compensated for unity gain
- Large DC voltage gain
- Wide bandwidth (unity gain) 100 dB
- (temperature compensated)
- Wide power supply range:
  - Single supply 3V to 32V
  - ±1.5V to ±16V
- Very low supply current drain (700 μA)—essentially independent of supply voltage
- Low input biasing current
- (temperature compensated)
- Low input offset voltage
- and offset current
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing
  - 0V to V+ - 1.5V

**Connection Diagram**

Dual-In-Line Package

Top View


See NS Package Number J14A, M14A or N14A

**Order Number LM124AE/883 or LM124E/883**

See NS Package Number E20A

Order Number LM124W/883 or LM124W/883

See NS Package Number W14B
### Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 9)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td>260°C</td>
<td>-65°C to +150°C</td>
<td>260°C</td>
</tr>
<tr>
<td>Lead Temperature (Soldering, 10 seconds)</td>
<td>260°C</td>
<td>260°C</td>
<td>260°C</td>
<td>260°C</td>
</tr>
<tr>
<td>Soldering Information</td>
<td>Dual-In-Line Package</td>
<td>Soldering (10 seconds)</td>
<td>260°C</td>
<td>260°C</td>
</tr>
<tr>
<td>Power Dissipation (Note 1)</td>
<td>1130 mW</td>
<td>1130 mW</td>
<td>215°C</td>
<td>215°C</td>
</tr>
<tr>
<td>Small Outline Package</td>
<td>800 mW</td>
<td>800 mW</td>
<td>225°C</td>
<td>225°C</td>
</tr>
<tr>
<td>See AN-450 &quot;Surface Mounting Methods and Their Effect on Product Reliability&quot; for other methods of soldering surface mount devices.</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>ESD Tolerance (Note 10)</td>
<td>250V</td>
<td>250V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Operating Temperature Range

- LM124A/LM224A/LM324A: 0°C to +70°C
- LM2902: -55°C to +125°C

### Electrical Characteristics

**V^+ = +5.0V, (Note 4), unless otherwise stated**

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</tr>
</thead>
<tbody>
<tr>
<td>Input Offset Voltage</td>
<td>(Note 5) TA = 25°C</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>2</td>
<td>1</td>
<td>3</td>
<td>2</td>
<td>3</td>
<td>2</td>
<td>5</td>
<td>2</td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>V^+ = 30V, V^-= 20V, TA = 25°C</td>
<td>20</td>
<td>50</td>
<td>40</td>
<td>80</td>
<td>45</td>
<td>100</td>
<td>45</td>
<td>150</td>
<td>45</td>
</tr>
<tr>
<td>Input Offset Current</td>
<td></td>
<td>2</td>
<td>10</td>
<td>2</td>
<td>15</td>
<td>5</td>
<td>30</td>
<td>3</td>
<td>30</td>
<td>5</td>
</tr>
<tr>
<td>Input Common-Mode Voltage Range</td>
<td></td>
<td>0</td>
<td>V^+ -1.5</td>
<td>0</td>
<td>V^- -1.5</td>
<td>0</td>
<td>V^+ -1.5</td>
<td>0</td>
<td>V^- -1.5</td>
<td>0</td>
</tr>
<tr>
<td>Supply Current</td>
<td>Over Full Temperature Range</td>
<td>1.5</td>
<td>3</td>
<td>1.5</td>
<td>3</td>
<td>1.5</td>
<td>3</td>
<td>1.5</td>
<td>3</td>
<td>1.5</td>
</tr>
<tr>
<td>Large Signal Voltage Gain</td>
<td></td>
<td>50</td>
<td>100</td>
<td>50</td>
<td>100</td>
<td>25</td>
<td>100</td>
<td>25</td>
<td>100</td>
<td>25</td>
</tr>
<tr>
<td>Common-Mode Rejection Ratio</td>
<td></td>
<td>70</td>
<td>85</td>
<td>70</td>
<td>85</td>
<td>85</td>
<td>85</td>
<td>70</td>
<td>85</td>
<td>85</td>
</tr>
<tr>
<td>Power Supply Rejection Ratio</td>
<td></td>
<td>65</td>
<td>100</td>
<td>65</td>
<td>100</td>
<td>65</td>
<td>100</td>
<td>65</td>
<td>100</td>
<td>65</td>
</tr>
</tbody>
</table>

Units: mV
## Electrical Characteristics \( V^+ = +5.0 \text{V (Note 4)} \) unless otherwise stated (Continued)

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Amplifier-to-Amplifier Coupling (Note 8)</td>
<td>( f = 1 \text{kHz} \text{to} 20 \text{kHz}, T_A = 25^\circ \text{C} ) (Input Referred)</td>
<td>( -120 )</td>
<td>( -120 )</td>
<td>( -120 )</td>
<td>( -120 )</td>
<td>( -120 )</td>
<td>( -120 )</td>
<td>dB</td>
</tr>
<tr>
<td>Output Current Source</td>
<td>( V_{IN}^+ = 1 \text{V}, V_{IN}^- = 0 \text{V}, V^+ = 15 \text{V}, V_O = 0 \text{V}, T_A = 25^\circ \text{C} )</td>
<td>( 20 )</td>
<td>( 40 )</td>
<td>( 20 )</td>
<td>( 40 )</td>
<td>( 20 )</td>
<td>( 40 )</td>
<td>mA</td>
</tr>
<tr>
<td>Output Current Sink</td>
<td>( V_{IN}^+ = 1 \text{V}, V_{IN}^- = 0 \text{V}, V^+ = 15 \text{V}, V_O = 2 \text{V}, T_A = 25^\circ \text{C} )</td>
<td>( 12 )</td>
<td>( 50 )</td>
<td>( 12 )</td>
<td>( 50 )</td>
<td>( 12 )</td>
<td>( 50 )</td>
<td>( 12 )</td>
</tr>
<tr>
<td>Short Circuit to Ground</td>
<td>( \text{(Note 2)} \ V^+ = 15 \text{V}, T_A = 25^\circ \text{C} )</td>
<td>( 40 )</td>
<td>( 60 )</td>
<td>( 40 )</td>
<td>( 50 )</td>
<td>( 40 )</td>
<td>( 50 )</td>
<td>( 40 )</td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>( \text{(Note 5)} )</td>
<td>( 4 )</td>
<td>( 4 )</td>
<td>( 5 )</td>
<td>( 7 )</td>
<td>( 9 )</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Input Offset Voltage Drift</td>
<td>( R_J = 0 \Omega )</td>
<td>( 7 )</td>
<td>( 20 )</td>
<td>( 7 )</td>
<td>( 20 )</td>
<td>( 7 )</td>
<td>( 30 )</td>
<td>( 7 )</td>
</tr>
<tr>
<td>Input Offset Current</td>
<td>( I_{N(+)} = I_{N(-)}, V_{CM} = 0 \text{V} )</td>
<td>( 30 )</td>
<td>( 30 )</td>
<td>( 75 )</td>
<td></td>
<td>( 150 )</td>
<td>( 45 )</td>
<td>( 200 )</td>
</tr>
<tr>
<td>Input Offset Current Drift</td>
<td>( R_J = 0 \Omega )</td>
<td>( 10 )</td>
<td>( 200 )</td>
<td>( 10 )</td>
<td>( 200 )</td>
<td>( 10 )</td>
<td>( 300 )</td>
<td>( 10 )</td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>( I_{N(+)} ) or ( I_{N(-)} )</td>
<td>( 40 )</td>
<td>( 100 )</td>
<td>( 40 )</td>
<td>( 100 )</td>
<td>( 40 )</td>
<td>( 200 )</td>
<td>( 40 )</td>
</tr>
<tr>
<td>Input Common-Mode Voltage Range (Note 7)</td>
<td>( V^+ = +30 \text{V} ) (LM2050; ( V^+ = 26 \text{V} ))</td>
<td>( 0 )</td>
<td>( V^+ - 2 )</td>
<td>( 0 )</td>
<td>( V^+ - 2 )</td>
<td>( 0 )</td>
<td>( V^+ - 2 )</td>
<td>( 0 )</td>
</tr>
<tr>
<td>Large Signal Voltage Gain</td>
<td>( V^+ = +15 \text{V} ) (( V_O ) Swing = 1 \text{V} to 11 \text{V})</td>
<td>( 25 )</td>
<td>( 25 )</td>
<td></td>
<td>( 15 )</td>
<td></td>
<td>( 15 )</td>
<td></td>
</tr>
<tr>
<td>Output Voltage Swing</td>
<td>( V_{OH} )</td>
<td>( V^+ = 30 \text{V} ) (LM2050; ( V^+ = 26 \text{V} ))</td>
<td>( R_L = 2 \Omega )</td>
<td>( 28 )</td>
<td>( 26 )</td>
<td></td>
<td>( 26 )</td>
<td></td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>( V^+ = 5 \text{V}, R_L = 10 \Omega )</td>
<td>( 5 )</td>
<td>( 20 )</td>
<td></td>
<td>( 5 )</td>
<td></td>
<td>( 20 )</td>
<td></td>
</tr>
</tbody>
</table>
### Electrical Characteristics

**v\(^+\) = +5.0V** (Note 4) unless otherwise stated (Continued)

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>V(O) = 2V</td>
<td>V(IN) = +1V, V(IN) = 0V, V(OUT) = 15V</td>
<td>10 20</td>
<td>10 20</td>
<td>10 20</td>
<td>10 20</td>
<td>10 20</td>
<td>10 20</td>
</tr>
<tr>
<td></td>
<td>Sink</td>
<td>V(IN) = +1V, V(IN) = 0V, V(OUT) = 15V</td>
<td>10 15</td>
<td>5 8</td>
<td>5 8</td>
<td>5 8</td>
<td>5 8</td>
<td>5 8</td>
</tr>
</tbody>
</table>

| Units     | mA     |

**Note 1:** For operating at high temperatures, the LM24/LM324A/LM3202 must be derated based on a +150°C maximum junction temperature and a thermal resistance of 80°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM24/LM324A and LM124/LM224A can be derated based on a +150°C maximum junction temperature. The derating is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate at 0 to reduce the power which is dissipated in the integrated circuit.

**Note 2:** Short circuits from the output to V\(^+\) can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 50 mA independent of the magnitude of V\(^+\). At values of supply voltage in excess of +15V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive destruction can result from simultaneous shorts on both amplifiers.

**Note 3:** The input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also inverse FET parasitic transistor action on the IC chip. This transistor action causes the output voltages of the op amp to go to the V\(^+\) voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than +0.3V (at 25°C).

**Note 4:** These specifications are limited to +10°C ≤ TA ≤ +125°C for the LM124/LM224A and LM324/LM3202A. All temperature specifications are limited to −25°C ≤ TA ≤ +85°C, the LM24/LM324A temperature specifications are limited to 0°C ≤ TA ≤ +70°C, and the LM3202 specifications are limited to −40°C ≤ TA ≤ +85°C.

**Note 5:** V\(O\) = 1.0V, R\(P\) = 50Ω with V\(^+\) from 6V to 20V, and over the full input common-mode range (0V to V\(^+\) − 1.25V) for LM24/LM324A, V\(^+\) from 6V to 28V.

**Note 6:** The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the input so no loading change exists on the input lines.

**Note 7:** The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode range voltage is V\(^+\) − 1.25V (at 25°C), but either or both inputs can go to +32V without damage (+28V for LM3202). Independent of the magnitude of V\(^+\).

**Note 8:** Due to proximity of external components, ensure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at frequencies...

**Note 9:** Refer to REF214XX for LM124A military specifications and refer to REF214XX for LM124 military specifications...

**Note 10:** Human body model, 1.5kΩ in series with 100 pF.

### Schematic Diagram

(Each Amplifier)

![Schematic Diagram](image-url)
Typical Performance Characteristics

- **Input Voltage Range**
- **Input Current**
- **Supply Current**

- **Voltage Gain**
- **Open Loop Frequency Response**
- **Common Mode Rejection Ratio**

- **Voltage Follower Pulse Response**
- **Voltage Follower Pulse Response (Small Signal)**
- **Large Signal Frequency Response**

- **Output Characteristics Current Sourcing**
- **Output Characteristics Current Sinking**
- **Current Limiting**
Application Hints

The LM124 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 VDC. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 VDC.

The pins of the package have been designed to simplify PCB board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Provisions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than +V with the proper use of external clamp diodes. Protection should be provided to prevent the input voltages from going negative more than –0.3 VDC (at 25°C). An input clamp diode with a resistor to the IC input terminals can be used.

To reduce the power supply drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion.

Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gain or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

The bias network of the LM124 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 VDC to 30 VDC.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperature. Pulling direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of V^+/2) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.
Typical Single-Supply Applications ($V^+ = 5.0 V_{DC}$)

Non-Inverting DC Gain (0V input - 0V output)

DC Summing Amplifier ($V_{IN} = 0 V_{DC}$ and $V_O = 0 V_{DC}$)

Power Amplifier

Where:

$V_O = V_1 + V_2 - V_3 - V_4$

$V_1 + V_2 > (V_3 + V_4)$ and $V_O > 0 V_{DC}$

LED Driver

"BI-QUAD" RC Active Bandpass Filter

$A_v = 100$ (40 dB)

$Q = 50$

$C = 100$ (40 dB)
Typical Single-Supply Applications ($V^+ = 5 \, V_{DC}$) (Continued)

**Fixed Current Sources**

$$I_2 = \left( \frac{R_1}{R_2} \right) I_1$$

**Lamp Driver**

$30 \, mA$ to $80 \, mA$

**Current Monitor**

$V_0 = \frac{V_{DD}}{1A}$  
$V_0 \approx V^+ - 2V$  
($\text{Pinchoff for } I_a \leq 5 \, mA$)

**Driving TTL**

**Voltage Follower**

$bV = V_0$

**Pulse Generator**
Typical Single-Supply Applications ($V^+ = 5.0 \ V_{DD}$) (Continued)

Squarewave Oscillator

Pulse Generator

High Compliance Current Sink

Low Drift Peak Detector

Comparator with Hysteresis

Ground Referencing a Differential Input Signal

$V_o = 1 \ \text{amp/volt} \ V_{DD}$

(increase $R_2$ for $l_2$ small)

HIGH $Z_{IN}$

LOW $Z_{OUT}$

AUX AMP

INPUT CURRENT

COMPENSATION
Typical Single-Supply Applications ($V^+ - 5.0 \, V_{OC}$) (Continued)

Voltage Controlled Oscillator Circuit

\[ \text{Photo Voltaic-Cell Amplifier} \]

\[ \text{AC Coupled Inverting Amplifier} \]

*Wide control voltage range: $0 \, V_{DC} \leq V_C \leq 2.9 \, V^+ - 1.5 \, V_{OC}$

\[ A_v = \frac{R_3}{R_1} \text{ (As shown, } A_v = 10) \]
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

**AC Coupled Non-Inverting Amplifier**

![AC Coupled Non-Inverting Amplifier Diagram]

- $A_V = \frac{R_2}{R_1}$
- $A_V = 11$ (As shown)

**DC Coupled Low-Pass RC Active Filter**

![DC Coupled Low-Pass RC Active Filter Diagram]

- $f_0 = 1\ kHz$
- $Q = 1$
- $A_V = 2$

**High Input Z, DC Differential Amplifier**

![High Input Z, DC Differential Amplifier Diagram]

- For $\frac{R_1}{R_2} = \frac{R_4}{R_3}$ (CMRR depends on the resistor ratio match)
- $V_o = 1 + \frac{R_4}{R_3}(V_2 - V_1)$
- As shown: $V_o = 2(V_2 - V_1)$
Typical Single-Supply Applications ($V^+ = 5.0V_{DD}$) (Continued)

High Input Z Adjustable-Gain DC Instrumentation Amplifier

If $R_1 = R_5$ & $R_3 = R_4 = R_6 = R_7$ (CMRR depends on match)

$V_O = 1 + \frac{R_1}{R_2}(V_2 - V_1)$

As shown $V_O = 101(V_2 - V_1)$

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)

Bridge Current Amplifier

For $B < 1$ and $R_1 > R$

$V_O = V_{Inp} \left( \frac{R_1}{R} \right)$

TL/4/2090-30
Typical Single-Supply Applications ($V^+ = 5.0 V_{DC}$) (Continued)
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LM124/LM224/LM324/LM2902
Low Power Quad Operational Amplifiers
LM35/LM35A/LM35C/LM35CA/LM35D
Precision Centigrade Temperature Sensors

General Description
The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±0.5°C at room temperature and ±3°C over a full -55°C to +150°C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM35’s low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 μA from its supply, it has very low self-heating, less than 0.1°C in still air. The LM35 is rated to operate over a -55°C to +150°C temperature range, while the LM35C is rated for a -40°C to +125°C range (-10°C with improved accuracy). The LM35 sensors is available packaged in hermetic TO-46 transistor packages, while the LM35C, LM35CA, and LM35D are also available in the plastic TO-92 transistor package. The LM35D is also available in an 8-lead surface mount small outline package and a plastic TO-202 package.

Features
- Calibrated directly in °Celsius (Centigrade)
- Linearity = 10.0 mV/°C scale factor
- ±0.5°C accuracy guaranteed (at +25°C)
- Rated for full -55°C to +150°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4 to 30 volts
- Less than 60 μA current drain
- Low self-heating, 0.08°C in still air
- Nonlinearity only ±0.5°C typical
- Low impedance output, 0.1 Ω for 1 mA load

Connection Diagrams

Connection Diagrams

**TO-92**
Metal Can Package

**TO-202**
Plastic Package

**SO-8**
Small Outline Molded Package

Order Number LM35H, LM35AH
LM35CH, LM35CAH or LM35DH
See NS Package Number H03H

Order Number LM35CZ
LM35CAZ or LM35EZ
See NS Package Number Z03A

Order Number LM35DM
See NS Package Number M08A

**Typical Applications**

**FIGURE 1. Basic Centigrade Temperature Sensor (+2°C to +150°C)**

Choose Rf = -Vg/50 μA

Vout = +1,500 mV at +150°C
= +500 mV at +20°C
= -500 mV at -55°C

**FIGURE 2. Full-Range Centigrade Temperature Sensor**
### Absolute Maximum Ratings (Note 10)
- Supply Voltage: +35V to -0.2V
- Output Voltage: +6V to -1.0V
- Output Current: 10 mA
- Supply Temp., TO-46 Package: -60°C to +180°C
- TO-92 Package: -60°C to +150°C
- SO-8 Package: -65°C to +150°C
- TO-202 Package: -65°C to +150°C

### Lead Temp.
- TO-46 Package, (Soldering, 10 seconds): 300°C
- TO-92 Package, (Soldering, 10 seconds): 250°C
- TO-202 Package, (Soldering, 10 seconds): +230°C

### Electrical Characteristics (Note 1) (Note 6)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>LM35A</th>
<th>LM35CA</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Typical</td>
<td>Tested Limit (Note 4)</td>
</tr>
<tr>
<td>Accuracy</td>
<td>TA = 25°C</td>
<td>±0.2</td>
<td>±0.5</td>
</tr>
<tr>
<td>(Note 7)</td>
<td>TA = -10°C</td>
<td>±0.3</td>
<td>±1.0</td>
</tr>
<tr>
<td></td>
<td>TA = TMAX</td>
<td>±0.4</td>
<td>±1.0</td>
</tr>
<tr>
<td></td>
<td>TA = TMIN</td>
<td>±0.18</td>
<td>±0.35</td>
</tr>
<tr>
<td>Nonlinearity</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sensor Gain</td>
<td>TMIN = TA = TMAX</td>
<td>+10.0</td>
<td>+9.9</td>
</tr>
<tr>
<td>Average Slope</td>
<td>TA = 25°C</td>
<td>±0.4</td>
<td>±1.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>±0.5</td>
<td>±1.0</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>TMIN = TA = TMAX</td>
<td>±0.01</td>
<td>±0.05</td>
</tr>
<tr>
<td>(Note 2)</td>
<td>TMIN = TMAX</td>
<td>±0.02</td>
<td>±0.01</td>
</tr>
<tr>
<td></td>
<td>4V ≤ VG ≤ 30V</td>
<td>±0.02</td>
<td>±0.01</td>
</tr>
<tr>
<td>Line Regulation</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dropout Current</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Note 5)</td>
<td>Vg = +SV, +25°C</td>
<td>50</td>
<td>67</td>
</tr>
<tr>
<td></td>
<td>Vg = +SV, +5V</td>
<td>105</td>
<td>131</td>
</tr>
<tr>
<td></td>
<td>Vg = +30V +25°C</td>
<td>50.5</td>
<td>68</td>
</tr>
<tr>
<td></td>
<td>Vg = +30V, +5V</td>
<td>105.5</td>
<td>133</td>
</tr>
<tr>
<td></td>
<td>4V ≤ VG ≤ 30V</td>
<td>±0.3</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td>4V ≤ VG ≤ 30V</td>
<td>±0.3</td>
<td>2.0</td>
</tr>
<tr>
<td>Oscillating Current</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Note 3)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cutoff Temperature</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Note 7)</td>
<td></td>
<td></td>
<td></td>
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<td></td>
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</tr>
<tr>
<td>Temperature</td>
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<tr>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Coefficient of Dropoff Current</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Note 3)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vacuum Temperature In Rated Accuracy</td>
<td>In circuit of Figure 1, C = 0</td>
<td>+1.5</td>
<td>+2.0</td>
</tr>
<tr>
<td>Long Term Stability</td>
<td>TJ = TMAX, for 1000 hours</td>
<td>±0.08</td>
<td>±0.08</td>
</tr>
</tbody>
</table>

Note 1: Unless otherwise noted, these specifications apply: -55°C ≤ Tj ≤ +125°C for the LM35 and LM35A, -40°C ≤ Tj ≤ +10°C for the LM35C and LM35CA, and -5°C ≤ Tj ≤ +100°C for the LM335. Vg = +5V and ILOAD = 50 μA, in the circuit of Figure 2. These specifications also apply Tj = +2°C to TMAX at the bottom of Table 1. Specifications in boldface apply over the full rated temperature range.

Note 2: In circuit of Figure 2, C = 0.

Note 3: Dropout resistance of the TO-46 package is 400Ω/V, junction to ambient, and 24Ω/V function to case. Dropout resistance of the TO-92 package is 24Ω/V function to case. Dropout resistance of the small outline module package is 220Ω/V function to ambient. Dropout resistance of the TO-202 package is 120Ω/V function to ambient. For additional thermal resistance information see table in the Applications section.

Note 5: Specifications in boldface apply over the full rated temperature range.

Note 6: Dropout resistance of the TO-46 package is 400Ω/V, junction to ambient, and 24Ω/V function to case. Dropout resistance of the TO-92 package is 24Ω/V function to case. Dropout resistance of the small outline module package is 220Ω/V function to ambient. Dropout resistance of the TO-202 package is 120Ω/V function to ambient. For additional thermal resistance information see table in the Applications section.
### Electrical Characteristics (Note 1) (Note 6) (Continued)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>LM35</th>
<th>LM35C, LM35D</th>
</tr>
</thead>
<tbody>
<tr>
<td>Accuracy, LM35, LM35C (Note 7)</td>
<td>$T_A = +25°C$</td>
<td>$0.4 \leq 1.0$</td>
<td>$0.4 \leq 1.0$</td>
</tr>
<tr>
<td></td>
<td>$T_A = -10°C$</td>
<td>$0.5 \leq 1.0$</td>
<td>$0.5 \leq 1.0$</td>
</tr>
<tr>
<td></td>
<td>$T_A = T_{MAX}$</td>
<td>$0.8 \leq 1.5$</td>
<td>$0.8 \leq 1.5$</td>
</tr>
<tr>
<td></td>
<td>$T_A = T_{MIN}$</td>
<td>$0.8 \leq 1.5$</td>
<td>$0.8 \leq 1.5$</td>
</tr>
<tr>
<td>Accuracy, LM35D (Note 7)</td>
<td>$T_A = +25°C$</td>
<td>$0.6 \leq 1.5$</td>
<td>$0.6 \leq 1.5$</td>
</tr>
<tr>
<td></td>
<td>$T_A = T_{MAX}$</td>
<td>$0.9 \leq 2.0$</td>
<td>$0.9 \leq 2.0$</td>
</tr>
<tr>
<td></td>
<td>$T_A = T_{MIN}$</td>
<td>$0.9 \leq 2.0$</td>
<td>$0.9 \leq 2.0$</td>
</tr>
<tr>
<td>Nonlinearity (Note 8)</td>
<td>$T_{MIN} \leq T_A \leq T_{MAX}$</td>
<td>$0.3 \leq 0.2$</td>
<td>$0.3 \leq 0.2$</td>
</tr>
<tr>
<td>Sensor Gain (Average Slope)</td>
<td>$T_{MIN} \leq T_A \leq T_{MAX}$</td>
<td>$0.9 \leq 0.2$</td>
<td>$0.9 \leq 0.2$</td>
</tr>
<tr>
<td>Load Regulation (Note 3)</td>
<td>$0 \leq I_L \leq 1 \text{ mA}$</td>
<td>$0.4 \leq 2.0$</td>
<td>$0.4 \leq 2.0$</td>
</tr>
<tr>
<td></td>
<td>$T_A = +25°C$</td>
<td>$0.3 \leq 2.0$</td>
<td>$0.3 \leq 2.0$</td>
</tr>
<tr>
<td>Line Regulation (Note 5)</td>
<td>$V_S = +5V, +25°C$</td>
<td>$0.01 \leq 0.01$</td>
<td>$0.01 \leq 0.01$</td>
</tr>
<tr>
<td></td>
<td>$4V \leq V_S \leq 30V$</td>
<td>$0.02 \leq 0.02$</td>
<td>$0.02 \leq 0.02$</td>
</tr>
<tr>
<td>Quiescent Current (Note 5)</td>
<td>$V_S = +5V, +25°C$</td>
<td>$56 \leq 80$</td>
<td>$56 \leq 80$</td>
</tr>
<tr>
<td></td>
<td>$V_S = +5V$</td>
<td>$105 \leq 158$</td>
<td>$105 \leq 158$</td>
</tr>
<tr>
<td></td>
<td>$V_S = 30V, +25°C$</td>
<td>$56.2 \leq 56$</td>
<td>$56.2 \leq 56$</td>
</tr>
<tr>
<td></td>
<td>$V_S = 30V$</td>
<td>$105.5 \leq 151$</td>
<td>$105.5 \leq 151$</td>
</tr>
<tr>
<td>Change of Quiescent Current (Note 3)</td>
<td>$4V \leq V_S \leq 30V, +25°C$</td>
<td>$0.2 \leq 0.2$</td>
<td>$0.2 \leq 0.2$</td>
</tr>
<tr>
<td></td>
<td>$4V \leq V_S \leq 30V$</td>
<td>$0.5 \leq 0.5$</td>
<td>$0.5 \leq 0.5$</td>
</tr>
<tr>
<td>Temperature Coefficient of Quiescent Current</td>
<td>$V_S = 30V, +25°C$</td>
<td>$+0.39 \leq +0.39$</td>
<td>$+0.39 \leq +0.39$</td>
</tr>
<tr>
<td>Minimum Temperature for Rated Accuracy</td>
<td>In circuit of Figure 1, $I_L = 0$</td>
<td>$+1.5 \leq +1.5$</td>
<td>$+2.0 \leq +2.0$</td>
</tr>
<tr>
<td>Long Term Stability</td>
<td>$T_J = T_{MAX}$, for 1000 hours</td>
<td>$0.08 \leq 0.08$</td>
<td>$0.08 \leq 0.08$</td>
</tr>
</tbody>
</table>

**Units:**
- $\mu$A
- $\text{mV/}^\circ\text{C}$
- $\mu$A/$^\circ\text{C}$
- $^\circ\text{C}$

---

**Notes:**
1. Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.
2. Test limits are guaranteed and 100% tested in production.
3. Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.
4. Specifications in this data sheet apply over the full rated temperature range.
5. Accuracy is defined as the error between the output voltage and 10mV/°C times the device's case temperature, at specified conditions of voltage, current, and temperature (expressed in °C).
6. Nonlinearity is defined as the deviation of the output-voltage versus-temperature curve from the best-fit straight line, over the device's rated temperature range.
7. Quiescent current is defined in the circuit of Figure 1.
8. Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note 1.
9. Human body model, 100 pf discharged through a 1.5 kΩ resistor.
10. See AN-493 "Surface Mounting Methods and Their Effects on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of ordering surface mount devices.
Applications

The LM35 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about 0.01°C of the surface temperature.

This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature of the LM35 die would be at an intermediate temperature between the surface temperature and the air temperature. This is especially true for the TO-92 plastic package, where the copper leads are the principal thermal path to carry heat into the device, so its temperature might be closer to the air temperature than to the surface temperature.

To minimize this problem, be sure that the wiring to the LM35, as it leaves the device, is held at the same temperature as the surface of interest. The easiest way to do this is to cover up these wires with a bead of epoxy which will insure that the leads and wires are all at the same temperature as the surface, and that the LM35 die's temperature will not be affected by the air temperature.

<table>
<thead>
<tr>
<th>Package</th>
<th>Temperature Rise of LM35 Due To Self-heating (Thermal Resistance)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TO-46</td>
<td>Still air 40°C/CW, 100°C/CW, 167°C/CW, 10°C/CW, 14°C/CW, 22°C/CW, 25°C/CW, 40°C/CW</td>
</tr>
<tr>
<td>TO-46</td>
<td>Moving air 100°C/CW, 45°C/CW, 90°C/CW, 70°C/CW, 10°C/CW, 25°C/CW, 40°C/CW</td>
</tr>
<tr>
<td>TO-82</td>
<td>Still oil 100°C/CW, 45°C/CW, 90°C/CW, 70°C/CW, 10°C/CW, 25°C/CW, 40°C/CW</td>
</tr>
<tr>
<td>TO-82</td>
<td>Soldered oil 90°C/CW, 45°C/CW, 90°C/CW, 70°C/CW, 10°C/CW, 25°C/CW, 40°C/CW</td>
</tr>
<tr>
<td>TO-202</td>
<td>(Clamped to metal, infinite heat sink) (24°C/CW)</td>
</tr>
<tr>
<td>TO-202</td>
<td>(23°C/CW)</td>
</tr>
</tbody>
</table>

* Waterfed type 201, or 1" disc of 0.020" sheet brass, soldered to case, or similar
** TO-92 and SO-8 packages glued and heat soldered to 1" square of 3/16" printed circuit board with 0.010" or similar.

Typical Applications (Continued)

CAPACITIVE LOADS

Like most microcircuit circuits, the LM35 has a limited ability to drive heavy capacitive loads. The LM35 by itself is able to drive 50 pf without special precautions. However, when heavy loads are anticipated, it is easy to isolate or decouple the load with a resistor; see Figure 3. Or you can improve the tolerance of capacitance by using a series R-C damper from output to ground, see Figure 4.

When the LM35 is applied with a 200 pf load resistor as shown in Figure 5, 6, or 8, it is relatively immune to wiring capacitance because the capacitance forms a bypass from ground to input, not on the output. However, as with any linear circuit connected to wires in a hostile environment, its performance can be affected adversely by intense electromagnetic sources such as relays, radio transmitters, motors with arcing brushes, SCR transistors, etc., as its wiring can act as a receiving antenna and its internal junctions can act as rectifiers. For best results in such cases, a by-pass capacitor from Vout to ground and a series R-C damper such as 753 in series with 0.2 or 1 µF output to ground are often useful. These are shown in Figures 13, 14, and 15.
Typical Applications (Continued)

FIGURE 5. Two-Wire Remote Temperature Sensor (Grounded Sensor)

FIGURE 6. Two-Wire Remote Temperature Sensor (Output Referred to Ground)

FIGURE 7. Temperature Sensor, Single Supply, -55°C to +150°C

FIGURE 8. Two-Wire Remote Temperature Sensor (Output Referred to Ground)

FIGURE 9. 4-To-20 mA Current Source (0°C to +100°C)

FIGURE 10. Fahrenheit Thermometer
Typical Applications (Continued)

FIGURE 11. Centigrade Thermometer (Analog Meter)

FIGURE 12. Expanded Scale Thermometer (50° to 80° Fahrenheit, for Example Shown)

FIGURE 13. Temperature to Digital Converter (Serial Output) (< 125°C Full Scale)

FIGURE 14. Temperature to Digital Converter (Parallel TRI-STATE® Outputs for Standard Data Bus to µP Interface) (125°C Full Scale)
Typical Applications (Continued)

FIGURE 15. Bar-Graph Temperature Display (Dot Mode)

FIGURE 16. LM35 With Voltage-To-Frequency Converter And Isolated Output
(2°C to -150°C; 20 Hz to 1500 Hz)
**National Semiconductor**

**LM136-2.5/LM236-2.5/LM336-2.5V Reference Diode**

**General Description**

The LM136-2.5/LM236-2.5 and LM336-2.5 integrated circuits are precision 2.5V shunt regulator diodes. These monolithic IC voltage references operate as a low-temperature-coefficient 2.5V zener with 0.2Ω dynamic impedance. A guard terminal on the LM336-2.5 allows the reference voltage and temperature coefficient to be trimmed easily.

The LM136-2.5 series is useful as a precision 2.5V low-voltage reference for digital voltmeters, power supplies or op-amp circuits. The 2.5V make it convenient to obtain a stable reference from 5V logic supplies. Further, since the LM136-2.5 operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

The LM136-2.5 is rated for operation over -55°C to -125°C while the LM236-2.5 is rated over a -25°C to -85°C temperature range.

**Features**

- Low temperature coefficient
- Wide operating current of 400 μA to 10 mA
- 0.2Ω dynamic impedance
- ±1% initial tolerance available
- Guaranteed temperature stability
- Easily trimmed for minimum temperature drift
- Fast turn-on
- Three lead transistor package

**Connection Diagrams**

**TO-92**

Plastic Package

**TO-46**

Metal Can Package

**SO Package**

**Typical Applications**

2.5V Reference

2.5V Reference with Minimum Temperature Coefficient

Wide Input Range Reference

The LM336-2.5 is rated for operation over a 0°C to +70°C temperature range. See the connection diagrams for available packages.
Absolute Maximum Ratings (Note 1)

If military/aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Reverse Current: 15 mA
Forward Current: 10 mA
Storage Temperature: -60°C to +150°C
Operating Temperature Range (Note 2)
- LM136: -55°C to +150°C
- LM236: -25°C to +85°C
- LM336: 0°C to +70°C

Soldering Information
- TO-92 Package (10 sec.): 260°C
- TO-46 Package (10 sec.): 300°C
- SO Package: Vapor Phase (60 sec.): 215°C
- Infrared (15 sec.): 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Electrical Characteristics (Note 3)

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Reverse Breakdown Voltage</td>
<td>TA = 25°C, IQ = 1 mA</td>
<td>2.440</td>
<td>2.490</td>
<td>2.540</td>
<td>2.390</td>
</tr>
<tr>
<td></td>
<td>LM136, LM236, LM336</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LM136A, LM236A, LM336A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reverse Breakdown Change With Current</td>
<td>VA Adjusted to 2.490V IQ = 1 mA (Figure 2)</td>
<td>2.6</td>
<td>1</td>
<td>2.6</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>0°C ≤ TA ≤ 70°C (LM336)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>-25°C ≤ TA ≤ 85°C (LM236H, LM236Z)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>-25°C ≤ TA ≤ 85°C (LM236M)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>-5°C ≤ TA ≤ -125°C (LM136)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Stability (Note 1)</td>
<td>TA = 25°C, IQ = 1 mA, f = 100 Hz</td>
<td>0.2</td>
<td>0.6</td>
<td>0.2</td>
<td>1</td>
</tr>
<tr>
<td>Reverse Dynamic Impedance</td>
<td>VA Adjusted to 2.490V IQ = 1 mA (Figure 2)</td>
<td>3.5</td>
<td>18</td>
<td>7.5</td>
<td>18</td>
</tr>
<tr>
<td></td>
<td>0°C ≤ TA ≤ 70°C (LM336)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>-25°C ≤ TA ≤ 85°C (LM236H, LM236Z)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>-25°C ≤ TA ≤ 85°C (LM236M)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>-5°C ≤ TA ≤ -125°C (LM136)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reverse Breakdown Change With Current</td>
<td>400 μA ≤ IQ ≤ 10 mA</td>
<td>3</td>
<td>10</td>
<td>3</td>
<td>12</td>
</tr>
<tr>
<td>Reverse Dynamic Impedance</td>
<td>IQ = 1 mA</td>
<td>0.4</td>
<td>1</td>
<td>0.4</td>
<td>1.4</td>
</tr>
<tr>
<td>Long Term Stability</td>
<td>TA = 25°C ± 0.1°C, IQ = 1 mA, t = 1000 hrs</td>
<td>20</td>
<td>20</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: For elevated temperature operation, t, max is:
- LM136: 150°C
- LM236: 125°C
- LM336: 100°C

Note 3: Unless otherwise specified, the LM136-2.5 is mounted from -55°C to 85°C, the LM236-2.5 from -25°C to 85°C and the LM336-2.5 from 0°C to 85°C.

Note 4: Temperature stability for the LM136 and LM236 family is guaranteed by design. Design limits are guaranteed but not 100% production tested over indicated temperature and supply voltage ranges. These limits are not used to calculate output quality levels. Stability is defined as the maximum change in fA from 75°C to 25°C (mean of Tj Max).
Application Hints

The LM135 series voltage references are much easier to use than ordinary zener diodes. Their low impedance and wide operating current range simplify biasing in almost any circuit. Further, either the breakdown voltage or the temperature coefficient can be adjusted to optimize circuit performance.

Figure 1 shows an LM136 with a 10k potentiometer for adjusting the reverse breakdown voltage. With the addition of R1 the breakdown voltage can be adjusted without affecting the temperature coefficient of the device. The adjustment range is usually sufficient to adjust for both the initial device imbalance and inaccuracies in buffer circuitry.

If minimum temperature coefficient is desired, two diodes can be added in series with the adjustment potentiometer as shown in Figure 2. When the device is adjusted to 2.490V the temperature coefficient is minimized. Almost any silicon signal diode can be used for this purpose such as a 1N914, 1N4148 or a 1N457. For proper temperature compensation the diodes should be in the same thermal environment as the LM136. It is usually sufficient to mount the diodes near the LM136 on the printed circuit board. The absolute resistance of R1 is not critical and any value from 2k to 20k will work.

FIGURE 1. LM136 With Pot for Adjustment of Breakdown Voltage
(Trim Range = ±120 mV typical)

FIGURE 2. Temperature Coefficient Adjustment
(Trim Range = ±70 mV typical)
Typical Applications (Continued)

Low Cost 2 Amp Switching Regulator

Precision Power Regulator with Low Temperature Coefficient

Trimmed 2.5V Reference with Temperature Coefficient Independent of Breakdown Voltage
Typical Applications (Continued)

Adjustable Shunt Regulator

OUTPUT 3V to 9V

Linear Ohmmeter

LM138

CALIBRATE

LM326-2.5

LM312

VOUT
Typical Applications (Continued)

Op Amp with Output Clamped

Bipolar Output Reference

2.5V Square Wave Calibrator
ADC0801, ADC0802, ADC0803, ADC0804, ADC0805 8-Bit μP Compatible A/D Converters

General Description
The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and NS6800A derivative control bus with TRI-STATE® output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features
- Compatible with 8080 μP derivatives—no interfacing logic needed - access time - 155 ns
- Easy interface to all microprocessors, or operates "stand alone"

Key Specifications
- Resolution 8 bits
- Total error ± ¼ LSB, ± ⅛ LSB and ± ⅛ LSB
- Conversion time 100 μs

Typical Applications

<table>
<thead>
<tr>
<th>Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Part Number</td>
</tr>
<tr>
<td>-------------</td>
</tr>
<tr>
<td>ADC0801</td>
</tr>
<tr>
<td>ADC0802</td>
</tr>
<tr>
<td>ADC0803</td>
</tr>
<tr>
<td>ADC0804</td>
</tr>
<tr>
<td>ADC0805</td>
</tr>
</tbody>
</table>
### Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributor for availability and specifications.

- **Supply Voltage (VCC)** (Note 5): 6.5V
- **Storage Temperature Range**: -65°C to 150°C
- **Package Dissipation at TA = 25°C**: 875 mW
- **ESD Susceptibility** (Note 10): 600V

### Operating Ratings (Notes 1 & 2)

- **Temperature Range**:
  - TA_MIN ≤ TA ≤ TA_MAX
  - -55°C ≤ TA ≤ +125°C
  - -40°C ≤ TA ≤ +85°C
  - -40°C ≤ TA ≤ +85°C
  - -4°C ≤ TA ≤ +70°C
  - 0°C ≤ TA ≤ +70°C
  - 0°C ≤ TA ≤ +70°C
  - Range of VCC:
    - 4.5 VCC to 6.3 VCC

### Electrical Characteristics

The following specifications apply for VCC = 5 VCC, TA_MIN ≤ TA ≤ TA_MAX and fCLK = 640 kHz unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC0801: Total Adjusted Error (Note 8)</td>
<td>With Full-Scale Adj. (See Section 2.2)</td>
<td>± 1/2 LSB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC0802: Total Unadjusted Error (Note 8)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC0803: Total Adjusted Error (Note 8)</td>
<td>With Full-Scale Adj. (See Section 2.2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC0804: Total Unadjusted Error (Note 8)</td>
<td></td>
<td>± 1/2 LSB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC0805: Total Unadjusted Error (Note 8)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VREF/2 Input Resistance (Pin 6)</td>
<td>ADC0801/02/03/05</td>
<td>2.5 kΩ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ADC0804 (Note 8)</td>
<td>0.75 kΩ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Analog Input Voltage Range (Note 4)</td>
<td>V(+ ) or V(− )</td>
<td>GND - 0.05 VCC ± 0.05 VCC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DC Common-Mode Error</td>
<td>Over Analog Input Voltage Range</td>
<td>± 1/4 LSB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Supply Sensitivity</td>
<td>VCC = 5 VCC ± 10% Over Allowed VSS(+) and VSS(−) Voltage Range (Note 4)</td>
<td>± 1/8 LSB</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### AC Electrical Characteristics

The following specifications apply for VCC = 5 VCC and TA = 25°C unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>TC</td>
<td>Conversion Time</td>
<td>LA8 = 64kHz (Note 6)</td>
<td>103</td>
<td>114</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>TC</td>
<td>Conversion Time</td>
<td>(Note 5, 6)</td>
<td>66</td>
<td>73</td>
<td>1/CLK</td>
<td></td>
</tr>
<tr>
<td>fCLK</td>
<td>Clock Frequency</td>
<td>VCC = 5V, (Note 5)</td>
<td>100</td>
<td>640</td>
<td>1490 kHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Clock Duty Cycle</td>
<td>(Note 5)</td>
<td>40</td>
<td>50</td>
<td>60 %</td>
<td></td>
</tr>
<tr>
<td>CR</td>
<td>Conversion Rate in Free-Running Mode</td>
<td>RTMR fed to WR with</td>
<td>8770</td>
<td>8708</td>
<td>conv/s</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CS = 0 and fCLK = 640 kHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WFR(1)</td>
<td>Width of WR Input (Start Pulse Width)</td>
<td>CS = 0 VCC (Note 7)</td>
<td>150</td>
<td>150 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDD(1)</td>
<td>Access Time (Delay from Falling Edge of RD to Output Data Valid)</td>
<td>Cl = 100 pF</td>
<td>135</td>
<td>200 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tHH, tHH</td>
<td>TRI-STATE Control (Delay from Rising Edge of RD to Hi-Z State)</td>
<td>Cl = 10 pF, RL = 10k</td>
<td>125</td>
<td>200 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(See TRI-STATE Test Circuits)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tHH, tHH</td>
<td>Delay from Falling Edge of WR or RD to Reset of INTR</td>
<td>500</td>
<td>450 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tIC, tIC</td>
<td>Input Capacitance of Logic Control Inputs</td>
<td>5</td>
<td>7.5</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cout</td>
<td>TRI-STATE Output Capacitance (Data Buffers)</td>
<td>5</td>
<td>7.5</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**CONTROL INPUTS**: (Note: GLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately.)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL(1)</td>
<td>Logical “1” Input Voltage</td>
<td>VCC = 5.5 VCC</td>
<td>2.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOH(1)</td>
<td>Logical “1” Input Voltage</td>
<td>(Except Pin 4 CLK IN)</td>
<td>15</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### AC Electrical Characteristics (Continued)

The following specifications apply for \( V_{CC} = 5 \text{VDC} \) and \( 10^5 \leq T_A \leq T_{MAX} \), unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IN} ) (0)</td>
<td>Logical “0” Input Voltage (Except Pin 4 CLK IN)</td>
<td>( V_{CC} - 0.75 \text{VDC} )</td>
<td>0.8</td>
<td></td>
<td></td>
<td>VCC</td>
</tr>
<tr>
<td>( I_{IN} ) (1)</td>
<td>Logical “1” Input Current (All Inputs)</td>
<td>( 5 \text{VDC} )</td>
<td>0.005</td>
<td>1</td>
<td></td>
<td>( \mu \text{ADC} )</td>
</tr>
<tr>
<td>( I_{IN} ) (0)</td>
<td>Logical “0” Input Current (All Inputs)</td>
<td>( 0 )</td>
<td>-1</td>
<td>-0.005</td>
<td></td>
<td>( \mu \text{ADC} )</td>
</tr>
</tbody>
</table>

#### CLOCK IN AND CLOCK IN

- **\( V_{TT} \)**: CLK IN (Pin 4) Positive Going Threshold Voltage
  - 2.7 VCC
- **\( V_{TN} \)**: CLK IN (Pin 4) Negative Going Threshold Voltage
  - 1.5 VCC
- **\( V_H \)**: CLK IN (Pin 4) Hysteresis
  - 0.6 VCC
- **\( V_{OUT} \)**: Logical “0” CLK R Output Voltage
  - \( I_O = 360 \mu \text{A} \)
  - \( V_{CC} = 4.75 \text{VDC} \)
- **\( I_{OUT} \)**: Logical “1” CLK R Output Voltage
  - \( I_O = 20 \mu \text{A} \)
  - \( V_{CC} = 4.75 \text{VDC} \)

#### DATA OUTPUTS AND IN/IN

- **\( V_{OUT} \)**: Logical “0” Output Voltage
  - Data Outputs
  - \( I_{OUT} = 1.6 \text{mA} \), \( V_{CC} = 4.75 \text{VDC} \)
  - \( I_{OUT} = 1.0 \text{mA} \), \( V_{CC} = 4.75 \text{VDC} \)
  - \( I_{OUT} = 0.4 \text{mA} \), \( V_{CC} = 4.75 \text{VDC} \)
- **\( V_{OUT} \)**: Logical “1” Output Voltage
  - \( I_O = 360 \mu \text{A} \)
  - \( V_{CC} = 4.75 \text{VDC} \)
  - \( I_O = 20 \mu \text{A} \)
  - \( V_{CC} = 4.75 \text{VDC} \)
  - \( I_O = 3 \mu \text{A} \)
  - \( V_{CC} = 4.75 \text{VDC} \)

#### POWER SUPPLY

- **\( I_{CC} \)**: Supply Current (Includes Ladder Current)
  - \( (\text{CLK} = 640 \text{kHz}) \)
  - \( V_{REF2} = \text{NC} \), \( T_A = 25^\circ \text{C} \)
  - \( I_{CC} = 6.0 \text{mA} \)
  - \( V_{REF12} = \text{NC} \), \( T^- = 25^\circ \text{C} \)
  - \( I_{CC} = 1.9 \text{mA} \)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified. The separate A GND point should always be wired to the 0 GND.

Note 3: A single diode exists, internally, from \( V_{CC} \) to GND and has a typical breakdown voltage of \( 7 \text{VDC} \).

Note 4: For \( V_{CC} = 12 \text{VDC} \) the diode output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the \( V_{CC} \) supply. This is because during testing at low \( V_{CC} \) levels (3.5V), the on-chip diode will be forward biased. The same applies in the case of \( V_{CC} = 5 \text{VDC} \). This means that as long as the analog \( V_{IN} \) does not exceed the supply voltage by more than 50 mV, the output diodes will be correct. To achieve an absolute 5 Vpp (an analog \( V_{IN} \)) the output diodes will therefore require a minimum supply voltage of 4.5 \( V_{CC} \) over temperature variations, initial tolerance, and loading.

Note 5: Accuracy is guaranteed at \( V_{CC} = 5 \text{VDC} \). At higher \( V_{CC} \) frequencies accuracy can degrade. For lower \( V_{CC} \) frequencies, the device's cycle limits can be extended to allow for the maximum clock high/low times. The maximum clock has a 3% duty cycle limit.

Note 6: With an asynchronous start pulse, up to 6 clock periods may be required before the internal clock phases are properly synchronized. This is due to the length of time it takes for the clock to stabilize.

Note 7: The \( V_{CC} \) input is assumed to be equal to the \( V_{CC} \) output and therefore timing is dependent on the \( V_{CC} \) input. An arbitrary worst-case pulse width will hold the converter in a Reset mode and the start of conversion is determined by the clock frequency of the WRT pulse (see timing diagram).

Note 8: None of these A/OS requires a zero adjust (see section 7.5.1). To obtain zero code at other analog input voltages see section 7.5 and Figure 5.

Note 9: The \( V_{REF} \) pin is the center point of a two resistive divider connected from \( V_{CC} \) to ground. Each resistor is 2.2k, except for the \( V_{CC} \) input where each resistor is 1.0k. The analog input resolution is the sum of the two equal resistors.

Note 10: Human body model, 100 pf discharged through a 1.5 kΩ resistor.
Typical Performance Characteristics

- Logic Input Threshold Voltage vs. Supply Voltage
- Delay From Falling Edge of RD to Output Data Valid vs. Load Capacitance
- CLK IN Schmitt Trip Levels vs. Supply Voltage
- fCLK vs. Clock Capacitor
- Full-Scale Error vs. Conversion Time
- Effect of Unadjusted Offset Error vs. VREF/2 Voltage
- Output Current vs. Temperature
- Power Supply Current vs. Temperature (Note 9)
- Linearity Error at Low VREF/2 Voltages
Timing Diagrams (All timing is measured from the 50% voltage points)

Output Enable and Reset HIGH

Note: Read strobe must occur 8 clock periods (8/clk) after assertion of interrupt to guarantee reset of INT.
Typical Applications (Continued)

6400 Interface

- Ratiometric with Full-Scale Adjust

Absolute with a 2.500V Reference

Absolute with a 5V Reference

Zero-Shift and Span Adjust: 2V ≤ V_IN ≤ 5V

Span Adjust: 0V ≤ V_IN ≤ 3V

Note: For use, see also LM385-2.5
Typical Applications (Continued)

Directly Converting a Low-Level Signal

A μP Interfaced Comparator

1 mV Resolution with μP Controlled Range

Digitizing a Current Flow
Self-Clocking Multiple A/Ds

External Clocking

- Use a large R value to reduce loading on CLK R output.
- VREF12 for feedback

Self-Clocking in Free-Running Mode

μP Interface for Free-Running A/D

- After power-up, a momentary grounding of the WR input is needed to guarantee operation.

Operating with "Automotive" Ratiometric Transducers

Reliometric with VREF/2 Forced

- VREF = 1.067 VCC
- 15% of VCC = VDEAD, > 85% of VCC

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Typical Applications (Continued)

µP Compatible Differential-Input Comparator with Pre-Set Vth (with or without Hysteresis)

Handling ±10V Analog Inputs

Low-Cost, µP Interfaced, Temperature-to-Digital Converter

µP Interfaced Temperature-to-Digital Converter

*See figure 2 to deduce H value

DBT = "01" for Vth < VREF < 0.3V (Vth < 0.3V)

Omit circuitry within the dotted area if hysteresis is not needed.

Craft

- Gain is Qo + 12fC
- Calibration and readout as earlier, except for

A/D can then be calibrated with a pre-set input voltage.

Cambridge Instruments # 654-8R10K resistor array

*All values shown are for T A = T s = 25°C

**Can calibrate each sensor to allow easy replacement, then

A/D can be calibrated with a pre-set input voltage.
Handling 15V Analog Input

Analog Self-Test for a System

A Low-Disturbance Logarithmic Converter

Protecting the Input

Input Interface

Handling 15V Analog Inputs

Provided by: PERSATUAN
Ungaran Kelola Wilma Management
SURA DATA
3-Decade Logarithmic A/D Converter

A, B, C, D = LM324A

Noise Filtering the Analog Input

Multiplexing Differential Inputs

Output Buffers with A/D Data Enabled

Increasing Bus Drive and/or Reducing Time on Bus

If applied, output data is undelayed 1 CLK period prior to assertion of INTR.
Sampling an AC Input Signal

Note 1: Oversample whenever possible (use a > 2k - 8C) to eliminate input frequency folding (aliasing) and to allow for the skirt responses of the filter.
Note 2: Consider the amplitude errors which are introduced within the passband of the filter.

70% Power Savings by Clock Gating

(Please note that the 70% power saving is achieved by clock gating.

Power Savings by A/D and VREF Shutdown

*Use ADC0801, 02, 03 or 05 for lower power consumption.
Note: Logic inputs can be driven to 0V with A/D supply at zero volts.
Buffer prevents data bus from overpowering output of A/D when in shutdown mode.

3-27
1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in Figure 1a. The horizontal scale is analog input voltage and the vertical points labeled are in steps of 1 LSB (19.55 mV with 2.5V tied to the VREF/2 pin). The digital output codes that correspond to these inputs are shown as D = 0, 1, and D + 1. For the perfect A/D, not only will center-value (A - 1, A, A + 1, ... ) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located ± 1/2 LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend ± 1/2 LSB from the ideal center-values. Each broad (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

Figure 1b shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the 1% worst case error is guaranteed to be no closer to the center value points than ± 1/2 LSB. In other words, if we apply an analog input equal to the center-value ± 1/2 LSB, we guarantee that the A/D will produce the correct digital code. The center value of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than 1/2 LSB.

The error curve of Figure 1c shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of Figure 1a is ± 1/2 LSB because the digital code appeared 1/2 LSB in advance of the center-value of the linear. The error plots always have a constant negative slope and the largest upward slope is always 1 LSB in magnitude.

FIGURE 1. Clarifying the Error Specs of an A/D Converter
2.0 FUNCTIONAL DESCRIPTION

The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage \(V_{AD} = V_{AG} - V_{AB}\) to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 6-bit binary code \(111111 = \text{full-scale}\) is transferred to an output latch and then an interrupt is asserted (INTR makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting INTR to the WR input with \(CS = 0\). To ensure start-up under all possible conditions, an external WR pulse is required during the first power-up cycle.

On the high-to-low transition of the WR input the internal SAR latches and the shift register stages are reset. As long as the CS input and WR input remain low, the A/D will remain in a reset state. Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.

Conversion begins with the least significant bit. The internal SAR latch makes a low-to-high transition on the start event. The logic circuit, G1, controls the logic to ensure a valid output. This logic therefore allows for wide CS and WR signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

A functional diagram of the A/D converter is shown in Figure 2. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having CS and WR simultaneously low. This sets the start flip-flop (F/F) and the result of "1" level resets the 8-bit shift register, resets the interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is then the input end of the 8-bit shift register. Internal clock signals then transfer the "1" to the C output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (with WR or CS is a "1") the start F/F resets and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide CS and WR signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

FIGURE 2. Block Diagram
After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR FF/F to set. An inverting buffer then supplies the INTR input signal.

Note that this SET control of the INTR FF/F remains low for 8 of the external clock periods (as the internal clocks run at 1/4 of the frequency of the external clock). If the data output is continuously enabled (CS and RD both held low), the INTR output will still signal the end of conversion (by a high-to-low transition), because the SET input can control the Q output of the INTR FF/F even though the RESET input is constantly at a "1" level in this operating mode. This INTR output will therefore stay low for the duration of the SET signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode (INTR pin tied to WR and CS wired low—see also section 2.8), the START FF/F is SET by the high-to-low transition of the INTR signal. This resets the SHIFT REGISTER which causes the input to the C-type latch, LATCH 1, to go low. As the latch enable input is still present, the C output will go high, which then allows the INTR FF/F to be RESET. This reduces the width of the resulting INTR output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both CS and RD being low will cause the INTR FF/F to be reset, and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs (CS, RD, and WR) meet standard TTL logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor-based applications, the CS input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the WR input (pin 3) and the Output Enable function is caused by an active low pulse at the RD input (pin 2).

2.2 Analog Differential Voltage inputs and Common-Mode Rejection

The A/D has additional applications flexibility due to the analog differential voltage input. The \( V_{IN}(-) \) input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input. The time interval between sampling \( V_{IN}(+) \) and \( V_{IN}(-) \) is 4-5 clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

\[
\Delta V_{IN}(MAX) = (V_p) \left( \frac{4.5}{f_{CLK}} \right).
\]

where:

\[ \Delta V_p \] is the error voltage due to sampling delay.

\[ V_p \] is the peak value of the common-mode voltage.

\[ f_{CLK} \] is the common-mode frequency.

As an example, to keep this error to \( \frac{1}{4} \) LSB (5 mV) when operating with a 60 Hz common-mode frequency, \( f_{CLK} \) and using a 640 kHz A/D clock, \( f_{CLK} \) would allow a peak value of the common-mode voltage, \( V_p \), which is given by:

\[
V_p = \left( \frac{5 \times 10^{-5}}{(640 \times 10^3)} \right) \left( \frac{6.28}{6.28 \times 0.04 \times 0.01} \right)
\]

which gives

\[ V_p = 1.9V. \]

The allowed range of analog input voltages usually places more severe restrictions on input common-mode voltage levels.

An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3.1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in Figure 3.

\[
\text{FIGURE 3. Analog Input Impedance}
\]
The voltage on this capacitive is switched and will result in currents entering the \( V_{IN}(+) \) input pin and leaving the \( V_{IN}(-) \) input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and do not cause errors as the on-chip comparator is strobed at the end of the clock period.

**Fault Mode**

If the voltage source applied to the \( V_{IN}(+) \) or \( V_{IN}(-) \) pin exceeds the allowed operating range of \( V_{CC} \pm 50 \text{ mV} \), large input currents can flow through a parasitic diode to the \( V_{CC} \) pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the \( V_{CC} \) pin (with the current bypassed with this diode, the voltage at the \( V_{IN}(+) \) pin can exceed the \( V_{CC} \) voltage by the forward voltage of this diode).

**2.2.2 Input Bypass Capacitors**

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistance to the analog signal sources. This charge pumping action is worse for continuous conversions with the \( V_{IN}(+) \) input voltage at full-scale. For continuous conversions with a 3.5 kHz clock frequency, the \( V_{IN}(+) \) input is at 5V, this DC current is at a maximum of approximately 5 \( \mu \text{A} \). Therefore, bypass capacitors should not be used at the analog input of the \( V_{INF} \) pin for high resistance sources (\( > 1 \) k\( \Omega \)).

**2.2.3 Input Source Resistance**

Large values of source resistance where an input bypass capacitor is not used, will not cause errors as the input currents settle out prior to the comparison time. If a low pass filter is required on the system, use a low valued series resistor (\( \leq 1 \) k\( \Omega \)) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, \( \leq 1 \) k\( \Omega \), a 0.1 \( \mu \text{F} \) bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long wire. A 100\( \Omega \) series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

**2.3.4 Noise**

The leads to the analog inputs (pin 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 k\( \Omega \). Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust \( V_{REF}/2 \) for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

**2.4 Reference Voltage**

**2.4.1 Span Adjust**

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 \( V_{CC} \), 2.5 \( V_{CC} \) or an adjusted voltage range, this has been achieved in the design of the IC as shown in Figure 4.

**FIGURE 4. The VREF Design on the IC**

Notice that the reference voltage for the IC is either \( 1/2 \) of the voltage applied to the \( V_{CC} \) supply pin, or equal to the voltage that is externally forced at the \( V_{REF}/2 \) pin. This allows for a ratiometric voltage reference using the \( V_{CC} \) supply, or a 5 \( V_{CC} \) reference voltage can be used for the \( V_{CC} \) supply or a voltage less than 2.5 \( V_{CC} \) can be applied to the \( V_{REF}/2 \) input for increased application flexibility. The internal gain to the \( V_{REF}/2 \) input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.0 \( V_{CC} \) to 3.5 \( V_{CC} \) instead of 0V to 5 \( V_{CC} \), the span would be 3V as shown in Figure 5. With 0.5 \( V_{CC} \) applied to the \( V_{IN}(+) \) pin to absorb the offset, the reference voltage can be made equal to \( 1/2 \) of the 3V span or 1.5 \( V_{CC} \). The A/D now willocode the \( V_{IN}(+) \) signal from 0.5V to 2.5V with the 0.5V input corresponding to zero and the 3.5 \( V_{CC} \) input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.
2.4.2 Reference Accuracy Requirements

The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The AD08005 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For VREF/2 voltages of 2.5 V, nominal value, initial errors of ±10 mV will cause conversion errors of ±1 LSB due to the gain of 2 of the VREF/2 input. In reduced span applications, the initial value and the stability of the VREF/2 input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the VREF/2 input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (0 mV max) over 0°C ≤ TA ≤ 70°C. Other temperature range parts are also available.

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, \( V_{IN}(MIN) \), is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D \( V_{IN}^- \) input at this \( V_{IN}(MIN) \) value (see Applications section). This utilizes the differential mode operation of the A/D. The zero error of the A/D converter relates to the location of the first rise of the transfer function and can be measured by grounding the \( V_{IN}^- \) input and applying a small magnitude positive voltage to the \( V_{IN}^+ \) input. Zero error is the difference between the actual DC-input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal 1/2 LSB value (1/2 LSB = 9.8 mV for \( V_{REF}/2 = 2.500 \ V_{DC} \)).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1/2 LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the \( V_{REF}/2 \) input (pin 9 or the \( V_{CC} \) supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.
2.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground) this may zero reference should be properly adjusted first. A $V_{ADJ(+)}$ voltage that equals this desired zero reference plus $1/2$ LSB (where the LSD is calculated for the desired analog span, 1 LSB = analog span/256) is applied to pin 8 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 01H6X to 01H6X code transition.

The full-scale adjustment should then be made (with the proper $V_{ADJ(-)}$ voltage applied) by forcing a voltage to the $V_{ADJ(+)}$ input which is given by:

$$V_{ADJ(+)} = V_{MAX} - 1.5 \left( \frac{V_{MAX} - V_{MIN}}{256} \right)$$

where:

- $V_{MAX}$ = The high end of the analog input range
- $V_{MIN}$ = The low end (the offset zero) of the analog range.

(Both are ground referenced.)

The $V_{ADJ(\pm)}$ (or $V_{ADJ}$) voltage is then adjusted to provide a code change from FFFFH to FFH6X. This completes the adjustment procedure.

2.5 Clocking Option

The clock for the A/D can be derived from the CPU clock, or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in Figure 6.

![Figure 6. Self-Clocking the A/D](image)

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D convertor clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard TTL buffer).

2.7 Restarting During a Conversion

If the A/D is restarted (SS and WR go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the date of the previous conversion remains in this latch. The INT output simply remains at the "1" level.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the CR input is grounded and the WRI input is tied to the INT pin. This WRI and INT node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MCS A/D, like all CMOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRISTATE (high impedance mode). Backplane busing also greatly adds to the stray capacitance of the data bus.

Thus there are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus end therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads and/or writes by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if it is short and capacitive loading is high, external bus drivers must be used. These can be TRISTATE buffers (low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the $V_{CC}$ supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter. $V_{CC}$ pin and values of 1 uF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the $V_{CC}$ supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for constructing this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.
A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitor, analog input filter capacitor, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of $1/2$ LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in Figure 7.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.550 Vcc and a Vcc supply voltage of 5.12 Vcc should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.000 Vcc (5.120 - 1/2 LSB) should be applied to the $V_{IN}(+) pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). Table I shows the fractional binary equivalent of these 2-bit groups. By adding the voltages obtained from the "MS" and "LS" columns in Table I, the nominal value of the digital display (when $V_{REF}/2 = 2.560$V) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 Vcc. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpolation of the test results.

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in Figure 8. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, "A - C", directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis). The construction details of a tester of this type are provided in the NSC application note AN-179, "Analog-to-Digital Converter Testing".

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of Figure 9, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides 1/2 LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error on the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

4.0 MICROPROCESSOR INTERFACING

To discuss the interface with 8080A and 6800 microprocessors, a common example subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space using standard memory address decoding for CS and the MEMR and MEMW strobes or it can be controlled as an I/O device by using the I70 R and I70 W strobes and decoding the address bits A9 → A0 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the CS input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in Figure 10.
**TABLE I. DECODING THE DIGITAL OUTPUT LEDs**

<table>
<thead>
<tr>
<th>HEX</th>
<th>BINARY</th>
<th>FRACTIONAL BINARY VALUE FOR OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2 = 2.560$ Voc</th>
<th>VMS GROUP*</th>
<th>VLS GROUP*</th>
</tr>
</thead>
<tbody>
<tr>
<td>F</td>
<td>1 1 1 1</td>
<td>7/8 15/16 LS GROUP 15/256</td>
<td>4.800</td>
<td>0.300</td>
</tr>
<tr>
<td>E</td>
<td>1 1 1 0</td>
<td>7/8 13/16 LS GROUP 13/256</td>
<td>4.480</td>
<td>0.280</td>
</tr>
<tr>
<td>D</td>
<td>1 1 0 1</td>
<td>3/4 1/64 LS GROUP 1/256</td>
<td>4.160</td>
<td>0.260</td>
</tr>
<tr>
<td>C</td>
<td>1 1 0 0</td>
<td>1/2 1/32 LS GROUP 1/64</td>
<td>3.840</td>
<td>0.240</td>
</tr>
<tr>
<td>B</td>
<td>1 0 1 1</td>
<td>5/8 11/16 LS GROUP 11/256</td>
<td>3.520</td>
<td>0.220</td>
</tr>
<tr>
<td>A</td>
<td>1 0 1 0</td>
<td>3/8 7/16 LS GROUP 7/256</td>
<td>3.200</td>
<td>0.200</td>
</tr>
<tr>
<td>9</td>
<td>1 0 0 1</td>
<td>1/4 1/64 LS GROUP 1/64</td>
<td>2.880</td>
<td>0.180</td>
</tr>
<tr>
<td>8</td>
<td>1 0 0 0</td>
<td>1/2 1/32 LS GROUP 1/64</td>
<td>2.560</td>
<td>0.160</td>
</tr>
<tr>
<td>7</td>
<td>0 1 1 1</td>
<td>3/8 3/16 LS GROUP 3/256</td>
<td>2.240</td>
<td>0.140</td>
</tr>
<tr>
<td>6</td>
<td>0 1 1 0</td>
<td>5/16 5/32 LS GROUP 5/128</td>
<td>1.920</td>
<td>0.120</td>
</tr>
<tr>
<td>5</td>
<td>0 1 0 1</td>
<td>1/8 1/16 LS GROUP 1/64</td>
<td>1.600</td>
<td>0.100</td>
</tr>
<tr>
<td>4</td>
<td>0 1 0 0</td>
<td>1/4 1/64 LS GROUP 1/64</td>
<td>1.280</td>
<td>0.080</td>
</tr>
<tr>
<td>3</td>
<td>0 0 1 1</td>
<td>3/16 3/64 LS GROUP 3/128</td>
<td>0.960</td>
<td>0.060</td>
</tr>
<tr>
<td>2</td>
<td>0 0 1 0</td>
<td>1/8 1/16 LS GROUP 1/64</td>
<td>0.640</td>
<td>0.040</td>
</tr>
<tr>
<td>1</td>
<td>0 0 0 1</td>
<td>1/16 1/64 LS GROUP 1/64</td>
<td>0.320</td>
<td>0.020</td>
</tr>
<tr>
<td>0</td>
<td>0 0 0 0</td>
<td>0 0 LS GROUP 0 0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

*Decimal Output = VMS Group + VLS Group
SAMPLE PROGRAM FOR FIGURE 10 ADC0801-INS8080A CPU INTERFACE

```assembly
0038 C3 00 03 RST 7: JMP LD DATA
0100 21 00 02 START:
0103 31 00 04 RETURN:
0106 7D LXI H '0200H
0107 FE 0F MOV A, L
0109 C4 13 01 CP 0FH
010C D5 E0 JC CNT
010F FB JEJ X
0110 C3 07 01 LOOP:
0113 CONT:
0300 DB 0E LD DATA:
0302 77 MOV A, X
0303 93 INX H
0304 C3 03 01 JMP RETURN
```

Note 1: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

Note 2: All address values were arbitrarily chosen.
**Functional Description (Continued)**

The standard control bus signals of the 8080 CS, RD and WR can be directly used to the digital control inputs of the A/D and the bus timing requirements are met to allow both the interface and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

### 4.1.1 Sample 8080A CPU Interfacing Circuity and Program

The following sample program and associated hardware shown in Figure 10 may be used to input data from the converter to the INS8080A CPU chip set (comprising of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate CS for the converter.

It is important to note that in systems where the A/D converter is 1-of-N or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as CS inputs—one for each I/O device.

### 4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see Figure 11) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit D of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals RD, WR and INT of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The RD and WR signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.

**Figure 11. INS8048 Interface**

**SAMPLE PROGRAM FOR FIGURE 11 INS8048 INTERFACE**

| 04 10 | JMP LCH | Program starts at offset 10 |
| 04 50 | ORC 3H |
| 89 FE | JMP 50H | Interrupt jump vector |
| 81   | ORC 10H | Main program |
| 89 01 | ANL Pl, #0FEH | Chip select |
| 81   | MOV A, #F1 | Read in the 1st data |
| 89 20 | ORL Pl, #1 | To reset the interrupt |
| 89 FF | MOV RO, #20H | Set port pin high |
| 8A 10 | MOV R1, #0FH | Data address |
| 23 FF | MOV K2, #10H | Dummy address |
| 89 FE | MOV A, #0FH | Count for 16 bytes |
| 81   | ANL Pl, #0FEH | Set ACC for inter loop |
| 85   | MOV GPZ, A | Send CS (bit 0 of Pl) |
| 84 21 | JNZ LOOP | Send WR out |
| 9A 18 | DJNZ R2, AGAIN | Enable interrupt |
| 00   | NOP | Wait for interrupt |
| 81   | INDATA | If 16 bytes are read |
| 04 20 | INDCS | gets user's program |
| 04 20 | MOVX A, #81 | Input data, CS still low |
| 80   | MOV A, RO | Store in memory |
| 18   | INC PO | Increment storage counter |
| 69 01 | ORL Pl, #1 | Reset CS signal |
| 27   | CLR A | Clear ACC to get out of |
| 93   | RETR | the interrupt loop |

3-37
4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General RD and WR strobes are provided and separate memory request, MREQ, and I/O request, IREQ, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the RD and WR strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in Figure 13. Additional I/O advantages exist as software DMA routines are available and can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the RD and WR strobe signals. Instead it employs a single R/W line and additional timing, if needed, can be derived from the 62 clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. Figure 14 shows an Interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the CS decoding is shown using 1/2 DM0092. Note that in many 6800 systems, an 

The following subroutine performs essentially the same function as in the case of the CS80A interface and it can be called from anywhere in the user's program. In Figure 15 the ADC8001 series is interfaced to the M6800 microprocessor through the (arbitrarily chosen) Port B of the M6820 or MC6821 Peripheral Interface Adapter (PIA). Here the CS pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no CS decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D RD pin can be grounded.

A sample interface program equivalent to the previous section is shown below Figure 15. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor that is desired.

5.1 Multiple ADC801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sampled simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in Figure 16.
Functional Description (Continued)

SAMPLE PROGRAM FOR FIGURE 14 ADC0801-MC6800 CPU INTERFACE

0010 DF 36 DATAIN STX TEMP2 ; Save contents of X
0012 CE 00 2C LDX #FF02C ; Upon IRC lw CPU
0015 FF 7B STD $FF7B ; Jumps to 002C
0018 57 50 00 STA $5000 ; Start ADC0801
001B GE CLI
001C 3E CONVRT WAI ; Wait for interrupt
001D DE 34 LDX TEMP1
001F BC 00 07 CPX #0007F ; Is final data stored?
0022 27 14 BEQ ENDFP
0024 57 50 00 STAA $5000 ; Restarts ADC0801
0027 08 INX
002A DF 34 STX TEMP1
002D 20 7D BRA CONVRT
002E DE 34 IDTRPT LDX TEMP1
0030 DE 50 00 LDAA $5000 ; Read data
0033 A7 00 STA $X ; Store it at X
0036 38 RTI
0039 02 00 TEMP1 FDB $0200 ; Starting address for
003C 00 00 TEMP2 FDB $0000 ; data storage
003F CE 02 00 ENDP LDX #10200 ; Reinitialize TEMP1
0042 DF 34 STX TEMP1
0045 DE 36 LDX TEMP2
0048 DF 39 RTS ; Return from subroutine

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

FIGURE 15. ADC0801-MC6820 PIA INTERFACE
The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

All the converters are started simultaneously with a STORE instruction at HEX address 5000. Noting that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the CS inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to ensure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to C207, before returning to the user's program. All CPU registers then recover their original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.
Functional Description (Continued)

**FIGURE 16: Interfacing Multiple A/DTs in an MC6800 System**

**SAMPLE PROGRAM FOR FIGURE 16 INTERFACING MULTIPLE A/DTs IN AN MC6800 SYSTEM**

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>HEX CODE</th>
<th>MINEMONICS</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0010</td>
<td>DF 44</td>
<td>DATAIN</td>
<td>STX</td>
</tr>
<tr>
<td>0012</td>
<td>CE 00 2A</td>
<td>STX</td>
<td>#$002A</td>
</tr>
<tr>
<td>0015</td>
<td>YYYY FB</td>
<td>STX</td>
<td>#$FFFB</td>
</tr>
<tr>
<td>0018</td>
<td>BP 50 00</td>
<td>STL A</td>
<td>$5000</td>
</tr>
<tr>
<td>0019</td>
<td>DX</td>
<td>CLD</td>
<td></td>
</tr>
<tr>
<td>001C</td>
<td>3X</td>
<td>RST</td>
<td></td>
</tr>
<tr>
<td>001D</td>
<td>CE 00 00</td>
<td>LDX INDEX1</td>
<td></td>
</tr>
<tr>
<td>0020</td>
<td>DF 4C</td>
<td>LDX INDEX2</td>
<td></td>
</tr>
<tr>
<td>0022</td>
<td>CE 02 00</td>
<td>LDX TEMP</td>
<td></td>
</tr>
<tr>
<td>0025</td>
<td>DF 42</td>
<td>LDX INDEX1</td>
<td></td>
</tr>
<tr>
<td>0027</td>
<td>DX 44</td>
<td>LDX INDEX2</td>
<td></td>
</tr>
<tr>
<td>0029</td>
<td>39</td>
<td>RST</td>
<td></td>
</tr>
<tr>
<td>002A</td>
<td>CE 40</td>
<td>INTRPT</td>
<td>LDX INDEX1</td>
</tr>
<tr>
<td>002C</td>
<td>A3 00</td>
<td>LI A X</td>
<td>Read data in from A/DT at X</td>
</tr>
<tr>
<td>002E</td>
<td>0B</td>
<td>LDA</td>
<td>X ← INDEX</td>
</tr>
<tr>
<td>002F</td>
<td>DF 4C</td>
<td>STL INDEX1</td>
<td>INDEX1 ← INDEX2</td>
</tr>
<tr>
<td>0031</td>
<td>DF 44</td>
<td>LDX INDEX2</td>
<td>INDEX2 ← V</td>
</tr>
</tbody>
</table>
### SAMPLE PROGRAM FOR FIGURE 16 INTERFACING MULTIPLE A/D IN AN MCS480 SYSTEM

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>HEX CODE</th>
<th>MENTONICS</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0033</td>
<td>A7 00</td>
<td>STA X</td>
<td>Store data at X</td>
</tr>
<tr>
<td>0035</td>
<td>BC 02 97</td>
<td>CPU #0007</td>
<td>Have all A/D's been read?</td>
</tr>
<tr>
<td>0038</td>
<td>27 05</td>
<td>BEQ #0007</td>
<td>( A\rightarrow D1 )</td>
</tr>
<tr>
<td>003A</td>
<td>08</td>
<td>INX</td>
<td>( X \rightarrow index )</td>
</tr>
<tr>
<td>003B</td>
<td>DF 42</td>
<td>STX INDEX2</td>
<td>Increase X by one</td>
</tr>
<tr>
<td>003D</td>
<td>20 ER</td>
<td>BRA INTRPT</td>
<td>Branch to 002A</td>
</tr>
<tr>
<td>003F</td>
<td>38</td>
<td>RETURN REI</td>
<td></td>
</tr>
<tr>
<td>0040</td>
<td>50 00</td>
<td>INDEX1 FBD</td>
<td>30000</td>
</tr>
<tr>
<td>0042</td>
<td>02 00</td>
<td>INDEX2 FDB</td>
<td>30000</td>
</tr>
<tr>
<td>0044</td>
<td>00 00</td>
<td>TEMP FDB</td>
<td>30000</td>
</tr>
</tbody>
</table>

Note: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be incremented in the user's program.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. Figure 17 is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the IN8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 \( \mu V \) for 1/2 LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

\[
V_o = \frac{1}{1 + \frac{R1}{2R2}} \cdot \left( V_{in+} - V_{in-} \right)
\]

where \( V_{in+} \) is the input through resistor \( R_1 \). All of the offset error terms can be cancelled by making \( \frac{1}{2R2} \cdot R_1 = V_{OS} \). This is the principle of this auto-zeroing scheme.

The IN8080A uses the 3 I/O ports of an IN8255 Programmable Peripheral Interface (PPI) to control the auto-zeroing and input data from the ADC0801 as shown in Figure 18. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preampl. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage \( V_2 \) increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A1 is approximately 2.5\( V \) so that a logic "1" (5\( V \)) on any output of Port B will source current into node \( V_2 \) thus raising the voltage at \( V_2 \) and making the differential output more negative. Conversely, a logic "0" (0\( V \)) will pull current out of node \( V_2 \) and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, \( V_2 \) can move \( \pm 12 \, mV \) with a resolution of 50 \( \mu V \), which will null the offset error term to 1/2 LSB of full-scale for the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0\( V \) to 5\( V \) is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a single 5\( V \) source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.

```
Functional Description (Continued)

Note 1: $R_2 = 49.5 \text{ k}\Omega$

Note 2: Switches are LMC2094 CMOS analog switches.

Note 3: The resistors used in the buffer-zero section can be ±5% tolerance.

FIGURE 17. Gain of 100 Differential Transducer Preamp

FIGURE 18. Microprocessor Interface Circuitry for Differential Preamp
5.3 Multiple A/D Converters in a Z-80 Interrupt

Driver Mode

In data acquisition systems where more than one A/D converter (or other peripheral devices) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. Figure 21 and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion (RTTR asserted) and is requesting an interrupt. This circuit allows starting the A/D converters and reading valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit OR latch. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identical word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.

FIGURE 19. Flow Chart for Auto-Zero Routine
![Image](image_url)

FIGURE 20. Software for Auto-Zeroed Differential A/D

5.3 Multiple A/D Converters in a Z-80® Interrupt Driven Mode (Continued)

The following notes apply:

1) It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU in interrupt mode). Hence, the subroutine starting address of X003B.

2) The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.

3) A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X E230.

4) The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.

5) The peripherals of concern are mapped into I/O space with the following port assignments:

<table>
<thead>
<tr>
<th>HEX PORT ADDRESS</th>
<th>PERIPHERAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>MM74C374 8-bit flip-flop</td>
</tr>
<tr>
<td>01</td>
<td>A/D 1</td>
</tr>
<tr>
<td>02</td>
<td>A/D 3</td>
</tr>
<tr>
<td>03</td>
<td>A/D 4</td>
</tr>
<tr>
<td>04</td>
<td>A/D 5</td>
</tr>
<tr>
<td>05</td>
<td>A/D 6</td>
</tr>
<tr>
<td>06</td>
<td>A/D 7</td>
</tr>
</tbody>
</table>

This port address also serves as the A/D identifying word in the program.
FIGURE 21: Multiple A/Ds with Z-80 Type Microprocessor

<table>
<thead>
<tr>
<th>LOC</th>
<th>OBJ CODE</th>
<th>STATEMENT</th>
<th>COMMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0038</td>
<td>E5</td>
<td>PUSH HL</td>
<td>Save contents of all registers affected by this subroutine.</td>
</tr>
<tr>
<td>0039</td>
<td>C5</td>
<td>PUSH AC</td>
<td>this subroutine.</td>
</tr>
<tr>
<td>003A</td>
<td>F5</td>
<td>PUSH AF</td>
<td>Assumed INT mode earlier set.</td>
</tr>
<tr>
<td>003B</td>
<td>21 00 3F</td>
<td>LD (HL), 0300</td>
<td>Initialize memory pointer where data will be stored.</td>
</tr>
<tr>
<td>003C</td>
<td>80 01</td>
<td>LD C, X01</td>
<td>Register will be port ADDR of A/D converters.</td>
</tr>
<tr>
<td>0040</td>
<td>D300</td>
<td>OUT X00, A</td>
<td>Load peripheral status word into 8-bit latch.</td>
</tr>
<tr>
<td>0042</td>
<td>D400</td>
<td>IN A, X00</td>
<td>Load status word into accumulator.</td>
</tr>
<tr>
<td>0044</td>
<td>47</td>
<td>LD B, A</td>
<td>Save the status word.</td>
</tr>
<tr>
<td>0045</td>
<td>79</td>
<td>TEST 0000</td>
<td>Test to see if the status of all A/D's have been checked. If so, exit subroutine.</td>
</tr>
<tr>
<td>0046</td>
<td>FE 03</td>
<td>CP, X00</td>
<td></td>
</tr>
<tr>
<td>0048</td>
<td>CA 60 00</td>
<td>JPZ, DONE</td>
<td></td>
</tr>
<tr>
<td>0438</td>
<td>78</td>
<td>LD A, B, C</td>
<td></td>
</tr>
<tr>
<td>0440</td>
<td>47</td>
<td>RRA</td>
<td></td>
</tr>
<tr>
<td>0442</td>
<td>DA 5500</td>
<td>JP C, LOAD</td>
<td></td>
</tr>
<tr>
<td>0511</td>
<td>0C</td>
<td>INC C</td>
<td></td>
</tr>
<tr>
<td>0522</td>
<td>C3 4500</td>
<td>JP, TEST</td>
<td></td>
</tr>
<tr>
<td>0556</td>
<td>ED 78</td>
<td>LOAD IN A, (3)</td>
<td></td>
</tr>
<tr>
<td>0577</td>
<td>EF FF</td>
<td>XOR FF</td>
<td></td>
</tr>
<tr>
<td>0587</td>
<td>77</td>
<td>LD (HL), A</td>
<td>Store the data.</td>
</tr>
<tr>
<td>0591</td>
<td>2C</td>
<td>INC L</td>
<td>Store A/D identifier (A/D port ADDR).</td>
</tr>
<tr>
<td>05A8</td>
<td>71</td>
<td>LD (HL), C</td>
<td></td>
</tr>
<tr>
<td>05AC</td>
<td>2C</td>
<td>INC L</td>
<td></td>
</tr>
<tr>
<td>05D0</td>
<td>C3 51 00</td>
<td>JP, NEXT</td>
<td></td>
</tr>
<tr>
<td>0602</td>
<td>F1</td>
<td>DONE</td>
<td>Test next bit in status word.</td>
</tr>
<tr>
<td>0621</td>
<td>C1</td>
<td>POP AF</td>
<td>Re-establish all registers as they were before the interrupt.</td>
</tr>
<tr>
<td>0622</td>
<td>E1</td>
<td>POP HL</td>
<td></td>
</tr>
<tr>
<td>0639</td>
<td>C9</td>
<td>RET</td>
<td>Return to original program.</td>
</tr>
</tbody>
</table>
Connection Diagrams

ADCO80X
Dual-In-Line and Small Outline (SO) Packages

<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CS</td>
</tr>
<tr>
<td>2</td>
<td>E4</td>
</tr>
<tr>
<td>3</td>
<td>E5</td>
</tr>
<tr>
<td>4</td>
<td>E6</td>
</tr>
<tr>
<td>5</td>
<td>VDD</td>
</tr>
<tr>
<td>6</td>
<td>VSS</td>
</tr>
<tr>
<td>7</td>
<td>AGND</td>
</tr>
<tr>
<td>8</td>
<td>VREF+/2</td>
</tr>
<tr>
<td>9</td>
<td>D4H</td>
</tr>
<tr>
<td>10</td>
<td>D4L</td>
</tr>
</tbody>
</table>

ADC080X
Molded Chip Carrier (PCC) Package

<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CS</td>
</tr>
<tr>
<td>2</td>
<td>E4</td>
</tr>
<tr>
<td>3</td>
<td>E5</td>
</tr>
<tr>
<td>4</td>
<td>E6</td>
</tr>
<tr>
<td>5</td>
<td>VDD</td>
</tr>
<tr>
<td>6</td>
<td>VSS</td>
</tr>
<tr>
<td>7</td>
<td>AGND</td>
</tr>
<tr>
<td>8</td>
<td>VREF+/2</td>
</tr>
</tbody>
</table>

See Ordering Information
LAMPIRAN B
;--------
; Constants
;--------

;----------------------
; Memory Allocation
;----------------------

Timer_Status EQU 30h ; status utk timer 0
Sec_Tick EQU 31h ; 0 -> dipakai untuk delay geser pada header
X_Header EQU 32h ; 1 -> untuk menghitung lebar pulsa data infrared
J_Header EQU 33h ; variabel utk counter timer
Mode EQU 32h ; variabel yg menunjukkan mode yg ditampilkan pada LCD
X_Enter_SP EQU 33h ; mode 1 = menampilkan nilai SP dan PV
SP EQU 34h ; mode 2 = menampilkan status kran
Set_Point EQU 35h ; mode 3 = input nilai SP dari keypad
BUFFER_SP EQU 36h ; mode 4 = Verifikasi pembukaan kran isi
; mode 5 = Verifikasi penutupan kran isi
; mode 6 = Verifikasi pembukaan kran buang
; mode 7 = Verifikasi penutupan kran buang
; mode 8 = pesan error bila SP yg dimasukkan > 100
; mode 9 = menampilkan level air dan status heater
; mode 10= pesan error apabila membuka kran isi padahal
; air sudah penuh
Tank_Status EQU 39h ; variabel koordinat X posisi kursor saat menginputkan
Data.Counter EQU 3Ah ; variabel untuk menampilkan 3 digit nilai
from kontroler 1
Ctrl_Status EQU 3Bh ; variabel counter jumlah pulsa data yg akan
dikirim ke kontroler 1
Count EQU 3Ch ; variabel penampung nilai kontrol status
Set_Ctrl_St EQU 3Dh ; variabel yang menampung nilai kontrol status yg akan
dikirimkan ke kontroler 1

;----------------------
; Bit Addressable
;----------------------

LCD_RS BIT p3.6 ; pin output untuk register select LCD
LCD_CS BIT p3.7 ; pin output enable LCD
Scan_Key_1 BIT p2.6 ;
Scan_Key_2 BIT p2.5 ; pin output pembacaan matrix keypad
Scan_Key_3 BIT p2.4 ;
Scan_Key_4 BIT p2.3 ;
IR_TX BIT p3.4 ; pin output transmitter IR
IR_RX BIT p3.2 ; pin input receiver IR

;---------------------
; Flag / Indicator
;---------------------

Button_F BIT 00h ; 0 -> idle, 1 -> lakukan pembacaan tombol
Header_F BIT 01h ; 0 -> idle, 1 -> refresh tampilan header pada LCD
Show_Header_F BIT 02h ; 0 -> header tdk ditampilkan, 1 -> header ditampilkan
Upper_Valve BIT 03h ; 0 -> close, 1 -> open
Lower_Valve BIT 04h ; 0 -> close, 1 -> open
Upper_Valve_C BIT 05h ; 0 -> close, 1 -> open
Lower_Valve_C BIT 06h ; 0 -> close, 1 -> open
Heater BIT 07h ; 0 -> stop, 1 -> active
Update_Mode_F BIT 08h ; 0 -> idle, 1 -> refresh tampilan pada LCD
Data_Type_F BIT 09h ; 0 -> data PV, 1 -> data kontrol status
Send_Data_F BIT 0Ah ; data yg akan dikirim : 0 -> data SP, 1 -> data kontrol status
No_Data_F BIT 0Bh ; 0 -> masih ada data yg diterima, 1 -> tidak ada data yg masuk

;---------------------
; Program Reset
;---------------------

ORG 0000h
LJMP Start

ORG 0003h ; vector address untuk interrupt 0
LJMP Int_0

ORG 000Bh ; vector address untuk timer 0
LJMP Timer_0

ORG 001Bh ; vector address untuk timer 1
LJMP Timer_1

;---------------------
; ROM Database
;---------------------

; ini adalah data karakter-karakter yang akan ditampilkan pada LCD
; untuk tiap-tiap mode

Header   DB 149
          DB ' ALAT PEMANTAU DAN PENGENDALI SUHU AIR '
          DB ' IR TANPA KABEL BERBASIS uC89C51 - Hartono Rahardjo'
          DB ' - NRP. 5103094049 - Unika WIDYA MANDALA Surabaya '
          DB '
Opened   DB 'buka '
Closed    DB 'tutup'
; Y_or_N
 DB '*Y #=N'

; Active
 DB 'aktif'

; Stop
 DB 'stop '

; Full
 DB 'penuh '

; Not_Full
 DB 'terisi'

; Empty
 DB 'kosong'

; Status_1_Text
 DB 'PV = '
 DB 'SP = '

; Status_2_Text
 DB 'Kran isi :
 DB 'Kran buang:'

; Status_3_Text
 DB 'SP (',0DFh,','C) = '

; Status_4_Text
 DB 'Buka kran isi ? '

; Status_5_Text
 DB 'Tutup kran isi ?'

; Status_6_Text
 DB 'Buka kran buang?'

; Status_7_Text
 DB 'Ttp kran buang? '

; Status_8_Text
 DB 'SP > 100 !!!!'
 DB 'Tekan #'

; Status_9_Text
 DB 'Vol. air: '
 DB 'Heater : '

; Status_10_Text
 DB 'Air sudah penuh.'
 DB 'Tekan # '

;-----------------------------
; Interrupt Service Routine
;-----------------------------

; Interrupt timer 0 digunakan untuk:
; 1. menghitung pewaktuan 0.5 detik, setiap 0.5 dtk tampilan pada header
   bergeser
; 2. menghitung pewaktuan 4 detik, kalau tidak ada data yg diterima maka
   tampilkan
tulisan --- pada LCD

Timer_0

PUSH a
PUSH psw
MOV th0,#03Ch
MOV t10,#0AFh
INC Sec_Tick
MOV a,Timer_Status
CJNE a,#0,T0_J2
MOV a,Sec_Tick
CJNE a,#10,T0_J1
MOV Sec_Tick,#0
SETB Header_F
AJMP T0_J1

T0_J3 JNC T0_J4
AJMP T0_J1

T0_J2 MOV a,Sec_Tick
CJNE a,#60,T0_J3
T0_J4 MOV Sec_Tick,#0
MOV Present_Value,#0FFh
SETB No_Data_F
SETB Update_Mode_F
; CLR tr0
; CLR et0
T0_J1 POP psw
POP a
RETI

; Interrupt 0 digunakan untuk menerima dan menghitung pulsa data
; yang diterima dari receiver IR

Int_0

CLR ea
CLR et0
PUSH a
PUSH psw
MOV Data.Counter,#0
MOV th0,#0
MOV t10,#0
SETB tr0
JNB IR_RX,§
CLR tr0
MOV a,th0
CJNE a,#7,I0_J2
CLR Data.Type_F
AJMP I0_J5
I0_J2 CJNE a,#9,I0_J1
SETB Data.Type_F
I0_J5 MOV th0,#0E0h
MOV t10,#0
CLR tf0
SETB tr0
I0_J3 JB tf0,I0_J4
JB IR_RX,I0_J3
JNB IR_RX, $  
INC Data_Counter  
AJMP I0_J5  

I0_J4 DEC Data_Counter  
MOV a, Mode  
CJNE a, #1, I0_J7  

I0_J8 SETB Update_Mode_F  
AJMP I0_J9  

I0_J7 CJNE a, #2, I0_J10 ; cek apakah data yang masuk = PV?  
AJMP I0_J8  

I0_J10 CJNE a, #9, I0_J9 ; cek apakah data yang masuk = status kontrol?  
AJMP I0_J8  

I0_J9 CLR tf0  
CLR tr0  
JB Data_Type_F, I0_J6  
MOV Present_Value, Data_Counter  
AJMP I0_J11  

I0_J6 MOV Ctrl_Status, Data_Counter  

I0_J11 CLR No_Data_F  
MOV th0, #03Ch  
MOV t10, #0AFh  
MOV Sec_Tick, #0  

I0_J1  
SETB et0  
SETB tr0  
CLR ie0  
POP psw  
POP a  
SETB ea  
RETI  

; timer 1 digunakan untuk membangkitkan frekuensi 40 kHz (carrier)  

Timer_1  
CPL IR_TX  
RETI  

; Procedures  

; digunakan untuk menghasilkan delay kurang lebih 50 us (digunakan untuk penulisan data pada LCD)  

Delay_50  
PUSH 7  
MOV r7, #50 ; Delay 50 us  
DJNZ r7, $  
POP 7  
RETI  

; digunakan untuk menghasilkan delay kurang lebih 4 ms (digunakan untuk
; penulisan instruksi pada LCD

Delay_2
    PUSH 7
    PUSH 6
    MOV r7,#0
D_2_J1  MOV r6,#0Eh
    DJNZ r6,\$
    DJNZ r7,D_2_J1
    POP 6
    POP 7
    RET

; prosedur penulisan instruksi pada LCD

LCD_Write_Inst
    CLR LCD_RS
    SETB LCD_CS
    MOV pl,a
    CLR LCD_CS
    LCALL Delay_2
    RET

; prosedur penulisan data pada LCD

LCD_Write_Data
    SETB LCD_RS
    SETB LCD_CS
    MOV pl,a
    CLR LCD_CS
    LCALL Delay_50
    RET

; prosedur inisialisasi LCD

Initialize_LCD
    MOV r7,#5
I_L_J1   LCALL Delay_2
    DJNZ r7,I_L_J1
    MOV a,#03Fh
    LCALL LCD_Write.Inst
    LCALL LCD_Write.Inst
    LCALL LCD_Write.Inst
    MOV a,#0Eh
    LCALL LCD_Write.Inst
    MOV a,#06h
    LCALL LCD_Write.Inst
    MOV a,#01h
    LCALL LCD_Write.Inst
    MOV a,#0Ch
    LCALL LCD_Write.Inst
    RET

; Ini adalah prosedur untuk setting timer, interrupt, dan nilai awal variabel

Initialize_Data
    MOV tmmod,#21h ; timer 0 -> timer 16 bit, timer 1 -> timer auto reload
MOV th0, #03Ch ; timer 0 digunakan utk pewaktuan 50.000 us
MOV tl0, #0AFh

MOV th1, #0F4h ; timer 1 digunakan utk pewaktuan 25 us (periode dari 40 kHz)
MOV tl1, #0F4h

MOV ie, #82h ; aktifkan int. timer 0

CLR Button_F
SETB Header_F
SETB Show_Header_F
SETB No_Data_F
MOV X_Header, #0
MOV Sec_Tick, #0
MOV Timer_Status, #0
MOV Set_Point, #OFFh
MOV Present_Value, #OFFh
MOV Buffer_SP, #0
MOV Buffer_SP+1, #0
MOV Buffer_SP+2, #0
CLR Upper_Valve
CLR Lower_Valve
CLR Heater
SETB IR_TX
MOV Tank_Status, #0

MOV dptr, #Header
CLR a
MOVC a, @a+ dptr
MOV J_Header, a
SETB tr0
RET

; prosedur untuk menampilkan tulisan header pada LCD

Show_Header
JNB Header_F, H_J1
CLR Header_F
MOV a, #080h
LCALL LCD_Write_Inst
MOV dptr, #Header
INC dptr
MOV r7, #16

H_J2
MOV a, X_Header
MOVC a, @a+dptr
LCALL LCD_Write_Data
INC dptr
DJNZ r7, H_J2
INC X_Header
MOV a, X_Header
CJNE a, J_Header, H_J1
MOV X_Header, #0

H_J1 RET
; prosedur delay untuk menghilangkan bouncing saat tombol ditekan

Remove_Bouncing

    MOV r4, #0FFh
    RB_J1 MOV r3, #00Fh
    DJNZ r3, $;
    DJNZ r4, RB_J1
    RET

; prosedur pengecekan tombol

Check_Button

    MOV r7, #1
    CLR Scan_1
    SETB Scan_2
    SETB Scan_3
    SETB Scan_4
    MOV a, p2
    ANL a, #7h
    CJNE a, #7h, CB_J2
    MOV r7, #4
    SETB Scan_1
    CLR Scan_2
    SETB Scan_3
    SETB Scan_4
    MOV a, p2
    ANL a, #7h
    CJNE a, #7h, CB_J2
    MOV r7, #7
    SETB Scan_1
    SETB Scan_2
    CLR Scan_3
    SETB Scan_4
    MOV a, p2
    ANL a, #7h
    CJNE a, #7h, CB_J2
    MOV r7, #10
    SETB Scan_1
    SETB Scan_2
    SETB Scan_3
    CLR Scan_4
    MOV a, p2
    ANL a, #7h
    CJNE a, #7h, CB_J2
    CLR Button_F
    CB_J1 RET

CB_J2 JB Button_F, CB_J1
SETB Button_F
LCALL Remove_Bouncing
JNB Show_Header_F, CB_J3
MOV ie, #089h
SETB it0
MOV Mode, #1
SETB Update_Mode_F
CLR Show_Header_F
CLR tr0
MOV Timer_Status,#1
CLR Header_F
RET
CB_J3 CJNE a,#3,CB_J4
MOV a,#0
AJMP CB_J6
CB_J4 CJNE a,#5,CB_J5
MOV a,#1
AJMP CB_J6
CB_J5 CJNE a,#6,CB_J1
MOV a,#2
CB_J6 MOV b,r7
ADD a,b

; Button 1

CJNE a,#1,CB_J7
MOV a,Mode
CJNE a,#3,Btn1_J1
MOV a,X_Enter_SP
CJNE a,#3,Btn1_J2
RET
Btn1_J2 MOV r0,#Buffer_SP
ADD a,r0
MOV r0,a
MOV @r0,#1
MOV a,#31h
LCALL LCD_Write_Data
INC X_Enter_SP
Btn1_J1 RET

; Button 2

CB_J7 CJNE a,#2,CB_J8
MOV a,Mode
CJNE a,#3,Btn2_J1
MOV a,X_Enter_SP
CJNE a,#3,Btn2_J2
RET
Btn2_J2 MOV r0,#Buffer_SP
ADD a,r0
MOV r0,a
MOV @r0,#2
MOV a,#32h
LCALL LCD_Write_Data
INC X_Enter_SP
Btn2_J1 RET

; Button 3

CB_J8 CJNE a,#3,CB_J9
MOV a,Mode
CJNE a,#3,Btn3_J1
MOV a,X_Enter_SP
CJNE a,#3,Btn3_J2
RET
Btn3_J2 MOV r0,#Buffer_SP
ADD  a, r0
MOV  r0, a
MOV  @r0, #3
MOV  a, #33h
LCALL LCD_Write_Data
INC  X_Enter_SP

Btn3_J1  RET

; Button 4

CB_J9  CJNE  a, #4, CB_J10
MOV  a, Mode
CJNE  a, #3, Btn4_J1
MOV  a, X_Enter_SP
CJNE  a, #3, Btn4_J2
RET

Btn4_J2  MOV  r0, #Buffer_SP
ADD  a, r0
MOV  r0, a
MOV  @r0, #4
MOV  a, #34h
LCALL LCD_Write_Data
INC  X_Enter_SP

Btn4_J1  RET

; Button 5

CB_J10  CJNE  a, #5, CB_J11
MOV  a, Mode
CJNE  a, #3, Btn5_J1
MOV  a, X_Enter_SP
CJNE  a, #3, Btn5_J2
RET

Btn5_J2  MOV  r0, #Buffer_SP
ADD  a, r0
MOV  r0, a
MOV  @r0, #5
MOV  a, #35h
LCALL LCD_Write_Data
INC  X_Enter_SP

Btn5_J1  RET

; Button 6

CB_J11  CJNE  a, #6, CB_J12
MOV  a, Mode
CJNE  a, #3, Btn6_J1
MOV  a, X_Enter_SP
CJNE  a, #3, Btn6_J2
RET

Btn6_J2  MOV  r0, #Buffer_SP
ADD  a, r0
MOV  r0, a
MOV  @r0, #6
MOV  a, #36h
LCALL LCD_Write_Data
INC  X_Enter_SP
BTN6_J1    RET

; Button 7

CB_J12    CJNE    a,#7,CB_J13
         MOV     a,Mode
         CJNE    a,#3,Btn7_J1
         MOV     a,X_Enter_SP
         CJNE    a,#3,Btn7_J2
         RET

BTN7_J2    MOV     r0,#Buffer_SP
ADD     a,r0
MOV     r0,a
MOV     @r0,#7
MOV     a,#37h
LCALL    LCD_Write_Data
INC     X_Enter_SP
BTN7_J1    RET

; Button 8

CB_J13    CJNE    a,#8,CB_J14
         MOV     a,Mode
         CJNE    a,#3,Btn8_J1
         MOV     a,X_Enter_SP
         CJNE    a,#3,Btn8_J2
         RET

BTN8_J2    MOV     r0,#Buffer_SP
ADD     a,r0
MOV     r0,a
MOV     @r0,#8
MOV     a,#38h
LCALL    LCD_Write_Data
INC     X_Enter_SP
BTN8_J1    RET

; Button 9

CB_J14    CJNE    a,#9,CB_J15
         MOV     a,Mode
         CJNE    a,#3,Btn9_J1
         MOV     a,X_Enter_SP
         CJNE    a,#3,Btn9_J2
         RET

BTN9_J2    MOV     r0,#Buffer_SP
ADD     a,r0
MOV     r0,a
MOV     @r0,#9
MOV     a,#39h
LCALL    LCD_Write_Data
INC     X_Enter_SP
BTN9_J1    RET

CB_J19    LJMP    CB_J16

; Button 10
CB_J15      CJNE a, #10, CB_J19
     MOV a, Mode
     CJNE a, #1, Bt10_J1
     MOV Mode, #2
     SETB Update_Mode_F
     RET
Bt10_J1     CJNE a, #2, Bt10_J2
     MOV Mode, #9
     SETB Update_Mode_F
     RET
Bt10_J2     CJNE a, #3, Bt10_J3
     MOV a, X_Enter_SP
     CJNE a, #0, Bt10_J4
     RET
Bt10_J4     MOV a, #10h
     LCALL LCD_Write_Inst
     MOV a, #20h
     LCALL LCD_Write_Data
     MOV a, #10h
     LCALL LCD_Write_Inst
     DEC X_Enter_SP
     RET
Bt10_J3     CJNE a, #4, Bt10_J5
     MOV a, Tank_Status
     CJNE a, #3, B10_J10
     MOV Mode, #10
     SETB Update_Mode_F
     RET
B10_J10     SETB Upper_Valve_C

     LCALL Turn_Upper_Valve
     SETB Send_Data_F
     LCALL Send_Data

     MOV Mode, #2
     SETB Update_Mode_F
     RET
Bt10_J5     CJNE a, #5, Bt10_J6
     CLR Upper_Valve_C

     LCALL Turn_Upper_Valve
     SETB Send_Data_F
     LCALL Send_Data

     MOV Mode, #2
     SETB Update_Mode_F
     RET
Bt10_J6     CJNE a, #6, Bt10_J7

     SETB Lower_Valve_C

     LCALL Turn_Lower_Valve
     SETB Send_Data_F
     LCALL Send_Data

     MOV Mode, #2
SETB Update_Mode_F
RET

Bt10_J7 CJNE a,#7,Bt10_J8
CLR Lower_Valve_C

LCALL Turn_Lower_Valve
SETB Send_Data_F
LCALL Send_Data

MOV Mode,#2
SETB Update_Mode_F
RET

Bt10_J8 CJNE a,#9,Bt10_J9
MOV Mode,#1
SETB Update_Mode_F
RET

Bt10_J9 RET

; Button 11

CB_J16 CJNE a,#11,CB_J17
MOV a,Mode
CJNE a,#3,Bt11_J1
MOV a,X_Enter_SP
CJNE a,#3,Bt11_J2
RET

Bt11_J2 MOV r0,#Buffer_SP
ADD a,r0
MOV r0,a
MOV @r0,#0
MOV a,#30h
LCALL LCD_Write_Data
INC X_Enter_SP
RET

Bt11_J1 CJNE a,#2,Bt11_J3
JNB No_Data_F,Bt11_J5
RET

Bt11_J5 MOV Mode,#4
SETB Update_Mode_F
JNB Upper_Valve,Bt11_J4
MOV Mode,#5
Bt11_J4 RET

Bt11_J3 RET

; Button 12

CB_J17 CJNE a,#12,CB_J18
MOV a,Mode
CJNE a,#1,Bt12_J1
JNB No_Data_F,Bt12_J6
RET

B12_J16 MOV Mode,#3
SETB Update_Mode_F
RET
Bt12_J1  CJNE  a,#3,Bt12_J2
       LCALL  Calculate_SP
       MOV  a,#0Ch
       LCALL  LCD_Write_Inst
       MOV  a,r6
       CJNE  a,#100,Bt12_J3
       AJMP  Bt12_J4
Bt12_J3  JC  Bt12_J4
       CJNE  a,#OFFh,Bt12_J7
       AJMP  Bt12_J6
Bt12_J7  SETB  Mode,#8
       RET
Bt12_J4  MOV  Set_Point,r6'
       CLR  Send_Data_F
       LCALL  Send_Data
Bt12_J6  MOV  Mode,#1
       SETB  Update_Mode_F
       RET
Bt12_J2  CJNE  a,#8,Bt12_J5
       AJMP  Bt12_J6
Bt12_J5  CJNE  a,#2,Bt12_J8
       JNB  No_Data_F,Bt12_J7
       RET
B12_J7  MOV  Mode,#6
       SETB  Update_Mode_F
       JNB  Lower_Valve,Bt12_J9
       MOV  Mode,#7
       RET
Bt12_J9  RET
Bt12_J8  CJNE  a,#4,B12_J10
B12_J10  MOV  Mode,#2
       SETB  Update_Mode_F
       RET
B12_J14  CJNE  a,#5,B12_J11
       AJMP  B12_J14
B12_J11  CJNE  a,#6,B12_J12
       AJMP  B12_J14
B12_J12  CJNE  a,#7,B12_J13
       AJMP  B12_J14
B12_J13  CJNE  a,#10,B12_J15
       AJMP  B12_J14
B12_J15  RET
CB_J18  RET

; prosedur untuk menghitung SP dalam hexadesimal dari nilai SP yang diinputkan melalui keypad

Calculate_SP
       MOV  r6,#0
MOV r7, X_Enter_SP
MOV r0, #Buffer_SP
MOV a, r7
CJNE a, #0, CSP_J3
MOV r6, Set_Point
MOV a, b
ADD a, #30h
LCALL LCD_Write_Data

CHD_J2 MOV a, #020h
LCALL LCD_Write_Data
MOV a, #0DFh
LCALL LCD_Write_Data
MOV a, #043h
LCALL LCD_Write_Data
RET

Mode_4_to_7
MOV r7, #16
Md47_J1 CLR a
MOVC a, @a + dpdr
LCALL LCD_Write_Data
INC dpdr
DJNZ r7, Md47_J1
MOV dpdr, #Y_or_N
MOV a, #0C0h
LCALL LCD_Write.Inst
MOV r7, #7
Md47_J2 CLR a
MOVC a, @a + dpdr
LCALL LCD_Write_Data
INC dpdr
DJNZ r7, Md47_J2
RET

; prosedur untuk menampilkan tulisan untuk setiap mode pada LCD

Update_Mode
JB Update_Mode_F, UM_J1
RET

UM_J1 CLR Update_Mode_F
MOV a, #1
LCALL LCD_Write.Inst
MOV a, Mode

; Mode 1

CJNE a, #1, UM_J2
MOV dpdr, #Status_1_Text
MOV r7, #5
Md1_J1 CLR a
MOVC a, @a + dpdr
LCALL LCD_Write_Data
INC dpdr
DJNZ r7, Md1_J1
MOV a, Present_Value
LCALL Calculate_Hex_2_Dec
MOV a, #0C0h
LCALL LCD_Write.Inst
MOV r7, #5
Md1_J2 CLR a
MOVC a, @a + dpdr
LCALL LCD_Write_Data
INC dptr
DJNZ r7, Md1_J2
MOV a, Set_Point
LCALL Calculate_Hex_2_Dec
RET

; Mode 2
UM_J2 CJNE a, #2, UM_J3
LCALL Check_Ctrl_Status
MOV dptr, #Status_2_Text
MOV r7, #11
Md2_J1 CLR a
MOVC a, @a+dptr
LCALL LCD_Write_Data
INC dptr
DJNZ r7, Md2_J1
PUSH dpl
PUSH dph
JNB No_Data_F, Md2_J7
MOV a, #020h
LCALL LCD_Write_Data
MOV a, #02Dh
LCALL LCD_Write_Data
MOV a, #02Dh
LCALL LCD_Write_Data
MOV a, #02Dh
LCALL LCD_Write_Data
AJMP Md2_J8
Md2_J7 MOV dptr, #Closed
JNB Upper_Valve, Md2_J3
MOV dptr, #Opened
Md2_J3 MOV r7, #5
Md2_J4 CLR a
MOVC a, @a+dptr
LCALL LCD_Write_Data
INC dptr
DJNZ r7, Md2_J4
Md2_J8 POP dph
POP dpl
LCALL LCD_Write_Inst
MOV r7, #11
Md2_J2 CLR a
MOVC a, @a+dptr
LCALL LCD_Write_Data
INC dptr
DJNZ r7, Md2_J2
JNB No_Data_F, Md2_J9
MOV a, #020h
LCALL LCD_Write_Data
MOV a, #02Dh
LCALL LCD_Write_Data
MOV a, #02Dh
LCALL LCD_Write_Data
MOV a, #02Dh
LCALL LCD_Write_Data
RET

; Mode 3
UM_J3 CJNE a, #3, UM_J4
MOV dptr, #Status_3_Text
MOV r7, #10
Md3_J1 CLR a
MOV a, @a + dptr
LCALL LCD_Write_Data
INC dptr
DJNZ r7, Md3_J1
MOV a, #0Eh
LCALL LCD_Write_Data
MOV X_Enter_SP, #0
RET

; Mode 4
UM_J4 CJNE a, #4, UM_J5
MOV dptr, #Status_4_Text
LCALL Mode_4_to_7
RET

; Mode 5
UM_J5 CJNE a, #5, UM_J6
MOV dptr, #Status_5_Text
LCALL Mode_4_to_7
RET

; Mode 6
UM_J6 CJNE a, #6, UM_J7
MOV dptr, #Status_6_Text
LCALL Mode_4_to_7
RET

; Mode 7
UM_J7 CJNE a, #7, UM_J8
MOV dptr, #Status_7_Text
LCALL Mode_4_to_7
RET
; Mode 8

UM_J8 CJNE a,#8,UM_J9
    MOV r7,#12
    MOV dptr,#Status_8_Text

Md8_J1 CLR a
    MOV a,@a+dptr
    LCALL LCD_Write_Data
    INC dptr
    DJNZ r7,Md8_J1
    MOV a,#0C0h
    LCALL LCD_Write_Init
    MOV r7,#7

Md8_J2 CLR a
    MOV a,@a+dptr
    LCALL LCD_Write_Data
    INC dptr
    DJNZ r7,Md8_J2
    RET

UM_J9 CJNE a,#9,UM_J10
    LCALL Check_CTRL_Status
    MOV r7,#10
    MOV dptr,#Status_9_Text

Md9_J1 CLR a
    MOV a,@a+dptr
    LCALL LCD_Write_Data
    INC dptr
    DJNZ r7,Md9_J1
    PUSH dpl
    PUSH dph
    JNB No_Data_F,Md9_J8
    MOV a,#02Dh
    LCALL LCD_Write_Data
    MOV a,#02Dh
    LCALL LCD_Write_Data
    MOV a,#02Dh
    LCALL LCD_Write_Data
    AJMP Md9_J9

Md9_J8 MOV dptr,#Full
    MOV a,Tank_Status
    CJNE a,#0,Md9_J3
    MOV dptr,#Empty
    AJMP Md9_J4

Md9_J3 CJNE a,#1,Md9_J4
    MOV dptr,#Not_Full

Md9_J4 MOV r7,#6

Md9_J5 CLR a
    MOV a,@a+dptr
    LCALL LCD_Write_Data
    INC dptr
    DJNZ r7,Md9_J5

Md9_J9 POP dph
    POP dpl
MOV a,#0COh
LCALL LCD_Write_Init
MOV r7,#10

Md9_J2
CLR a
MOVC a,@a+dptr
LCALL LCD_Write_Data
INC dptr
DJNZ r7,Md9_J2
JNB No_Data_F,Md9_J10
MOV a,#02Dh
LCALL LCD_Write_Data
MOV a,#02Dh
LCALL LCD_Write_Data
MOV a,#02Dh
LCALL LCD_Write_Data
RET

Md9_J10
MOV dptr,#Active
J0 Heater,Md9_J6
MOV dptr,#Stop
Md9_J6
MOV r7,#5
Md9_J7
CLR a
MOVC a,@a+dptr
LCALL LCD_Write_Data
INC dptr
DJNZ r7,Md9_J7
RET

UM_J10
CJNE a,#10,UM_J11
MOV r7,#16
MOV dptr,#Status_10_Text
Md10_J1
CLR a
MOVC a,@a+dptr
LCALL LCD_Write_Data
INC dptr
DJNZ r7,Md10_J1
MOV a,#0COh
LCALL LCD_Write_Init
MOV r7,#7
Md10_J2
CLR a
MOVC a,@a+dptr
LCALL LCD_Write_Data
INC dptr
DJNZ r7,Md10_J2
RET
UM_J11
RET

; prosedur untuk mengirimkan data pada kontroler 1

Send_Data
CLR ex0
CLR et0
SETB et1
MOV r7,#2    ; !!!!

SD_J4 JB Send_Data_F,SD_J1
MOV Counter, Set_Point
MOV th0, #0F5h
MOV tl0, #041h
SETB tr0
SETB tr1
JNB tf0, $ CLR tr1
SETB IR_TX
LJMP SD_J2

SD_J1 MOV Counter, Set_Ctrl_St
MOV th0, #0F3h
MOV tl0, #07Fh
SETB tr0
SETB tr1
JNB tf0, $ CLR tr1
SETB IR_TX

SD_J2 CLR tr0
CLR tf0
INC Counter

SD_J3 MOV th0, #0FDh
MOV tl0, #0A7h
SETB tr0
JNB tf0, $ CLR tf0
MOV th0, #0FDh
MOV tl0, #0A7h
SETB tr1
JNB tf0, $ CLR tr0
CLR tr1
CLR tr1
CLR tf0
DJNZ Counter, SD_J3

MOV th0, #0C0h ; !!!
MOV tl0, #000h
SETB tr0
JNB tf0, $ CLR tf0
CLR tf0
DJNZ r7, SD_J4

CLR et1
CLR ie0
SETB ex0
RET

; prosedur untuk meng update nilai kontrol status yg akan dikirimkan
; (membuka / menutup kran isi)

Turn_Upper_Valve
MOV Set_Ctrl_St, Ctrl_Status
ANL Set_Ctrl_St, #3
JB Upper_Valve_C, TUV_J1
ANL Set_Ctrl_St, #0FEh
RET
; prosedur untuk meng update nilai kontrol status yg akan dikirimkan
; (membuka / menutup kran buang)

Turn_Lower_Valve
MOV Set_Ctrl_St, Ctrl_Status
ANL Set_Ctrl_St, #3
JB Lower_Valve_C, TLV_J1
ANL Set_Ctrl_St, #0FDh
RET

TLV_J1 ORL Set_Ctrl_St, #2
RET

; prosedur untuk pembacaan nilai data kontrol status yang diterima dari
; kontroler 1, untuk ditampilkan pada LCD

Check_Ctrl_Status
MOV a, Ctrl_Status
ANL a, #1
CLR Upper_Valve
CJNE a, #1, CCS_J1
SETB Upper_Valve

CCS_J1 MOV a, Ctrl_Status
ANL a, #2
CLR Lower_Valve
CJNE a, #2, CCS_J2
SETB Lower_Valve

CCS_J2 MOV a, Ctrl_Status
ANL a, #0Ch
RR a
RR a
MOV Tank_Status, a
CJNE a, #0, CCS_J4
MOV Set_Point, #0FFh

CCS_J4 MOV a, Ctrl_Status
ANL a, #10h
CLR Heater
MOV Set_Point, #0FFh
CJNE a, #10h, CCS_J3
SETB Heater

CCS_J3 RET

;-----------
; Main Program
;-----------

Start
MOV sp, #7
LCALL Initialize_LCD
LCALL Initialize_Data

Loop LCALL Show_Header
LCALL Check_Button
LCALL Update_Mode
LJMP Loop
;---------------------
; Constants
;---------------------

; Memory Allocation
;---------------------

Num_Lo EQU 30h
Num_Hl EQU 31h
Div_0 EQU 32h
Div_1 EQU 33h
Div_2 EQU 34h
Div_3 EQU 35h
Tmp_0 EQU 36h
Tmp_1 EQU 37h ; Num_Lo s/d Tmp_3 adalah variabel
Tmp_2 EQU 38h ; untuk perhitungan aritmatika
Tmp_3 EQU 39h ;

Present_Value EQU 3Ah ; variabel utk menyimpan nilai PV (suhu sekarang)
Sec_Tick EQU 3Bh ; variabel utk counter timer

Ctrl_Status EQU 3Ch ; 0000 0000b
; \ 333 /
; 'U' Upper valve : 0 -> close, 1 -> open
; 'L' Lower Valve : 0 -> close, 1 -> open
; 'W' Water level : 00 -> kosong, 01 -> terisi, 11 ->

penuh ; Heater status : 0 -> stop, 1 -> aktif

Timer_Reg EQU 3Dh ; variabel counter utk menghitung jml pulsa data yang akan dikirim
Tank_Status EQU 3Eh ; Status level air : 0 -> kosong, 1 -> terisi, 2 ->
Penuh

Dummy EQU 3Fh ; variabel penampung sementara, serba guna
Set_Point EQU 40h ; variabel utk menyimpan nilai set point dari kontroler 2
Data_Counter EQU 41h ; variabel counter utk menghitung jml pulsa data yang diterima dari kontroler 2

Dummy_2 EQU 42h ; variabel penampung sementara, serba guna

;---------------------
; Bit Addressable
;---------------------

SOC BIT p3.1 ; pin pengontrol ADC start konversi: 0 -> reset, 1 ->
start konversi
EOC BIT p3.2 ; pin flag/indikator dari ADC bahwa ADC telah selesai
mengkonversi: 1 -> belum selesai, 0 -> sudah selesai
IR_RX BIT p3.3 ; pin input dari receiver infrared: 0 -> ada data, 1 ->
no data
IR_TX BIT p2.4 ; pin output untuk transmitter infrared: 0 -> on, 1 ->
off
Heater BIT p2.5 ; pin output relay heater: 0 -> off, 1 -> on

U_Valve_1 BIT p2.0 ; pin output driver motor utk kran isi (#1)
U_Valve_2 BIT p2.1 ; pin output driver motor utk kran isi (#2)
; #1 = 1, #2 = 1 : stop motor
; #1 = 0, #2 = 1 : motor putar ke kiri
; #1 = 1, #2 = 0 : motor putar ke kanan

L_Valve_1 BIT p2.2 ; pin output driver motor utk kran buang (#1)
L_Valve_2 BIT p2.3 ; pin output driver motor utk kran buang (#2)
; #1 = 1, #2 = 1 : stop motor
; #1 = 0, #2 = 1 : motor putar ke kiri
; #1 = 1, #2 = 0 : motor putar ke kanan

U_Level BIT p3.4 ; pin input dari sensor level air (atas): 0 -> tdk
; ada air, 1 -> ada air
U_Level BIT p3.5 ; pin input dari sensor level air (bawah): 0 ->
tdk ada air, 1 -> ada air

;-----------------------
; Flag / Indicator
;-----------------------

Send_Data_F BIT 00h ; 0 -> idle, 1 -> kirim data
Read_ADC_F BIT 01h ; 0 -> idle, 1 -> baca ADC
Upper_Valve BIT 03h ; 0 -> close, 1 -> open
Lower_Valve BIT 04h ; 0 -> close, 1 -> open
Heater_Status BIT 05h ; 0 -> stop, 1 -> active
Heater_F BIT 06h ; 0 -> idle, 1 -> kontroler heater aktif
Data_Type_F BIT 07h ; 0 -> data SP, 1 -> data status kontrol
Check_Ctrl_F BIT 08h ; 0 -> idle, 1 -> cek kontrol

;-----------------------
; Program Reset
;-----------------------

ORG 0000h
LJMP Start

ORG 0008h
LJMP Timer_0

ORG 0013h
LJMP Int_1

ORG 001Bh
LJMP Timer_1

;-----------------------
; Interrupt Service Routine
;-----------------------

; Timer 0 digunakan untuk menghitung 0.5 detik.
; Tiap 0.5 detik kontroler mengirim data PV, 0.5 detik berikutnya
; kontroler mengirim data status kontrol (heater, water level, status kran),
; 0.5 detik kemudian mengirim data PV lagi, dan seterusnya.

Timer_0

PUSH a
PUSH psw
MOV th0,#03Ch ; nilai th0 dan t10 ini akan menghasilkan
MOV t10,#0AFh  ; penghitungan waktu utk 50.000 us
SETB Read_ADC_F  ; pengkonversian / pembacaan ADC diaktifkan
INC Sec_Tick  ; counter untuk 50.000 us
MOV a,Sec_Tick  ; apakah sudah terjadi penghitungan waktu
CJNE a,#10,T0_J1  ; sebanyak 10 x 50.000 us = 500.000 us =
                   ; 500 ms = 0.5 detik ?
SETB Heater_F  ; lakukan pengecekan / pengontrolan heater
CLR ex1
MOV Sec_Tick,#0
CLR et0
CPL Send_Data_F
JB Send_Data_F,T0_J2
MOV Timer_Reg,Present_Value
MOV th0,#0F9h  ; timer 0 digunakan utk menghasilkan
MOV t10,#0BDh  ; pewaktuan 1100 us (header data PV)
SETB trl
JNB tf0,${}T0_J2
CLR trl
SETB IR_TX
AJMP T0_J3
T0_J2 MOV Timer_Reg,Ctrl_Status
MOV th0,#0F7h  ; timer 0 digunakan utk menghasilkan
MOV t10,#067h  ; pewaktuan 1650 us (header data status kontrol)
SETB trl
JNB tf0,${}T0_J3
CLR trl
SETB IR_TX
T0_J3 CLR tr0
CLR tf0
INC Timer_Reg
T0_J4 MOV th0,#0FDh
MOV t10,#0A7h
SETB tr0
JNB tf0,${}T0_J4
CLR tf0
MOV th0,#0FDh
MOV t10,#0A7h
SETB tr1
JNB tf0,${}T0_J4
CLR tf0
DJNZ Timer_Reg,T0_J4
MOV th0,#03Ch
MOV t10,#0AFh
SETB tr0
SETB et0
interrupt 1 digunakan untuk menerima input data dan menghitung data yang masuk dari receiver infrared

```assembly
T0_J1 POP psw
POP a

; CLR iel
SETB ex1
RETI

; cek apakah data yg masuk = SP ?
CLR ea
PUSH a
PUSH psw
PUSH t10
PUSH th0
MOV Data_Counter, #0
MOV th0, #0
MOV t10, #0
SETB tr0
JNB IR_RX, $
CLR tr0
MOV a, th0
CJNE a, #0Bh, I1_J2
CLR Data_Type_F
AJMP I1_J5
I1_J2 CJNE a, #0Dh, I1_J1

; cek apakah data yg masuk = status kontrol
SETB Data_Type_F
I1_J5 MOV th0, #0E0h
MOV t10, #0
CLR tf0
SETB tr0
I1_J3 JB tf0, I1_J4
JB IR_RX, I1_J3
JNB IR_RX, $
INC Data_Counter
AJMP I1_J5
I1_J4 DEC Data_Counter
CLR tf0
CLR tr0
JB Data_Type_F, I1_J6
MOV Set_Point, Data_Counter
SETB Heater_Status
SETB Heater_F
AJMP I1_J1
I1_J6 SETB Check_Ctrl_F
MOV Dummy_2, Data_Counter
I1_J1 CLR iel
POP th0
POP t10
```
POP psw
POP a
SETB ea
SETB tr0
RETI

; timer 1 digunakan untuk membangkitkan frekuensi 40 kHz (carrier)

Timer_1
CPL IR_TX
RETI

; Procedures

; Ini adalah prosedur untuk setting timer, interrupt, dan nilai awal variabel

Initialize_Data
MOV tmmod,#21h ; timer 0 -> timer 16 bit, timer 1 -> timer auto reload
MOV ie,#8Eh ; aktifkan interrupt 1, int. timer 0, int. timer 1
SETB it1 ; interrupt 1 aktif low edge
MOV ip,#0Ch ; prioritisasikan interrupt 1 dan int. timer 1
MOV th0,#03Ch ; timer 0 digunakan utk pewaktuan 50.000 us
MOV t10,#0AFh
MOV th1,#0F4h ; timer 1 digunakan utk pewaktuan 25 us (periode dari 40 kHz)
MOV t11,#0F4h

MOV Set_Point,#0 ; nilai set point sementara diisi 0
CLR Heater ; matikan heater
CLR Heater_Status ; heater status = mati / off
CLR Upper_Valve ; status kran isi = tutup
CLR Lower_Valve ; status kran buang = tutup

SETB tr0 ; nyalakan timer 0
SETB IR_TX ; matikan transmitter IR
SETB Read_ADC_F ; perintahkan prosedur Read_ADC utk membaca ADC
MOV Ctrl_Status,#0 ; Status kontrol sementara diisi nilai 0
RETI

;-----------------------------------------------
; Div_16 : Routine untuk pembagian
; 32 bit : 16 bit -> 32 bit
;
; MSB       LSB
; Pembagi   -> Num_Hi Num.Lo
; Bilangan  -> Div_3 Div_2 Div_1 Div_0
; Hasil     -> Div_3 Div_2 Div_1 Div_0
;-----------------------------------------------

Div_16:
;This divides the 32 bit OP register by the value supplied
MOV R7, #0 ; zero out partial remainder
MOV R6, #0
MOV Tmp_0, #0
MOV Tmp_1, #0
MOV Tmp_2, #0
MOV Tmp_3, #0
MOV R1, Num_Hi ; load divisor
MOV R0, Num_Lo
MOV R5, #32 ; loop count

;This begins the loop
Div_loop:
ACALL Shift_D ; shift the dividend and return MSB in C
MOV A, R6 ; shift carry into LSB of partial remainder
RLC A
MOV R6, A
MOV A, R7
RLC A
MOV R7, A
JC can_sub ; Revis tgl 20 okt 1998

; now test to see if R7:R6 >= R1:R0
CLR C
MOV A, R7 ; subtract R1 from R7 to see if R1 < R7
SUBB A, R1 ; A = R7 - R1, carry set if R7 < R1
JC Cant_sub

; at this point R7>R1 or R7=R1
JNZ Cant_sub ; jump if R7>R1

;if R7 = R1, test for R6>=R0
CLR C
MOV A, R6
SUBB A, R0 ; A = R6 - R0, carry set if R6 < R0
JC Cant_sub
Can_sub:
; subtract the divisor from the partial remainder
CLR C
MOV A, R6
SUBB A, R0 ; A = R6 - R0
MOV R6, A
MOV A, R7
SUBB A, R1 ; A = R7 - R1 - Borrow
MOV R7, A
SETB C ; shift a 1 into the quotient
AJMP Quot
Can_sub:
; shift a 0 into the quotient
CLR C
Quot:
; shift the carry bit into the quotient
ACALL Shift_Q

; Test for completion
DJNZ R5, Div_loop
; Now we are all done, move the TMP values back into OP
  MOV  Div_0, Tmp_0
  MOV  Div_1, Tmp_1
  MOV  Div_2, Tmp_2
  MOV  Div_3, Tmp_3
  RET

Shift D:
  ; shift the dividend one bit to the left and return the MSB in C
  CLR  C
  MOV  A, Div_0
  RLC  A
  MOV  Div_0, A
  MOV  A, Div_1
  RLC  A
  MOV  Div_1, A
  MOV  A, Div_2
  RLC  A
  MOV  Div_2, A
  MOV  A, Div_3
  RLC  A
  MOV  Div_3, A
  RET

Shift Q:
  ; shift the quotient one bit to the left and shift the C into LSB
  MOV  A, Tmp_0
  RLC  A
  MOV  Tmp_0, A
  MOV  A, Tmp_1
  RLC  A
  MOV  Tmp_1, A
  MOV  A, Tmp_2
  RLC  A
  MOV  Tmp_2, A
  MOV  A, Tmp_3
  RLC  A
  MOV  Tmp_3, A
  RET

; prosedur untuk start konversi dan membaca hasil konversi ADC

Read_ADC
  JNB  Read_ADC_F, RADC_J1; kalau Read_ADC_F = 0, jangan lakukan
    ; pembacaan ADC
  CLR  Read_ADC_F
  CLR  SOC; start konversi
  MOV  r7, #50
  DJNZ  r7, $; 
  SETB  SOC; 
  CLR  ea; matikan semua interrupt
  JB  EOC, $; tunggu sampai selesai konversi
  SETB  ea; nyalakan interrupt
  MOV  a, pl; baca data ADC dari port 1
MOV b, #100 ; data ADC adalah 0 s/d 255,
; untuk mengubahnya menjadi suhu
; digunakan persamaan :
; suhu = -------------------
; 255
MUL ab
MOV Div_0,a
MOV Div_1,b
MOV Div_2,#0
MOV Div_3,#0
MOV Num_Lo,#255
MOV Num_Hi,#0
LCALL Div_1
MOV Present_Value, Div_0
RADC J1 RET

; prosedur untuk mengisi nilai variabel kontrol status yg akan dikirimkan
; ke kontroler 2 dengan melakukan pengecekan sensor level air dan bit-bit
; indicator

Check_Ctrl_Status
MOV Dummy,#0
MOV Tank_Status,#0
JNB L_Level, CCS_J5
MOV Dummy,#4
MOV Tank_Status,#1
JNB U_Level, CCS_J5
MOV Dummy,#12
MOV Tank_Status,#2
CCS_J5
JB Upper_Valve, CCS_J1
ANL Dummy, #0FEh
AJMP CCS_J3
CCS_J1
ORL Dummy, #1
CCS_J3
JB Lower_Valve, CCS_J2
ANL Dummy, #0FDh
AJMP CCS_J4
CCS_J2
ORL Dummy, #2
CCS_J4
JB Heater_Status, CCS_J6
ANL Dummy, #0EFh
AJMP CCS_J7
CCS_J6
ORL Dummy, #10h
CCS_J7
MOV Ctrl_Status, Dummy
RET

; prosedur untuk kontrol heater secara otomatis

Check_Heater
JB Heater_F, CH_J1 ; apakah boleh melakukan kontrol heater ?
RET
CH_J1 CLR Heater_F
JB Heater_Status, CH_J2 ; apakah status heater stop / aktif ?
RET
CH_J2 MOV a, Present_Value
MOV b, Set_Point
; prosedur untuk membuka kran isi

Open_Upper_Valve
CLR ea
CLR tr0
SETB U_Valve_1 ; nyalakan motor
CLR U_Valve_2 ;
MOV r7,#200 ;
OUV_J2 MOV r6,#250 ; Ini adalah delay lama motor
OUV_J1 MOV r5,#20
DJNZ r5,$ ; berputar
DJNZ r6,OUV_J1 ;
DJNZ r7,OUV_J2 ;
SETB U_Valve_1 ; matikan motor
SETB U_Valve_2 ;
CLR iel
SETB tr0
SETB ea
RET

; prosedur untuk menutup kran isi

Close_Upper_Valve
CLR ea
CLR tr0
CLR U_Valve_1 ; nyalakan motor
SETB U_Valve_2 ;
MOV r7,#200 ;
CUV_J2 MOV r6,#250 ; Ini adalah delay lama motor
CUV_J1 MOV r5,#20
DJNZ r5,$ ; berputar
DJNZ r6,CUV_J1 ;
DJNZ r7,CUV_J2 ;
SETB U_Valve_1 ; matikan motor
SETB U_Valve_2 ;
CLR iel
SETB tr0
SETB ea
RET

; prosedur untuk membuka kran buang

Open_Lower_Valve
CLR ea
CLR tr0
SETB L_Va1ve_1 ; nyalakan motor
CLR L_Va1ve_2 ;

MOV r7,#200 ;
OLV_J2 MOV r6,#250 ; Ini adalah delay lama motor
OLV_J1 MOV r5,#20 ;

DJNZ r5,$ ; berputar
DJNZ r6,OLV_J1 ;
DJNZ r7,OLV_J2 ;

SETB L_Va1ve_1 ; matikan motor
SETB L_Va1ve_2 ;
CLR iel
SETB tr0
SETB ea
RET

; prosedur untuk menutup kran buang

Close_Lower_Va1ve
CLR ea
CLR tr0
CLR L_Va1ve_1 ; nyalakan motor
SETB L_Va1ve_2 ;

MOV r7,#200 ;
OLV_J2 MOV r6,#250 ; Ini adalah delay lama motor
OLV_J1 MOV r5,#20 ;

DJNZ r5,$ ; berputar
DJNZ r6,OLV_J1 ;
DJNZ r7,OLV_J2 ;

SETB L_Va1ve_1 ; matikan motor
SETB L_Va1ve_2 ;
CLR iel
SETB tr0
SETB ea
RET

; prosedur pengecekan / pengontrol pembukaan / penutupan kran secara otomatis

Valve_Ctr1
MOV a,Tank_Status
CJNE a,#0,VC_J1 ; kalau air kosong, lakukan :
CLR Heater_Status ;
CLR Heater ; 1. matikan heater
JNB Lower_Va1ve,VC_J2 ; 2. tutup kran buang (kalau masih terbuka)
CLR Lower_Va1ve ; 3. buka kran isi (kalau tertutup)
LCALL Close_Lower_Va1ve
VC_J2 JB Upper_Va1ve,VC_J3
SETB Upper_Va1ve
LCALL Open_Upper_Va1ve
VC_J3 RET

VC_J1 CJNE a,#2,VC_J3
JNB Upper_Va1ve,VC_J3
CLR Upper_Valve
LCALL Close_Upper_Valve
RET

; prosedur pengecekan / pengontrol pembukaan / penutupan kran
; yang dikontrol manual dari kontroler 2

Check_Valve_Ctrl
    JB C Check_Ctrl_F,CVC_J1 ; apakah ada pengontrolan manual ?
    RET ; (ada data kontrol status yg masuk)
CVC_J1
    CLR Check_Ctrl_F
    MOV a, Dummy_2
    ANL a, #1
    CJNE a, #1, CVC_J2
    JB Upper_Valve, CVC_J3 ; buka kran isi
    SETB Upper_Valve
    LCALL Open_Upper_Valve
    AJMP CVC_J3
CVC_J2
    CJNE a, #0, CVC_J3
    JNB Upper_Valve, CVC_J3 ; tutup kran isi
    CLR Upper_Valve
    LCALL Close_Upper_Valve
CVC_J3
    MOV a, Dummy_2
    ANL a, #2
    CJNE a, #2, CVC_J4
    JB Lower_Valve, CVC_J5 ; buka kran buang
    SETB Lower_Valve
    LCALL Open_Lower_Valve
    AJMP CVC_J5
CVC_J4
    CJNE a, #0, CVC_J5
    JNB Lower_Valve, CVC_J5 ; tutup kran buang
    CLR Lower_Valve
    LCALL Close_Lower_Valve
CVC_J5
    RET

;----------
; Main Program
;----------

Start
    LCALL Initialize_Data
Loop
    LCALL Read_ADC
    LCALL Check_Ctrl_Status
    LCALL Check_Heater
    LCALL Valve_Ctrl
    LCALL Check_Valve_Ctrl
    AJMP Loop
LAMPIRAN C
### 2.4 Instruction Outline

#### Table 5 List of instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Code</th>
<th>Function</th>
<th>Execution Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1) Display clear</td>
<td>0 0 0 0 0 0 0 0</td>
<td>Clears all display and returns cursor to home position (address 0)</td>
<td>1.64 ms</td>
</tr>
<tr>
<td>(2) Cursor Home</td>
<td>0 0 0 0 0 0 0 1</td>
<td>Returns cursor to home position. Shifted display returns to home position and DD RAM contents do not change.</td>
<td>1.64 ms</td>
</tr>
<tr>
<td>(3) Entry Mode Set</td>
<td>0 0 0 0 0 0 1 1</td>
<td>Sets direction of cursor movement and whether display will be shifted when data is written or read.</td>
<td>40 μs</td>
</tr>
<tr>
<td>(4) Display ON/OFF control</td>
<td>0 0 0 0 0 0 1 0 0 0 1</td>
<td>Turns ON/OFF total display (D) and cursor (C), and makes cursor position column start blinking (B).</td>
<td>40 μs</td>
</tr>
<tr>
<td>(5) Cursor/Display Shift</td>
<td>0 0 0 0 0 1</td>
<td>Moves cursor and shifts display without changing DD RAM contents.</td>
<td>40 μs</td>
</tr>
<tr>
<td>(6) Function Set</td>
<td>0 0 0 0 1</td>
<td>Sets interface data length (DL).</td>
<td>40 μs</td>
</tr>
<tr>
<td>(7) CG RAM Address Set</td>
<td>0 0 0</td>
<td>Sets CG RAM address to start transmitting or receiving CG RAM data.</td>
<td>40 μs</td>
</tr>
<tr>
<td>(8) DD RAM Address Set</td>
<td>0 0 1</td>
<td>Sets DD RAM address to start transmitting or receiving DD RAM data.</td>
<td>40 μs</td>
</tr>
<tr>
<td>(5) BF/Address Read</td>
<td>1 0</td>
<td>Reads BF indicating module in internal operation and AC contents (used for both CG RAM and DD RAM).</td>
<td>8 μs</td>
</tr>
<tr>
<td>(10) Data Write to CG RAM or DD RAM</td>
<td>1 0</td>
<td>Writes data into DD RAM or CG RAM.</td>
<td>40 μs</td>
</tr>
<tr>
<td>(11) Data Read from CG RAM or DD RAM</td>
<td>1 1</td>
<td>Reads data from DD RAM or CG RAM.</td>
<td>40 μs</td>
</tr>
</tbody>
</table>

* : Invalid bit

- Acc : CG RAM address
- Addr : DD RAM address

- D = 1 : Display ON
- D = 0 : Display OFF
- S = 1 : Display shift
- S = 0 : No display shift
- R = 1 : Cursor ON
- R = 0 : Cursor OFF
- R = 1 : Right shift
- R = 0 : Left shift
- C = 1 : Cursor ON
- C = 0 : Cursor OFF
- BF = 1 : Internal operation in progress
- BF = 0 : Instruction can be accepted

#### Symbol Explanation

- ID = 1 : Increment
- ID = 0 : Decrement
- BD = 1 : Blink ON
- BD = 0 : Blink OFF
- DL = 1 : 8 bits
- DL = 0 : 4 bits
- 5 = 1 : Internal operation in progress
- 5 = 0 : Instruction can be accepted

#### Additional Note

- Internal operation in progress: BF = 1
- Instruction can be accepted: BF = 0
### Table 3 CorresponJence between character codes and character patterns

<table>
<thead>
<tr>
<th>Upper bit 4 bit</th>
<th>Lower bit 4 bit</th>
<th>0000</th>
<th>0010</th>
<th>0011</th>
<th>0100</th>
<th>0101</th>
<th>0110</th>
<th>0111</th>
<th>1010</th>
<th>1011</th>
<th>1100</th>
<th>1101</th>
<th>1110</th>
<th>1111</th>
</tr>
</thead>
<tbody>
<tr>
<td>CG RAM (1)</td>
<td>0000</td>
<td>0aP</td>
<td>p</td>
<td>9eP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0001</td>
<td>110a</td>
<td>ąćęłńś</td>
<td></td>
<td></td>
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<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0010</td>
<td>2bBb</td>
<td>bńźż</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0011</td>
<td>#3Csc</td>
<td>sćęćś</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0100</td>
<td>$4Ddt</td>
<td>dt·čĐć</td>
<td></td>
<td></td>
<td></td>
<td></td>
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SURABAYA
Tempat / Tanggal lahir : LUMAJANG, 18 MEI 1976
Agama : KATOLIK

Riwayat Pendidikan :
Lulus SD Kristen Aletheia, Lumajang tahun 1988.