LAMPIRAN
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Tabel pengukuran kecepatan terhadap waktu pada 1400 rpm

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ORG 0000H

ORG 060H

Pembagian:

0060 78 24 MOV R0,#HasilBagi
0062 11 D3 =00D3 ACALL HapusNilai
0064 78 26 MOV R0,#SisaBagi
0066 11 D3 =00D3 ACALL HapusNilai
0068 7B 10 MOV R3,#SizeX*8
006A LoopPembagian:

006A C3 CLR C
006B 78 20 MOV R0,#Operand
006D 11 89 =0089 ACALL GeserKiri1X
006F 78 26 MOV R0,#SisaBagi
0071 11 89 =0089 ACALL GeserKiri1X
0073 78 26 MOV R0,#SisaBagi
0075 79 22 MOV R1,#Pembagi
0077 11 BE =00BE ACALL Perbandingan SisaBagi=Pembagi?
0079 40 06 =0081 JC JanganDikurangi SisaBagi<Pembagi, skip!
007B 78 26 MOV R0,#SisaBagi
007D 79 22 MOV R1,#Pembagi
007F 11 C8 =00C8 ACALL Pengurangan SisaBagi:=SisaBagi-Pembagi
0081 JanganDikurangi:

0081 B3 CPL C
0082 78 24 MOV R0,#HasilBagi Simpan hasil
0084 11 89 =0089 ACALL GeserKiri1X
0086 DB E2 =006A DJNZ R3,LoopPembagian
0088 22 RET
0089 GeserKiri1X:
0089 7A 02 MOV R2,#SizeX
008B LeftShift:
008B E6 MOV A,@R0
008C 33 RIC A
2008D F6       MOV @R0,A
2008E 08       INC R0
2008F DA FA    =008B DJNZ R2,LeftShift
20091 22       RET
20092
20092 78 24    MOV R0,#HasilKali
20094 11 D3    =00D3 ACALL HapusNilai
20096 7B 10    MOV R3,#SizeX*8
20098
20098 C3       CLR C
20099 78 23    MOV R0,#Pengali+SizeX-1
2009B 7A 02    MOV R2,#SizeX
2009D
2009D E6       MOV A,@R0
2009E 13       RRC A
2009F F6       MOV @R0,A
200A 18       DEC R0
200A1 DA FA    =009D DJNZ R2,GeserKanan
200A3 50 06    =00AB JNC JanganDitambah
200A5 78 24    MOV R0,#HasilKali
200A7 79 20    MOV R1,#Operand
200A9 11 B3    =00B3 ACALL Penambahan
200AB
200AB C3       CLR C
200AC 78 20    MOV R0,#Operand
200AE 11 89    =0089 ACALL GeserKiriX
200B0 DB E6    =0098 DJNZ R3,LoopPerkalian
200B2 22       RET
200B3
200B3 C3       CLR C
200B4 7A 02    MOV R2,#SizeX
200B6
200B6 E6       MOV A,@R0
200B7 37       ADDC A,@R1
200B8 F6       MOV @R0,A
200B9 08       INC R0
200BA 09       INC R1
200BB DA FA    =00B6 DJNZ R2,LoopPenambahan
200BD 22       RET
200BE
200BE C3       CLR C
200BF 7A 02    MOV R2,#SizeX
200C1
200C1 E6       MOV A,@R0
200C2 97       SUBB A,@R1
200C3 09       INC R1
200C4 08       INC R0
200C5 DA FA    =00C1 DJNZ R2,LoopPerbandingan
200C7 22       RET
200C8
200C8 C3       CLR C
200C9 7A 02    MOV R2,#SizeX
200C9
200CB
200CB E6       MOV A,@R0
200CC 97       SUBB A,@R1
200CD F6       MOV @R0,A
200CE 08       INC R0
200CF 09       INC R1
200DD DA FA    =00CB DJNZ R2,LoopPengurangan
200D2 22       RET
200D3
200D3 HapusNilai:
MOV R2,#SizeX
LOOPHapus:
MOV @R0,#0
INC R0
=00D5 DJNZ R2,LoopHapus
RET

POSISI2.1:
PUSH A
MOV A,R7 ;KOLOM 1
POSISI2:
ADD A,#11000000B ;POSISI DI BARIS 2
=00E7 SJMP POSISI.SUB
POSISI1.1:
PUSH A ;KOLOM 1
MOV A,R6
POSISI1:
ADD A,#10000000B
POSISI.SUB:
OEC 1>
=00FO ACAI,L CONTROLOUT
POP A
RET

PRINTSTRING2: ;CETAK STRING DI BARIS 2 KOLOM 1
=00DB ACALL POSISI2.1 ;BARIS 2 KOLOM 1
PRINTSTRING1: ;CETAK STRING DI BARIS 1 KOLOM 1
=00E2 ACALL POSISI1.1 ;BARIS 1 KOLOM 1
PRINTSTRING:
=00F3 SJMP PRINTSTRING ;CETAK STRING
PRINTSTRINGLOOP:
=0106 ACALL DATAOUT ;KIRIM SEBAGAI OPERASI KONTROL
PRINTSTRING:
=010F SJMP OUTSTRING ;KIRIM SEBAGAI OPERASI DATA
=0107 SJMP PRINTSTRINGLOOP ;APEKAH MASIH ADA DATA BERIKUTNYA
PRINTSTRING:

CONTROLOUT:
PUSH DPH ;SIMPAN DPH 01 STACK
PUSH OPL ;SIMPAN OPL 01 STACK
MOV OPTR,#L0CO ;ALAMAT OPERASI CONTROL LCD
=0100 SJMP LCD.OUT ;KIRIM KE LCD
DATAOUT:
PUSH DPH ;SIMPAN DPH DI STACK
PUSH DPL ;SIMPAN DPL DI STACK
MOV DPTR,#L0CD0 ;ALAMAT OPERASI CONTROL LCD
=010D SJMP LCD.OUT ;KIRIM KE LCD

L0CD0:
PUSH DPH ;SIMPAN DPH DI STACK
PUSH DPL ;SIMPAN DPL DI STACK
MOV DPTR,#L0CD1 ;ALAMAT OPERASI DATA LCD
LCD.OUT:
=010D SJMP LCD.OUT ;KIRIM KE LCD

PRINTSTRINGLOOP:
=010D SJMP PRINTSTRINGLOOP ;APEKAH MASIH ADA DATA BERIKUTNYA
=010F SJMP OUTSTRING ;KIRIM SEBAGAI OPERASI DATA
PRINTSTRING:

DATAOUT:
PUSH DPH ;SIMPAN DPH DI STACK
PUSH DPL ;SIMPAN DPL DI STACK
MOV DPTR,#L0CD1 ;ALAMAT OPERASI DATA LCD
LCD.OUT:
=010D SJMP LCD.OUT ;KIRIM KE LCD

DELAY.LCD:
=010E 74 FA MOV A,#250 ;250
=0110 55 E0 FD =0110 DJNZ A,$ ;AMBIL KEMBALI DPL DARI STACK
=0113 00 82 POP DPL ;AMBIL KEMBALI DPL DARI STACK
=0115 00 83 POP DPH
=0117 22 RET

DELAYIT:
=0118 79 40 MOV R1,#040h ;20h
=0119 DLY.LCD.LP:
=011A 7A 14 MOV R2,#20 ;0
=011C DA FE =011C DJNZ R2,$
=011E D9 FA =011A DJNZ R1,DLY.LCD.LP
Init_LCD:

MOV A,#DISPCLR ; DISPLAY CLEAR
ACALL CONTROLROUT

MOV A,#DISPON ; DISPLAY ON
ACALL CONTROLROUT

MOV A,#ENTRMOD ; ENTRY MODE
ACALL CONTROLROUT

Delay:

MOV r3,#2

Delay2:

MOV r4,#255

Delay1:

MOV r5,#255
DJNZ r5,delay1

DJNZ r4,delay1

DJNZ r3,delay2

Tamp_setup:

MOV r6,#12
ACALL posisi1.1
MOV a,#0
ADD ab
ACALL dataout

Ulang1:

MOV buffer, setup
MOV r6,#11

MOV a,buffer
MOV b,#10
DIV ab
MOV buffer, a
MOV a,b
ADD a,#30h
ACALL dataout

Dec r6

CJNE r6,#8,ulang1

MOV r6,#14
ACALL posisi1.1
MOV a,'#R'
ACALL dataout
MOV r6,#15
ACALL posisi1.1
MOV a,'#P'
ACALL dataout
MOV r6,#16
ACALL posisi1.1
MOV a,'#M'
ACALL dataout

ACALL CONTROLROUT

RET

Tampilan:

MOV hasilbagi,simpan
0180 85 09 25  MOV hasilbagi+1, simpan+1
0183 7F 0C  MOV R7, #12
0185      ulxx:
0185 11 DB =00DB ACALL POSISI2.1
0187 85 24 20  MOV operand, hasilbagi
018A 85 25 21  MOV operand+1, hasilbagi+1
018D 75 22 0A  MOV pembagi, #10
0190 11 60 =0060 ACALL pembagian -
0192 78 26  MOV r0, #sisabagi
0194 B6  MOV a, @r0
0195 CO E0  PUSH a
0197 78 24  MOV r0, #hasilbagi
0199 B6  MOV a, @r0
019A B4 00 08 =01A5 CJNE a, #0, err
019D D0 E0  POP a
019F 24 30  ADD A, #30H
01A1 31 06 =0106 ACALL DATAOUT
01A3 21 B1 =01B1 AJMP akhir
01A5  err:
01A5 D0 E0  POP a
01A7 24 30  ADD A, #30H
01A9 31 06 =0106 ACALL DATAOUT
01AB 1F  DEC r7
01AC BF 08 D6 =0185 CJNE r7, #8, ulxx
01AF 21 C7 =01C7 AJMP selesai

01B1      akhir:
01B1 BF 01 08 =01BC CJNE r7, #1, ada
01B4 11 DB =00DB ACALL posisi2.1
01B6 74 30  MOV a, #'0'
01B8 31 06 =0106 ACALL dataout
01BA 21 C7 =01C7 AJMP selesai
01BC      ada:
01BC 1F  DEC r7
01BD      bersih:
01BD 11 DB =00DB ACALL posisi2.1
01BF 74 20  MOV a, #'
01C1 31 06 =0106 ACALL dataout
01C3 1F  DEC r7
01C4 BF 08 F6 =01BD CJNE r7, #8, bersih

01C7      selesai:
01C7 7F 0E  MOV r7, #14
01C9 11 DB =00DB ACALL posisi2.1
01CB 74 52  MOV a, #'R'
01CD 31 06 =0106 ACALL dataout
01CF 7F 0F  MOV r7, #15
01D1 11 DB =00DB ACALL posisi2.1
01D3 74 50  MOV a, #'P'
01D5 31 06 =0106 ACALL dataout
01D7 7F 10  MOV r7, #16
01D9 11 DB =00DB ACALL posisi2.1
01DB 74 4D  MOV a, #'M'
01DD 31 06 =0106 ACALL dataout
01DF 22  RET

01E0      hitung_rpm:
01E0 85 0A 20  MOV operand, setuprpm
01E3 85 0B 21  MOV operand+1, setuprpm+1
01E6 75 22 0A  MOV pengali, #10
01E9 11 92 =0092 ACALL perkalian
01EB 85 24 0A  MOV  setuprpm,hasilkali
01EE 85 25 0B  MOV  setuprpm+1,hasilkali+1

01F1 85 08 20  MOV  operand, simpan
01F4 85 09 21  MOV  operand+1, simpan+1
01F7 75 22 20  MOV  pengali,#32
01FA 11 92 00 92  ACALL  perkalian
01FC 85 24 08  MOV  simpan, hasilkali
01FF 85 25 09  MOV  simpan+1, hasilkali+1

0202 85 08 20  MOV  operand, simpan
0205 85 09 21  MOV  operand+1, simpan+1
0208 75 22 05  MOV  pembagi,#5
020B 11 60 00 60  ACALL  pembagian
020D 85 24 08  MOV  simpan, hasilkali
0210 85 25 09  MOV  simpan+1, hasilkali+1
0213 22  RET

0214 MAIN:
0214 75 81 60  MOV  SP,#60H
0217 75 A8 00  MOV  ie,#00H
021A 31 21 =0121 ACALL  init.lcd
021C 71 68 =0368 ACALL  INT_PPI
021E 7E 01  MOV  r6,#1
0220 7F 01  MOV  r7,#1
0222 90 03 77  MOV  dptr,#header1
0225 11 F1 =00F1 ACALL  printstring1
0227 90 03 88  MOV  dptr,#header2
022A 7E 01  MOV  r6,#1
0230 7F 01  MOV  r7,#1
0232 90 03 99  MOV  dptr,#header3
0235 11 F1 =00F1 ACALL  printstring1
0237 90 03 AA  MOV  dptr,#header4
023A 7E 01  MOV  r6,#1
023C 31 34 =0134 ACALL  delay
023E 7E 01  MOV  r6,#1
0240 7F 01  MOV  r7,#1
0242 90 03 BB  MOV  dptr,#header5
0245 11 F1 =00F1 ACALL  printstring1
0247 90 03 CC  MOV  dptr,#header6
024A 7E 01  MOV  r6,#1
024C 7F 01  MOV  r7,#1
0250 90 03 DD  MOV  dptr,#header7
0255 11 F1 =00F1 ACALL  printstring1
0257 90 03 EE  MOV  dptr,#header8
025A 7E 01  MOV  r6,#1
025C 31 34 =0134 ACALL  delay

025E 75 0C 00  MOV  setup,#0
0261 75 0D 00  MOV  buffer,#0
0264 75 0E 00  MOV  input,#0
0267 75 0F 00  MOV  outputdac,#0

026A 74 01  MOV  A,#DISPCLR ;DISPLAY CLEAR
026C 11 FD =00FD ACALL  CONTROLOUT
026E 31 34 =0134 ACALL  delay
0270 90 03 FF  MOV  dptr,#output
0273 7E 01  MOV  r6,#1
0275 11 F1 =00F1 ACALL printstring1
0277 90 04 07 MOV dptr,#output2
027A 7F 01 MOV r7,#1
027C 11 ED =00ED ACALL printstring2
027E 31 34 =0134 ACALL delay
0280 31 41 =0141 ACALL tamp_setup

0282 TEST:
0282 30 90 68 =02F0 JNB P1.0, UP;jika tb UP ditekan maka akan ke label UP
0285 30 91 7A =0302 JNB P1.1, DOWN;jika tb DOWN ditekan ke label DOWN
0288 71 4A =034A ACALL READ_ADC ;panggil label READ_ADC
028A 75 08 00 MOV simpan,#0
028D 75 09 00 MOV simpan+1,#0
0290 75 0A 00 MOV setuprpm,#0
0293 75 0B 00 MOV setuprpm+1,#0
0296 85 0E 08 MOV simpan,input
0299 85 0C 0A MOV setuprpm, setup

029C 31 E0 =01E0 ACALL hitung_rpm
029E 78 08 MOV .r0,#simpan
02A0 79 0A MOV .r1,#setuprpm
02A2 11 BE =00BE ACALL perbandingan
02A4 40 23 =02C9 JC tambah_kecepatan

02A6 E5 0F MOV a, outputdac
02A8 B4 00 02 =02AD CJNE a,#0, kurang
02AB 41 EA =02EA AJMP lompat

02AD kurang:
02AD 15 0F DEC outputdac
02AF 7F 04 MOV r7,#4
02B1 11 DB =00DB ACALL posisi2.1
02B3 74 28 MOV a,#'('
02B5 31 06 =0106 ACALL dataout
02B7 7F 05 MOV r7,#5
02B9 11 DB =00DB ACALL posisi2.1
02BB 74 4B MOV a,#'K'
02BD 31 06 =0106 ACALL dataout
02BF 7F 06 MOV r7,#6
02C1 11 DB =00DB ACALL posisi2.1
02C3 74 29 MOV a,#')'
02C5 31 06 =0106 ACALL dataout

02C7 41 EA =02EA AJMP lompat

02C9 tambah_kecepatan:
02C9 E5 0F MOV a, outputdac
02CB B4 F1 02 =02D0 CJNE a,#255, tambah
02CE 41 EA =02EA AJMP lompat

02D0 tambah:
02D0 0F 05 INC outputdac
02D2 7F 04 MOV r7,#4
02D4 11 DB =00DB ACALL posisi2.1
02D6 74 28 MOV a,#'('
02D8 31 06 =0106 ACALL dataout
02DA 7F 05 MOV r7,#5
02DC 11 DB =00DB ACALL posisi2.1
02DE 74 54 MOV a,#'T'
02E0 31 06 =0106 ACALL dataout
02E2 7F 06 MOV r7,#6
02E4 11 DB =00DB ACALL posisi2.1
02E6 74 29 MOV a,')'
02E8 31 06 =0106 ACALL dataout

02EA lompat:
02EA 71 59 =0359 ACALL DAC_OUT ; panggil label DAC_OUT
02EC 31 7D =017D ACALL tampilan

02EE 41 82 =0282 AJMP TEST ; kembali ke label TEST

02F0 UP:
02F0 A8 0C MOV r0,setup
02F2 B8 A0 05 =02FA CJNE r0,#160,lom1
02F5 75 0C 00 MOV setup,#0
02F8 41 FC =02FC AJMP lom3
02FA lom1:
02FA 05 0C INC SETUP
02FC lom3:
02FC 71 34 =0334 ACALL delay_2ss
02FE 31 41 =0141 ACALL tampil_setup
0300 41 82 =0282 AJMP TEST

0302 DOWN:
0302 A8 0C MOV r0,setup
0304 B8 00 05 =030C CJNE r0,#0,lom2
0307 75 0C A0 MOV setup,#160
030A 61 0E =030E AJMP lom4
030C lom2:
030C 15 0C DEC SETUP
030E lom4:
030E 71 34 =0334 ACALL delay_2ss
0310 31 41 =0141 ACALL tampil_setup
0312 41 82 =0282 AJMP TEST

0314 DELAY_2S:
0314 C0 83 PUSH DPH
0316 C0 82 PUSH DPL
0318 C0 E0 PUSH ACC
031A C0 D0 PUSH PSW
031C 7D 01 MOV R5,#01H
031E DEL3:
031E 74 4F MOV A,#04FH
0320 DEL4:
0320 75 F0 FF MOV B,#0FFH
0323 D5 F0 FD =0323 DJNZ B,$
0326 D5 E0 F7 =0320 DJNZ ACC,DEL4
0329 DD F3 =0:1E DJNZ R5,DEL3
032B D0 D0 POP PSW
032D D0 E0 POP ACC
032F D0 82 POP DPL
0331 D0 B3 POP DPH
0333 22 RET

0334 DELAY_2SS:
0334 C0 83 PUSH DPH
0336 C0 82 PUSH DPL
0338 90 E0 02 MOV DPTR,#PORT_C
033B 74 01 MOV A,#00000000B
033D F0 MOVX @DPTR,A
033E 71 14 =0314 ACALL delay_2s
0340 74 00 MOV A,#00000000B
0342 F0 MOVX @DPTR,A
0343 71 14 =0314 ACALL DELAY_2s
0345 D0 82 POP DPL
0347 D0 83 POP DPH
0349 22 RET

;---------------------------------------------------------------------------
034A READ_ADC:
034A CO 83 PUSH DPH
034C CO 82 PUSH DPL
034E 90 E0 00 MOV DPTR,#PORT_A
0351 E0 MOVX A,@DPTR
0352 F5 03 MOV input,a
0354 D0 82 POP DPL
0356 D0 83 POP DPH
0358 22 RET

;----------------------------------
0359 DAC_OUT:
0359 CO 83 PUSH DPH
035B CO 82 PUSH DPL
035D 90 E0 01 MOV DPTR,#PORT_B
0360 E5 0F MOV A,outputdac
0362 F0 MOVX @DPTR,A
0363 D0 82 POP DPL
0365 D0 83 POP DPH
0367 22 RET

0368 INIT_PPI:
0368 CO 83 PUSH DPH
036A CO 82 PUSH DPL
036C 90 E0 03 MOV DPTR,#CONTROL_REG
036F 74 98 MOV A,#98H
0371 F0 MOVX @DPTR,A
0372 D0 82 POP DPL
0374 D0 83 POP DPH
0376 22 RET

;----------------------------------------------------------------------------
0377 HEADER1:
0377 4D 49 43 DB 'MICROCONTROLLER ',0
0388 HEADER2:
0388 20 20 20 DB ' DRIVEN ',0
0399 HEADER3:
0399 20 44 49 DB ' DIGITAL MOTOR ',0
03AA HEADER4:
03AA 53 50 45 DB 'SPEED CONTROLLER',0
03BB HEADER5:
03BB 20 20 44 DB ' DESIGNED BY: ',0
03CC HEADER6:
03CC 20 20 20 DB ' BAMBANG ',0
03DD HEADER7:
03DD 20 20 20 DB ' FTE UNIKA ',0
03EE HEADER8:
03EE 20 20 57 DB 'WIDYA MANDALA ',0
03FF OUTPUT:
03FF 53 45 54 DB 'SETUP :',0
0407 OUTPUT2:
0407 52 50 4D DB 'RPM :',0

***** Successfull
Features
Compatible with MCS-51™ Products
4K Bytes of In-System Reprogrammable Flash Memory
- Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
  - 128 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- 8x Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

Description
The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K
bytes of Flash Programmable and Erasable Read Only Memory (PEROM). The
device is manufactured using Atmel's high density nonvolatile memory technology
and is compatible with the industry standard MCS-51™ instruction set and pinout. The
in-chip Flash allows the program memory to be reprogrammed in-system or by a con-
tentional nonvolatile memory programmer. By combining a versatile 8-bit CPU with
Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which
provides a highly flexible and cost effective solution to many embedded control appli-
cations.

In Configurations

(continued)
ADC0801, ADC0802, ADC0803, ADC0804, ADC0805 8-Bit μP Compatible A/D Converters

General Description

ADC0801, ADC0802, ADC0803, ADC0804, ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—ear to the 255R products. These converters are designed to allow operation with the NSC800 and IN5808A/NSC814A/NSC815A on-chip clock generator

- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM330) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3V standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratio metrically or with 5 VDC, 2.5 VDC, or analog span adjusted voltage reference

Key Specifications

- Resolution 8 bits
- Total error ±½ LSB, ±½ LSB, and ±1 LSB
- Conversion time 100 μs

Applications

8080 Interface

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Full-Scale Adjusted</th>
<th>( V_{REF}/2 = 2.500 \text{ VDC} ) (No Adjustments)</th>
<th>( V_{REF}/2 = \text{No Connection} ) (No Adjustments)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC0801</td>
<td>±½ LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC0802</td>
<td>±½ LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC0803</td>
<td>±½ LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC0804</td>
<td>±1 LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC0805</td>
<td>±1 LSB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<Diagram of circuit>
### Maximum Ratings (Notes 1 & 2)

Aerospace specified devices are required, please contact National Semiconductor Sales Office for availability and specifications.

**Input Voltage (VCC)** (Note 3): 8.5V

**Input and Output Levels**:
- **Input (±0.3V to VCC ±0.3V)**
- **Output (0.3V to VCC +0.3V)**

**Package and Soldering**:
- Juke Package (plastic)
  - 260°C
- Juke Package (ceramic)
  - 300°C
- Mount Package
  - Phase (60 seconds)
    - 215°C
  - d (15 seconds)
    - 220°C

### Temperature Ranges

- **Storage Temperature Range**: -65°C to +150°C
- **Package Dissipation at T_A = 25°C**: 875 mW
- **ESD Susceptibility (Note 10)**: 800V

### Operating Ratings (Notes 1 & 2)

**Temperature Range**:
- **T_MIN ≤ T_A ≤ T_MAX**:
  - ADC0801/02LJ: -55°C ≤ T_A ≤ +125°C
  - ADC0801/02/03/04LCJ: -40°C ≤ T_A ≤ +85°C
  - ADC0801/02/03/05LCN: -40°C ≤ T_A ≤ +85°C
  - ADC0804LCN: 0°C ≤ T_A ≤ +70°C
  - ADC0802/03/04LCV: 0°C ≤ T_A ≤ +70°C
  - ADC0802/03/04LCWM: 0°C ≤ T_A ≤ +70°C

**Range of VCC**:
- 4.5 VDD to 6.3 VDD

### Electrical Characteristics

#### Analog Characteristics

All specifications apply for VCC = 5 VDD, T_MIN ≤ T_A ≤ T_MAX and ICLK = 640 kHz unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>With Full-Scale Adj. (See Section 2.5.2)</td>
<td>± 1/2</td>
<td>LSb</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VREF/2</td>
<td>2.500 VDD</td>
<td>± 1/2</td>
<td>LSb</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage Range</td>
<td>(Note 4) V(+ or V(−)</td>
<td>Gnd-0.05 VDD</td>
<td>± 1/4 VDD</td>
<td>LSb</td>
<td></td>
</tr>
</tbody>
</table>

#### Voltage Sensitivity

VDD = 5 VDD ± 10% Over Allowed VIN(+ and VIN(−) Voltage Range (Note 4)

### Technical Characteristics

All specifications apply for VCC = 5 VDD and T_A = 25°C unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conversion Time</td>
<td>ICLK = 640 kHz (Note 6)</td>
<td>103</td>
<td>114</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>Conversion Time</td>
<td>(Note 5, 6)</td>
<td>66</td>
<td>73</td>
<td>1/CLK</td>
<td></td>
</tr>
<tr>
<td>Clock Frequency</td>
<td>VCC = 5V, (Note 5)</td>
<td>100</td>
<td>640</td>
<td>1460 kHz</td>
<td></td>
</tr>
<tr>
<td>Clock Duty Cycle</td>
<td>(Note 5)</td>
<td>40</td>
<td>60</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Conversion Rate in Free-Running Mode</td>
<td>INTR tied to WR with CS = 0 VDD, ICLK = 640 kHz</td>
<td>8770</td>
<td>9708</td>
<td>conv/s</td>
<td></td>
</tr>
<tr>
<td>Width of WR Input (Start Pulse Width)</td>
<td>CS = 0 VDD (Note 7)</td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Access Time (Delay from Falling Edge of RD to Output Data Valid)

| CL | 100 pF | 135 | 200 | ns |

#### TRI-STATE Control (Delay from Rising Edge of RD to HI-Z State)

| CL | 10 pF, RL = 10k | 125 | 200 | ns |

#### Delay from Falling Edge of WR or RD to Reset of INTR

| 300 | 450 | ns |

#### Input Capacitance of Logic Control Inputs

| 5 | 7.5 | pF |

#### TRI-STATE Output Capacitance (Data Buffers)

| 5 | 7.5 | pF |

**NOTES**

- CL (Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately)
- Logical "1" Input Voltage (Except Pin 4 CLK IN)
  - VDD = 5.25 VDD
  - 2.0 | 15 | VDD
### Electrical Characteristics (Continued)

Flowing specifications apply for \( V_{CC} = 5 \text{VDC} \) and \( T_{IN} \leq T_A \leq T_{MAX} \) unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ROL INPUTS</strong> (NOT CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logical &quot;0&quot; Input Voltage (Except Pin 4 CLK IN)</td>
<td>( V_{CC} = 4.75 \text{ VDC} )</td>
<td>0.8</td>
<td></td>
<td></td>
<td>( \text{Vdc} )</td>
</tr>
<tr>
<td>Logical &quot;1&quot; Input Current (All Inputs)</td>
<td>( V_{IN} = 5 \text{ VDC} )</td>
<td>0.005</td>
<td>1</td>
<td></td>
<td>( \mu\text{Acc} )</td>
</tr>
<tr>
<td>Logical &quot;0&quot; Input Current (All Inputs)</td>
<td>( V_{IN} = 0 \text{ VDC} )</td>
<td>-1</td>
<td>-0.005</td>
<td></td>
<td>( \mu\text{Acc} )</td>
</tr>
</tbody>
</table>

| **CLK IN AND CLOCK R** | | | | | |
| CLK IN (Pin 4) Positive Going Threshold Voltage | | 2.7 | 3.1 | 3.5 | \( \text{Vdc} \) |
| CLK IN (Pin 4) Negative Going Threshold Voltage | | 1.5 | 1.8 | 2.1 | \( \text{Vdc} \) |
| CLK IN (Pin 4) Hysteresis \((V^+)-(V^-)\) | | 0.6 | 1.3 | 2.0 | \( \text{Vdc} \) |

| **A OUTPUTS AND INTR** | | | | | |
| Logical "0" Output Voltage Data Outputs | \( D_{OUT} = 1.6 \text{ mA}, V_{CC} = 4.75 \text{ VDC} \) | 0.4 | 0.4 | | \( \text{Vdc} \) |
| INTR Output | \( D_{OUT} = 1.0 \text{ mA}, V_{CC} = 4.75 \text{ VDC} \) | 0.4 | 0.4 | | \( \text{Vdc} \) |
| Logical "1" Output Voltage | \( D_{OUT} = -360 \mu\text{A}, V_{CC} = 4.75 \text{ VDC} \) | 2.4 | | | \( \text{Vdc} \) |
| Logical "1" Output Voltage | \( D_{OUT} = -10 \mu\text{A}, V_{CC} = 4.75 \text{ VDC} \) | 4.5 | | | \( \text{Vdc} \) |
| TRI-STATE Disabled Output Leakage (All Data Buffers) | | \( V_{OUT} = 0 \text{ VDC} \) | -3 | | \( \mu\text{Acc} \) |
| | | \( V_{OUT} = 5 \text{ VDC} \) | | 3 | \( \mu\text{Acc} \) |
| **AC** | | | | | |
| \( V_{OUT} \) Short to Gnd, \( T_A = 25^\circ \text{C} \) | 4.5 | | 6 | | \( \text{mAcc} \) |
| \( V_{OUT} \) Short to VCC, \( T_A = 25^\circ \text{C} \) | 9.0 | | 18 | | \( \text{mA} \) |

| **ER SUPPLY** | | | | | |
| Supply Current (Includes Ladder Current) | \( f_{CLK} = 640 \text{ kHz} \), \( V_{REF/2} = NC, T_A = 25^\circ \text{C} \) and \( CS = 5 \text{V} \) | 1.1 | 1.8 | | \( \text{mA} \) |
| | \( V_{CC0801/02/03/04/LCJ/05} \) | 1.9 | | 2.5 | | \( \text{mA} \) |

1. Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating vices beyond as specified operating conditions.

2. All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be used to the O Gnd.

3. A power supply must be applied from the device to Gnd and do not exceed 10% below the specified voltage of \( V_{CC} \).

4. For \( V_{CC} \) of \( 5 \text{ VDC} \), the digital output code will be 0000 0000. Two on-chip decoders are tied to each analog input (see block diagram) which are loaded by the output voltage. These pins can cause the input voltage to exceed the absolute maximum rating of \( 5 \text{VDC} \).

5. This is a guaranteed specification by \( V_{CC} \) and \( T_A \) maximum. The output voltage range is \( 0 \text{ VDC} \) to \( 5 \text{ VDC} \) when \( V_{CC} = 4.75 \text{ VDC} \) and \( T_A = 25^\circ \text{C} \).

6. Accuracy is guaranteed at \( V_{CC} = 4.4 \text{ VDC} \). At higher clock frequencies, accuracy can degrade. For lower clock frequencies, the device clock time can be set to ensure that the maximum clock high and low time is not less than 275 ns.

7. With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start pulse is internally limited, see Figure 2 and section 2.6.

8. With a clock frequency of \( 20 \text{ MHz} \), the internal clock phase is not required before the internal clock phases are proper to start the conversion process. The start pulse is internally limited, see Figure 2 and section 2.6.

9. When using an asynchronous start pulse, the output voltage range is \( 0 \text{ VDC} \) to \( 5 \text{ VDC} \) when \( V_{CC} = 4.75 \text{ VDC} \) and \( T_A = 25^\circ \text{C} \).

10. The output voltage range is \( 0 \text{ VDC} \) to \( 5 \text{ VDC} \) when \( V_{CC} = 4.75 \text{ VDC} \) and \( T_A = 25^\circ \text{C} \).

11. In normal mode, a minimum output voltage of \( 0 \text{ VDC} \) is not required before the internal clock phases are proper to start the conversion process. The start pulse is internally limited, see Figure 2 and section 2.6.

12. In normal mode, a minimum output voltage of \( 0 \text{ VDC} \) is not required before the internal clock phases are proper to start the conversion process.
**Performance Characteristics**

---

**Logic Input Threshold Voltage vs. Supply Voltage**

---

**Delay From Falling Edge of RD to Output Data Valid vs. Load Capacitance**

---

**CLK IN Schmitt Trip Levels vs. Supply Voltage**

---

**fCLK vs. Clock Capacitor**

---

**Full-Scaling Error vs. Conversion Time**

---

**Effect of Unadjusted Offset Error vs. VREF/2 Voltage**

---

**Output Current vs. Temperature**

---

**Power Supply Current vs. Temperature (Note 9)**

---

**Linearity Error at Low VREF/2 Voltages**

---
ATE Test Circuits and Waveforms

Output Enable and Reset INTA

Note: Read strobe must occur 6 clock periods (8/Clk) after assertion of interrupt to guarantee reset of INTA.
Directly Converting a Low-Level Signal

A µP Interfaced Comparator

1 mV Resolution with µP Controlled Range

Digitizing a Current Flow
Typical Applications (Continued)

Self-Clocking Multiple A/Ds

*Use a large R value to reduce loading at CLX R output.

Self-Clocking in Free-Running Mode

*After power-up, a momentary grounding of the WR input is needed to guarantee operation.

Operating with "Automotive" Ratiometric Transducers

*Rxtol -1 = 0.15 Vcc
15% of Vcc ≥ Vref ≥ 85% of Vcc

External Clocking

100 kHz ≤ CLK ≤ 1 MHz

μP Interface for Free-Running A/D

Ratiometric with Vref/2 Forced

TLV15571-7
Typical Applications (Continued)

μP Compatible Differential-Input Comparator with Pre-Set V_{OG} (with or without Hysteresis)

*See Figure 6 to select it value
DB7 = "1" for V_{OH} (-1 + V_{OH} - 1 / 3 (V_{CC}/2)
*Dot circuitry within the dotted area if hysteresis is not needed

Handling ± 10V Analog Inputs

Low-Cost, μP Interfaced, Temperature-to-Digital Converter

μP Interfaced Temperature-to-Digital Converter

*Sensotec Instruments #684-2-R10K resistor array

*Circuit values shown are for 0°C ≤ T_A ≤ 125°C

**Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage.
Typical Applications (Continued)

Handling ±5V Analog Inputs

μP Interfaced Comparator with Hysteresis

Protecting the Input

A Low-Cost, 3-Decade Logarithmic Converter

Analog Self-Test for a System
Typical Applications (Continued)

3-Decade Logarithmic A/D Converter

A, B, C, D = LM324A

Noise Filtering the Analog Input

\[ V_{in} \times 1.1 \]

\[ V_{out} \]

\[ C = 20 \text{ Hz} \]

Uses Chebyshev implementation for steep roll off
unity-gain, 2nd order, low-pass filter
Adding a separate filter for each channel increases
system response time if an analog multiplexer
in used

Multiplexing Differential Inputs

Output Buffers with A/D Data Enabled

Increasing Bus Drive and/or Reducing Time on Bus

*A/D output data is updated 1 CLK period
prior to assertion of INTR

*Allows output data to set-up at falling edge of CS
Typical Applications (Continued)

Sampling an AC Input Signal

Note 1: Oversample whenever possible (keep fs > 2(fns - f1)) to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.
Note 2: Consider the amplitude errors which are introduced within the passband of the filter.

70% Power Savings by Clock Gating

Power Savings by A/D and VREF Shutdown

*Use A/D0001, 02, 03 or 05 for lowest power consumption.
Note: Logic inputs can be driven to VCC with A/D supply at zero volts.
Buffer prevents data bus from overdriving output of A/D when in shutdown mode.
2.4.2 Reference Accuracy Requirements
The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0803 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For $V_{REF}/2$ voltages of 2.4 $V_{OC}$ nominal value, initial errors of $\pm 10$ m$V_{OC}$ will cause conversion errors of $\pm 1$ LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ Input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ Input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (6 mV max) over 0°C$\leq T_{A} \leq +70^\circ$C. Other temperature range parts are also available.

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error
The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN(-)}$ Input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first rise of the transfer function and can be measured by grounding the $V_{IN(-)}$ Input and applying a small magnitude positive voltage to the $V_{IN(+)}$ Input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal $1/2$ LSB value ($1/2$ LSB = 9.8 mV for $V_{REF}/2 = 2.500 V_{OC}$).

2.5.2 Full-Scale
The full-scale adjustment can be made by applying a differential input voltage that is $1/2$ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the $V_{OC}$ supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.
DAC0808, DAC0807, DAC0806 8-Bit D/A Converters

General Description

The DAC0808 series is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (IREF) trimming is required for most applications since the full scale output current is typically ±1 LSB or 255 IREF/256. Relative accuracies of better than ±0.10% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for IREF ≥ 2 mA. The power supply currents of the DAC0808 series are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

Features

- Relative accuracy: ±0.10% error maximum (DAC0808)
- Full scale current match: ±1 LSB typ
- 7 and 6-bit accuracy available (DAC0807, DAC0806)
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/μs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW ± ±5V

Block and Connection Diagrams

Ordering Information

<table>
<thead>
<tr>
<th>ACCURACY</th>
<th>OPERATING RANGE</th>
<th>J PACKAGE (J16A)*</th>
<th>N PACKAGE (N16A)*</th>
<th>SO PACKAGE (M16A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GRD</td>
<td>-55°C ≤ Ta ≤ -125°C</td>
<td>DAC0808BJ/MC1508BJ</td>
<td>DAC0808BLC/MC1408BLC</td>
<td>DAC0808BLCM/MC1408BLCM</td>
</tr>
<tr>
<td>0.08%</td>
<td>0°C ≤ Ta ≤ -125°C</td>
<td>DAC0808BLJ/MC1508BLJ</td>
<td>DAC0808BLCN/MC1408BLCN</td>
<td>DAC0808BLCM/MC1408BLCM</td>
</tr>
<tr>
<td>0.08%</td>
<td>0°C ≤ Ta ≤ -125°C</td>
<td>DAC0808BLCJ/MC1408BLCJ</td>
<td>DAC0808BLCN/MC1408BLCN</td>
<td>DAC0808BLCM/MC1408BLCM</td>
</tr>
</tbody>
</table>

*Note: Devices may be ordered by using either order number.
### Absolute Maximum Ratings (Note 1)

- Storage Temperature Range: $-65°C$ to $+150°C$
- Lead Temp. (Soldering, 10 seconds): $260°C$
- Dual-In-Line Package (Ceramic): $300°C$
- Package Type: $215°C$
- Infrared (15 seconds): $220°C$

#### Power Supply Voltage
- $V_{CC} = +18$ $V_{CC}$
- $V_{EE} = -18$ $V_{CC}$

#### Digital Input Voltage, $V_{5}$-V12
- $-10$ $V_{CC}$ to $+18$ $V_{CC}$

#### Applied Output Voltage, $V_{O}$
- $-11$ $V_{CC}$ to $+18$ $V_{CC}$

#### Reference Current, $I_{R}$
- 5 mA

#### Reference Amplifier Inputs, V14, V15
- $V_{CC}$, $V_{EE}$

#### Power Dissipation (Note 3)
- 1000 mW

#### ESD Susceptibility (Note 4)
- TBD

### Electrical Characteristics

- $(V_{CC} = 5V, V_{EE} = -15V, V_{REF}/R14 = 2mA, DAC0808, T_A = -55°C$ to $+125°C, DAC0808C, DAC0807C, DAC0806C, T_A = 0°C$ to $+75°C,$ and all digital inputs at high logic level unless otherwise noted.)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_{r}$</td>
<td>Relative Accuracy (Error Relative to Full Scale)</td>
<td>$V_{CC}$</td>
<td>$\pm 0.19$</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td> </td>
<td></td>
<td>DAC0808L (LM1508-8), DAC0806LC (LM1408-8), DAC0807LC (LM1408-7), DAC0806LC (LM1408-7), (Note 5)</td>
<td>$\pm 0.39$</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td> </td>
<td></td>
<td>DAC0806L (LM1406-8), (Note 5)</td>
<td>$\pm 0.78$</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td> </td>
<td>Settling Time to Within $\frac{1}{2}$ LSB (Includes $I_{R,HL}$)</td>
<td>$T_A = 25^°C$ (Note 6), (Figure 5)</td>
<td>150</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>$I_{PLH, I_{PHL}}$</td>
<td>Propagation Delay Time</td>
<td>$T_A = 25^°C$, (Figure 5)</td>
<td>30</td>
<td>100</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>$TC_{DQ}$</td>
<td>Output Full Scale Current Drift</td>
<td></td>
<td>$\pm 20$</td>
<td></td>
<td></td>
<td>ppm/°C</td>
</tr>
<tr>
<td> </td>
<td>Digital Input Logic Levels</td>
<td>$V_{IL}$ (High Level, Logic &quot;1&quot;)</td>
<td>0</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td> </td>
<td></td>
<td>$V_{IL}$ (Low Level, Logic &quot;0&quot;)</td>
<td>0</td>
<td></td>
<td></td>
<td>mA</td>
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<tr>
<td> </td>
<td>Digital Input Current</td>
<td>$V_{IH} = V_{CC}$</td>
<td>0.040</td>
<td></td>
<td></td>
<td>mA</td>
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<tr>
<td> </td>
<td></td>
<td>$V_{IL} = 0.8V$</td>
<td>$-0.003$</td>
<td>$-0.8$</td>
<td></td>
<td>mA</td>
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<tr>
<td>$I_{R}$</td>
<td>Reference Input Bias Current</td>
<td></td>
<td>$-1$</td>
<td>$-3$</td>
<td></td>
<td>µA</td>
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<tr>
<td> </td>
<td>Output Current Range</td>
<td>$V_{EE} = -5V$</td>
<td>0</td>
<td>2.0</td>
<td>21</td>
<td>mA</td>
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<tr>
<td> </td>
<td></td>
<td>$V_{EE} = -15V, T_A = 25^°C$</td>
<td>0</td>
<td>2.0</td>
<td>4.2</td>
<td>mA</td>
</tr>
<tr>
<td> </td>
<td>Output Current, All Bits Low</td>
<td>$V_{REF} = 2.000V$, $R14 = 1000Ω$, (Figure 7)</td>
<td>1.9</td>
<td>1.99</td>
<td>2.1</td>
<td>mA</td>
</tr>
<tr>
<td> </td>
<td></td>
<td>Output Current, All Bits Low</td>
<td>0</td>
<td>4</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>Output Voltage Compliance (Note 2)</td>
<td>$E_r \leq 0.19%$, $T_A = 25^°C$</td>
<td></td>
<td>$-0.55$</td>
<td>$+0.04$</td>
<td>$V_{CC}$</td>
</tr>
<tr>
<td> </td>
<td></td>
<td>$E_r \leq 0.19%$, $T_A = 25^°C$</td>
<td></td>
<td>$-5.0$</td>
<td>$+0.04$</td>
<td>$V_{CC}$</td>
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### Electrical Characteristics (Continued)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
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<tbody>
<tr>
<td>SRL12F</td>
<td>Reference Current Slew Rate (Figure 6)</td>
<td></td>
<td>4</td>
<td>8</td>
<td></td>
<td>mA/Vs</td>
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<tr>
<td></td>
<td>Output Current Power Supply</td>
<td>$-5V \leq V_{EE} \leq -18.5V$</td>
<td>0.05</td>
<td>2.7</td>
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<td>μA/V</td>
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<tr>
<td>VCC</td>
<td>Power Supply Current (All Bits Low)</td>
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<td>2.3</td>
<td>22</td>
<td>22</td>
<td>mA</td>
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<tr>
<td></td>
<td>Power Supply Voltage Range</td>
<td>$T_A = 25^\circ C$ (Figure 3)</td>
<td>4.5</td>
<td>5.0</td>
<td>5.5</td>
<td>VDC</td>
</tr>
<tr>
<td></td>
<td>Power Dissipation</td>
<td>$V_{OC} = 5V, V_{EE} = -5V$</td>
<td>-4.5</td>
<td>-15</td>
<td>-15</td>
<td>5.0</td>
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<tr>
<td></td>
<td>All Bits High</td>
<td>$V_{OC} = 15V, V_{EE} = -15V$</td>
<td>90</td>
<td>165</td>
<td>165</td>
<td>mW</td>
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<tr>
<td></td>
<td></td>
<td>$V_{OC} = 15V, V_{EE} = -15V$</td>
<td>180</td>
<td></td>
<td></td>
<td>mW</td>
</tr>
</tbody>
</table>

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: Range control is not required.

Note 3: The maximum power dissipation must be derived at increased temperatures and is dictated by $T_{Jmax}$, $R_{thJA}$, and the ambient temperature, $T_A$. The maximum allowable power dissipation at any temperature is $P_T = (T_{Jmax} - T_A)R_{thJA}$. If the number given in the Absolute Maximum Ratings, whichever is lower. For this part, $T_{Jmax} = 125^\circ C$, and the typical junction-to-ambient thermal resistance of the dual-in-line J package when the board mounted is 100°C/W. For the dual-in-line N package, this number increases to 177°C/W and the smallest outline N package this number is 105°C/W.

Note 4: Human body model, 100 μA, discharged through a 1.5 kΩ resistor.

Note 5: All current sources are listed to guarantee at least 50% of rated current.

Note 6: All pins are switching.

Note 7: Pin-out numbers for the DAC0808 represent the dual-in-line package. The small outline package pinout differs from the dual-in-line package.

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### Typical Application

![Typical Application Diagram](image-url)

**FIGURE 1.** 10V Output Digital to Analog Converter (Note 7)