LAMPIRAN
uses dos,crt,GRAPH;
const TX = $3F;
   RX = $3F;
   LCR = $3F3;
   MSB = $3F3;
   LSB = $3F3;
   IER = $3F3;
   LSR = $3F3;
   MCR = $3F3;
   IIR = $3F3;
   ACO = $20;
   A01 = $21;
Gray50 : FillPatternType = SAA, S55, SAA, S55, SAA, S55, SAA, S55;

var r:registers;
rev:pointer;
TOM:CHAR;
data_ok, read_ok:boolean;
n,serial,pointer:byte;
gd, gm:integer;
data:array[0..10]of byte;
temp_meteran,meteran:longint;
s:string[12];
pentol:string[9];

PROCEDURE INITSER;
BEGIN
   PORT[LCR]:=128;
   PORT[MSB]:=0;
   PORT[LSB]:=12;
   PORT[LCR]:=7;
   PORTIER]:=1;
   PORT[AOI]:=32;
   PORT[LSR]:=0;
   PORT[MCR]:=$F;
END;

FUNCTION DATA_IN:BOOLEAN;
BEGIN
   IF PORT[IIR]=4 THEN DATA_IN:=TRUE ELSE DATA_IN:=FALSE;
END;

FUNCTION TX_KOSONG:BOOLEAN;
BEGIN
   IF PORT[LSR]=96 THEN TX_KOSONG:=TRUE ELSE TX_KOSONG:=FALSE;
END;

function IntToStr(I:longint):string;
var
S: string[11];
begin
  Str(I,S);
  IntToStr := S;
end;

PROCEDURE SEND(DATA:BYTE);
BEGIN
  IF TX_KOSONG THEN PORT[TX] := DATA;
  delay[10];
  END;

PROCEDURE RECEIVER; INTERRUPT;
BEGIN
  IF DATA_IN THEN
    BEGIN
      if not(read_OK) then
        begin
          serial:=PORT[RX];
          data[pointer]: = serial;
          inc(pointer);
          if pointer=7 then
            begin
              meteran := meteran div 36;
              read_ok := true;
            end;
        end;
    END;
  PORT[AOO] := $20;
  END;

BEGIN
  Gd := Detect;
  InitGraph(Gd, Gm, ' ');
  if GraphResUlt <> grOk then Halt(1);
  clrscr;
  getintvec($c, rev);
  setintvec($c, receiver);
  initser;
  repeat
    if read_ok then
      begin
        cleardevice;
        setbkcolor(black);
        SetTextStyle(1,0,7);
        setcolor(white);
        outtextxy(120, 90, 'Pemakaian : ');
        SetFillPattern(Gray50, blue);
        ...
bar 20,170,600,300);
s:='0000,0000M';
temp_meteran:=meteran;
for n:=9 downto 1 do
begin
  if n<>5 then
    begin
      pentol:=inttostr(temp_meteran mod 10);
      s[n]:=pentol[1];
      temp_meteran:=temp_meteran div 10;
    end;
end;
SetTextStyle(1,0,7);
setcolor(yellow);
outtextxy:90,170,s);
SetTextStyle(1,0,5);
setcolor(yellow);
outtextxy:530,160,'3');
pointer:=3;
read_ok:=false;
end;
if keypressed then tom:=readkey;
until tom=#27;
setintvec($c,rev);
closegraph;
end.
COUNT EQU 08H
TEMP1 EQU 09H
TEMP2 EQU 0AH
TEMP3 EQU 0BH
TEMP4 EQU 0CH
IN1 EQU 0DH
IN2 EQU 0EH
IN3 EQU 0FH
IN4 EQU 10H
VAR6 EQU 11H
VAR7 EQU 12H
VAR8 EQU 13H
VAR9 EQU 14H
VAR10 EQU 15H
VAR11 EQU 16H
VAR12 EQU 17H
VAR1 EQU 18H
VAR2 EQU 19H
VAR3 EQU 1AH
VAR4 EQU 1BH
FREE EQU 1CH
SELECT EQU 1DH
VAR5 DATA 21H
VOLUME EQU 30H
DETIK EQU 34H
MENIT EQU 35H
JAM EQU 36H
DAY EQU 37H
VOLUME_DISP EQU 38H
prescaler EQU 3CH
lcd_buff_ln1 EQU 40H
lcd_buff_ln2 EQU 50H
PRESS BIT 0
UPDATE BIT 1
BLANK BIT 2
CLOCK BIT 3
STAT_BLINK BIT 4

ORG 00H
AJMP MULAI

ORG 0BH
AJMP TMRO

ORG 13H
AJMP INT1

ORG 30H

;-----------------------------

; TIMERO
F.iun

prescaler, esc_tmr0
prescaler, #30
prescaler+1, esc_tmr0
prescaler+1, #20
prescaler+2, esc_tmr0
prescaler+2, #3
stat_blink
stat_blink, esc_tmr0
clock

---

PULSA CPU

INT1
PUSH A
INC VOLUME
MOV A, VOLUME
JNZ RUTIN_UPDATE
INC VOLUME-1
MOV A, VOLUME-1
JNZ RUTIN_UPDATE
INC VOLUME-2
MOV A, VOLUME-2
JNZ RUTIN_UPDATE
INC VOLUME-3

RUTIN_UPDATE
JB UPDATE, ESC_INT1
MOV VOLUME_DISP, VOLUME
MOV VOLUME_DISP+1, VOLUME+1
MOV VOLUME_DISP+2, VOLUME+2
MOV VOLUME_DISP+3, VOLUME+3
SETB UPDATE

ESC_INT1
POP A
RETI

---

DELAY 4 mS

delay4m
mov r7, #50
del14m
mov r6, #250
djnz r6,$
djnz r7, del14m
ret

---

delay data lcd

del_lcd
mov a, #200
djnz a,$
ret

PERPUSTAKAAN
Universitas Katolik Widya Mandala
BURABAYA
; enable pulse

enable

; CONTROL LCD

lcdcontrol mov free,a
swap a
acall enable
mov a,free
acall enable
acall del_lcd
ret

; inisialisasi led

init_lcd4bit clr p0.4
mov r5,#10
wait_lcd mov a,#3
acall enable
acall delay4m
djnz r5,wait_lcd

WAITFUNCT mov a,#2
acall enable
acall delay4m

mov a,#2fh ;FUNCTIONSET
acall lcdcontrol
mov a,#0ch ;DISPLAY ON
acall lcdcontrol
mov a,#01h ;DISPLAY CLEAR
acall lcdcontrol
mov a,#06h ;ENTRY
acall lcdcontrol
ret
; DISPLAY LCD
;--------------------------------
lcd setb p0.4
mov free,a
swap a
acall enable
acall del_lcd
mov a,free
acall enable
clr p0.4
ret

; PEMBAGIAN
;--------------------------------
BAGI
MOV A,RO
PUSH A
MOV A,R1
PUSH A
MOV A,R2
PUSH A
MOV IN1,VAR1
MOV IN2,VAR2
MOV IN3,VAR3
MOV IN4,VAR4
MOV VAR1,#0
MOV VAR2,#0
MOV VAR3,#0
MOV VAR4,#0
MOV COUNT,#64

BAGI1
CLR C
MOV A,VAR5
RLC A
MOV VAR5,A
MOV R0,#11H
MOV R2,#11
SHIFT
MOV A,@R0
RLC A
MOV @R0,A
INC R0
DJNZ R2,SHIFT
MOV TEMP1,VAR1
MOV TEMP2,VAR2
MOV TEMP3,VAR3
MOV TEMP4,VAR4
CLR C
MOV R0,#18H
MOV R1,#0DH
MOV R2,#4

; PENGURANGAN
KURANG
MOV A,@R0
SUBB A,@R1
MOV @R0,A
INC R0
INC R1
DJNZ R2,KURANG
JC CLEAR_VARBIT0

NEGATIVE
SETB VAR5,0
AJMP CEK_COUNTER

CLEAR_VARBIT0
MOV VAR1,TEMP1
MOV VAR2,TEMP2
MOV VAR3,TEMP3
MOV VAR4,TEMP4

CEK_COUNTER
DJNZ COUNT,BAGII
POP A
MOV R2,A
POP A
MOV R1,A
POP A
MOV R0,A
RET

;-----------------------------
; PERKALIAN
;-----------------------------
KALI
MOV IN1,VAR1
MOV IN2,VAR2
MOV IN3,VAR3
MOV IN4,VAR4
MOV VAR9,#0
MOV VAR10,#0
MOV VAR11,#0
MOV VAR12,#0
MOV VAR1,#0
MOV VAR2,#0
MOV VAR3,#0
MOV VAR4,#0
MOV COUNT,#32

KALII
CLR C
JNB VAR5,0,PASS2
;APAKAH Q0 = 0 ?
MOV R0,#18H
MOV R1,#0DH
MOV R2,#4

TAMBAH
MOV A,@R0
ADDC A,@R1
MOV @R0,A
INC R0
INC R1
DJNZ R2, TAMBAH
PASS2
MOV R0, #1Bh
MOV R2, #4

SHIFTR1
MOV A, @R0
RRC A
MOVC @R0, A
DEC R0
DJNZ R2, SHIFTR1
MOVC R0, #13h
MOV R2, #3

SHIFTR2
MOV A, @R0
RRC A
MOVC @R0, A
DEC R0
DJNZ R2, SHIFTR2
MOVC A, VAR5
RRC A
MOVC VAR5, A
DJNZ COUNT, KALI1

MOV VAR12, VAR4
MOV VAR11, VAR3
MOV VAR10, VAR2
MOV VAR9, VAR1
RET

;--------------------------
; PROTOCOL DISPLAY 16 CHAR
;--------------------------
protocol_lcd mov r0, a
mov free, #16
next_protocol mov a, #0
movc a, @a+dptr
inc dptr
push dph
push dpl
push free
mov @r0, a
inc r0
pop free
pop dpl
pop dph
 djnz free, next_protocol
ret

;--------------------------
; MAPING MEMORY TO LCD
;--------------------------
map_buff mov a, #80h
acall  lcdcontrol
mov  r0,#lcd_buff_ln1
mov  r7,#16
disp_11
mov  a,#r0
acall  lcd
inc  r0
djnz  r7,disp_11
mov  a,#0c0h
acall  lcdcontrol
mov  r0,#lcd_buff_ln2
mov  r7,#16
disp_12
mov  a,#r0
acall  lcd
inc  r0
djnz  r7,disp_12
ret

;-----------------------
; delay 1 second
;-----------------------
delay
mov  a,#7
delay2
mov  r7,#250
delay1
mov  r6,#250
djnz  r6,delay1
djnz  r7,delay1
djnz  a,delay2
ret

;-----------------------
; IDENTITY
;-----------------------
IDENTITY  MOV  DPTR,#NAMA
MOV  A,#LCD_BUFF_LN1
ACALL  PROTOCOL_LCD
MOV  DPTR,#NRP
MOV  A,#LCD_BUFF_LN2
ACALL  PROTOCOL_LCD
ACALL  MAP_BUFF
ACALL  DELAY
RET
NAMA  DB  ' GO KIANG DJOEN ' 
NRP  DB  ' 51030960XX '

;-----------------------
; BACKGROUND
;-----------------------
BACKGROUND  MOV  DPTR,#BACKGROUND2
MOV  A,#LCD_BUFF_LN2
ACALL  PROTOCOL_LCD
BACKGROUND2 RET DB 'TOTAL: ', 1

;-------------------------
; ALU ACTIV 4 BYTES
;-------------------------
ACTIV_4BYTE MOV VAR9,#0
MOV VAR10,#1
MOV VAR11,#1
MOV VAR12,#1
RET

;-------------------------
; DISP BCD METER AIR
;-------------------------
DISP_BCD MOV VAR1,#1
MOV VAR2,#1
MOV VAR3,#0
MOV VAR4,#1
ACALL BAG1
MOV A,VAR1
ORL A,#30H
MOV @R0,A
DEC R0
DJNZ R7,DISP_BCD
RET

;---------------------
; Routine baris 1
;---------------------
baris1 mov a,detik
mov b,#60
div ab
mov detik,b ;detik
add a,menit ;menit
mov b,#60
div ab
mov menit,b
add a,jam ;jam
mov b,#24
div ab
mov jam,b
add a,day ;hari
mov b,#7
div ab
mov day,b
mov r0,#jam ;load jam to buffe
r_lcd mov r1,#lcd_buff_ln1+8
mov r7,#3
mov a,@r0
mov b,#10
div ab
orl a,#30h
orl b,#30h
mov @r1,a
inc r1
mov lrl,a
inc r1
inc r1
djnz r7,bcd_adjust
mov lcd_buff_ln1+8+2,#3ah
mov lcd_buff_ln1+8+5,#3ah
mov dptr,#hari ;load day to buffer

mov a,day
mov b,#6
mul ab
add a,dpl
mov dpl,a
mov a,#0
addc a,dph
mov dph,a
mov r0,#1lcd_buff_ln1
mov r7,#3
get_char_hari
mov a,#0
movc a,@a+dptr
mov @r0,a
inc dptr
inc r0
djnz r7,get_char_hari
inc detik
ret

hari
  db 'Senin'
db 'Selasa'
db 'Rabu'
db 'Kamis'
db 'Jumat'
db 'Sabtu'
db 'Minggu'

;---------------
; MAIN PROGRAM
;---------------
MULAI
  MOV SP,#60H
  ACA LL INITLCD4BIT
ACALL IDENTITY
CLR PRESS
MOV R0,#VOLUME
MOV R7,#11
MOV @R0,#0
INC R0
DJNZ R7,RESET_VALUE

MOV R0,#VOLUME_disp
MOV R7,#4

INC RC
DJNZ R7,RESET_volume
mov prescaler+2,#3
MOV DETIK,#0
MOV MENIT,#4
MOV JAM,#10
mov select,#3
MOV TMOD,#22H
MOV SCON,#5CH
MOV PCON,#80H
MOV TH1,#0FAH
MOV TH1,#0FAH
SETB TR1
MOV TL0,#64
MOV TH0,#64
SETB TR0
SETB IT1
MOV IE,#86H ;ACTIF INT1 & TMRO
SETB UPDATE

JNB UPDATE,RUTIN_JAM
acall background
MOV VAR5,VOLUME_DISP
MOV VAR6,VOLUME_DISP+1
MOV VAR7,VOLUME_DISP+2
MOV VAR8,VOLUME_DISP+3
ACALL ACTIV_4BYTE
MOV VAR1,#36
MOV VAR2,#0
MOV VAR3,#0
MOV VAR4,#0
ACALL BAGI
MOV R0,#LCD_BUFF_LN2+15
MOV R7,#4
ACALL DISP_BCD
MOV R0,#LCD_BUFF_LN2+10
MOV R7,#5
ACALL DISP_BCD
JB P1.0,esc_disp_volume
mov r0,#volume_disp

RUTIN_JAM

iseb press, rutinCLOCK
inc select
mov a,select
cjne a,#5, rutinCLOCK
mov select,#0
sjmp rutinCLOCK

cek_keyset

iseb press, rutinCLOCK
mov a,select
jz rutinCLOCK
cjne a,#1, set_mnt_jam_day ;if set detik then

detik=reset

mov detik,#0
sjmp rutinCLOCK

set_mnt_jam_day

add a,#detik-1
mov r0,a
inc @r0
sjmp rutinCLOCK

no_keypress

clear press

rutinCLOCK

iseb clock, blink
acall baris1
clr clock
ajmp display

blink

iseb stat_blink, no_display
mov a,select
cjne a,#1, blink_mnt
mov lcd_buff Ln1+14,#20h
mov lcd_buff Ln1+15,#20h

blink_mnt

cjne a,#2, blink detik
mov lcd_buff Ln1+11,#20h
mov lcd_buff Ln1+12,#20h

blink_detik

cjne a,#3, blink_day
mov lcd_buff Ln1+8,#20h
mov led_buff_lnl+9,#20h
cjne a,#4,display
mov lcd_buff_lnl+0,#20h
mov lcd_buff_lnl+1,#20h
mov lcd_buff_lnl+2,#20h
mov lcd_buff_lnl+3,#20h
mov lcd_buff_lnl+4,#20h
mov lcd_buff_lnl+5,#20h
acall map_buff
ajmp DISP_METER_AIR
Features
Compatible with MCS-51™ Products
4K Bytes of In-System Reprogrammable Flash Memory
- Endurance: 1,000 Write/Erase Cycles
Fully Static Operation: 0 Hz to 24 MHz
Three-level Program Memory Lock
128 x 8-bit Internal RAM
32 Programmable I/O Lines
Two 16-bit Timer/Counters
Six Interrupt Sources
Programmable Serial Channel
Low-power Idle and Power-down Modes

Description
The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash programmable and erasable read only memory (PEROM). The device - manufactured using Atmel’s high-density nonvolatile memory technology and is compatible with the industry-standard MCS-51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash in a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides highly-flexible and cost-effective solution to many embedded control applications.

Pin Configurations

PDIP

PLCC
ock Diagram

AT89C51
The AT89C51 provides the following standard features: 4K of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit counters, a five vector two-level interrupt architecture, duplex serial port, on-chip oscillator, and clock circuit. In addition, the AT89C51 is designed with static logic operation down to zero frequency and supports two selectable power saving modes. The Idle Mode allows the CPU while allowing the RAM, timer/counters, port, and interrupt system to continue functioning. The r-down Mode saves the RAM contents but freezes oscillator disabling all other chip functions until the next reset.

Description

current voltage.

is an 8-bit open-drain bi-directional I/O port. As an input port, each pin can sink eight TTL inputs. When 1s are written to Port 0 pins, the pins can be used as high-impedance inputs.

may also be configured to be the multiplexed low-address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups, and outputs the code bytes during Flash programming, and receives the code bytes during Flash verification. External pullups are required during programming.

is an 8-bit bi-directional I/O port with internal pullups. Port 1 output buffers can sink/source four TTL inputs. 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, pins that are externally being pulled low will source current (Ih) because of the internal pullups.

also receives the low-order address bytes during programming and verification.

is an 8-bit bi-directional I/O port with internal pullups. Port 2 output buffers can sink/source four TTL inputs. 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (Ih) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

is an 8-bit bi-directional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (Ih) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

<table>
<thead>
<tr>
<th>Port Pin</th>
<th>Alternate Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>P3.0</td>
<td>RXD (serial input port)</td>
</tr>
<tr>
<td>P3.1</td>
<td>TXD (serial output port)</td>
</tr>
<tr>
<td>P3.2</td>
<td>INTO (external interrupt 0)</td>
</tr>
<tr>
<td>P3.3</td>
<td>INT1 (external interrupt 1)</td>
</tr>
<tr>
<td>P3.4</td>
<td>T0 (timer 0 external input)</td>
</tr>
<tr>
<td>P3.5</td>
<td>T1 (timer 1 external input)</td>
</tr>
<tr>
<td>P3.6</td>
<td>WR (external data memory write strobe)</td>
</tr>
<tr>
<td>P3.7</td>
<td>RD (external data memory read strobe)</td>
</tr>
</tbody>
</table>

Port 3 also receives some control signals for Flash programming and verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/PROG

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE
is skipped during each access to external Data memory. ALE operation can be disabled by setting bit 0 of location 8EH. With the bit set, ALE is active only during MOVX or MOVC instruction. Otherwise, the pin is not pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

RAM Store Enable is the read strobe to external program memory. When the AT89C51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during access to external data memory.

PPN. Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. However, that if lock bit 1 is programmed, EA will be always latched on reset. It should be strapped to Vcc for internal program options. The 12-volt programming enable voltage (Vpp) during Flash programming, for parts that require Vpp.

1 to the inverting oscillator amplifier and input to the clock operating circuit.

2 from the inverting oscillator amplifier.

illator Characteristics

1 and XTAL2 are the input and output, respectively, to an external clock source. XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections

Note: C1 > 10 pF for Crystals
C2 > 10 pF for Ceramic Resonators

Class C1, C2 = 30 pF ± 10 pF for Crystals
50 pF ± 10 pF for Ceramic Resonators

Table: AT89C51

<table>
<thead>
<tr>
<th>Program Memory</th>
<th>ALE</th>
<th>PSEN</th>
<th>PORT0</th>
<th>PORT1</th>
<th>PORT2</th>
<th>PORT3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal</td>
<td>1</td>
<td>1</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
<tr>
<td>External</td>
<td>1</td>
<td>1</td>
<td>Float</td>
<td>Data</td>
<td>Address</td>
<td>Data</td>
</tr>
<tr>
<td>r-down Internal</td>
<td>0</td>
<td>0</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
<tr>
<td>r-down External</td>
<td>0</td>
<td>0</td>
<td>Float</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
</tbody>
</table>
2. External Clock Drive Configuration

- **NC**
- XTAL2

EXTERNAL OSCILLATOR SIGNAL

XTAL1

GND

**Power-down Mode**

In power-down mode, the oscillator is stopped, and the action that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. The only exit from power-down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before $V_{CC}$ is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

**Program Memory Lock Bits**

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below.

When lock bit 1 is programmed, the logic level at the $EA$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $EA$ be in agreement with the current logic level at that pin in order for the device to function properly.

**Lock Bit Protection Modes**

<table>
<thead>
<tr>
<th>Program Lock Bits</th>
<th>Protection Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>LB1</td>
<td>LB2</td>
</tr>
<tr>
<td>1</td>
<td>U</td>
</tr>
<tr>
<td>2</td>
<td>P</td>
</tr>
<tr>
<td>3</td>
<td>P</td>
</tr>
<tr>
<td>4</td>
<td>P</td>
</tr>
</tbody>
</table>

- Mode 2: MOVc instructions executed from external program memory are disabled from fetching code bytes from internal memory. $EA$ is sampled and latched on reset, and further programming of the Flash is disabled.
- Mode 3: Same as mode 2, also verify is disabled.
- Mode 4: Same as mode 3, also external execution is disabled.
Programming the Flash

AT89C51 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) ready to be programmed. The programming interface is either a high-voltage (12-volt) or a low-voltage program enable signal. The low-voltage programming mode provides a convenient way to program the C51 inside the user’s system, while the high-voltage programming mode is compatible with conventional third-Flash or EPROM programmers.

AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective device marking and device signature codes are listed in the following table.

<table>
<thead>
<tr>
<th>Side Mark</th>
<th>V_{pp} = 12V</th>
<th>V_{pp} = 5V</th>
</tr>
</thead>
<tbody>
<tr>
<td>AT89C51</td>
<td>AT89C51</td>
<td>AT89C51</td>
</tr>
<tr>
<td>xxxx</td>
<td>xxxx-5</td>
<td>yyyy</td>
</tr>
<tr>
<td>yyyy</td>
<td>yyyy</td>
<td>yyyy</td>
</tr>
</tbody>
</table>

T89C51 code memory array is programmed byte-by-byte in either programming mode. To program any non-byte in the on-chip Flash Memory, the entire memory be erased using the Chip Erase Mode.

Programming Algorithm: Before programming the C51, the address, data and control signals should be according to the Flash programming mode table and Figure 3 and Figure 4. To program the AT89C51, take the following steps:

1. Put the desired memory location on the address lines.
2. Put the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise EA/V_{pp} to 12V for the high-voltage programming mode.
5. Use ALE/PROG once to program a byte in the flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89C51 features Data Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on P0.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/BSY output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/PROG low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

- (030H) = 1EH indicates manufactured by Atmel
- (031H) = 51H indicates 89C51
- (032H) = FFH indicates 12V programming
- (032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.
**Flash Programming Modes**

<table>
<thead>
<tr>
<th>Mode</th>
<th>RST</th>
<th>PSEN</th>
<th>ALE/PROG</th>
<th>EA/Vpp</th>
<th>P2.6</th>
<th>P2.7</th>
<th>P3.6</th>
<th>P3.7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code Data</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>Code Data</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H/12V</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>Lock</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H/12V</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>Bit - 1</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>Bit - 3</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>Erase</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>Signature Byte</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
</tbody>
</table>

1. Chip Erase requires a 10 ms PROG pulse.

---

**Figure 4. Verifying the Flash**

---

**Figure 4. Verifying the Flash**

---

**Figure 4. Verifying the Flash**

---

**Figure 4. Verifying the Flash**

---

**Figure 4. Verifying the Flash**

---
h Programming and Verification Waveforms - High-voltage Mode ($V_{pp} = 12V$)

1.0 - P1.7  
2.0 - P2.3

PORT 0  
ALE/PROG  
EA/V_{pp}  
P2.7 (ENABLE)  
P3.4 (RDY/BSY)  

---

h Programming and Verification Waveforms - Low-voltage Mode ($V_{pp} = 5V$)

1.0 - P1.7  
2.0 - P2.3

PORT 0  
ALE/PROG  
EA/V_{pp}  
P2.7 (ENABLE)  
P3.4 (RDY/BSY)  

AT89C51
## AT89C51

### Programming and Verification Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Programming Enable Voltage</td>
<td>11.5</td>
<td>12.5</td>
<td>V</td>
</tr>
<tr>
<td>Programming Enable Current</td>
<td></td>
<td>1.0</td>
<td>mA</td>
</tr>
<tr>
<td>Oscillator Frequency</td>
<td>3</td>
<td>24</td>
<td>MHz</td>
</tr>
<tr>
<td>Address Setup to PROG Low</td>
<td>48tCLCL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Address Hold After PROG</td>
<td>48tCLCL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data Setup to PROG Low</td>
<td>48tCLCL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data Hold After PROG</td>
<td>48tCLCL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>P2.7 (ENABLE) High to VPP</td>
<td>48tCLCL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VPP Setup to PROG Low</td>
<td>10</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>VPP Hold After PROG</td>
<td>10</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>PROG Width</td>
<td>1</td>
<td>110</td>
<td>µs</td>
</tr>
<tr>
<td>Address to Data Valid</td>
<td>48tCLCL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ENABLE Low to Data Valid</td>
<td>48tCLCL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data Float After ENABLE</td>
<td>0</td>
<td>48tCLCL</td>
<td></td>
</tr>
<tr>
<td>PROG High to BUSY Low</td>
<td>1.0</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Byte Write Cycle Time</td>
<td>2.0</td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>

1. Only used in 12-volt programming mode.
**Absolute Maximum Ratings**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input Low-voltage</strong></td>
<td>(Except EA)</td>
<td>-0.5</td>
<td>0.2 Vcc</td>
<td>V</td>
</tr>
<tr>
<td><strong>Input Low-voltage (EA)</strong></td>
<td></td>
<td>-0.5</td>
<td>0.2 Vcc</td>
<td>V</td>
</tr>
<tr>
<td><strong>Input High-voltage</strong></td>
<td>(Except XTAL1, RST)</td>
<td>0.2 Vcc</td>
<td>0.9 Vcc</td>
<td>V</td>
</tr>
<tr>
<td><strong>Input High-voltage (XTAL1, RST)</strong></td>
<td></td>
<td>0.7 Vcc</td>
<td>Vcc + 0.5</td>
<td>V</td>
</tr>
<tr>
<td><strong>Output Low-voltage</strong> (Ports 1, 2, 3)</td>
<td></td>
<td>I&lt;sub&gt;OL&lt;/sub&gt; = 1.6 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Output Low-voltage</strong> (Port 0, ALE, PSEN)</td>
<td></td>
<td>I&lt;sub&gt;OL&lt;/sub&gt; = 3.2 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Output High-voltage</strong> (Ports 1, 2, 3, ALE, PSEN)</td>
<td></td>
<td>I&lt;sub&gt;OH&lt;/sub&gt; = 100 µA, VCC = 5 V -10%</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Output High-voltage</strong> (Port 0 in External Bus Mode)</td>
<td></td>
<td>I&lt;sub&gt;OH&lt;/sub&gt; = 200 µA, VCC = 5 V -10%</td>
<td>2.4</td>
<td>V</td>
</tr>
<tr>
<td><strong>Logical 0 Input Current</strong> (Ports 1, 2, 3)</td>
<td></td>
<td>V&lt;sub&gt;IH&lt;/sub&gt; = 0.45 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Logical 1 Input Current</strong> (Ports 1, 2, 3)</td>
<td></td>
<td>V&lt;sub&gt;IH&lt;/sub&gt; = 2 V, VCC = 5 V ± 10%</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Input Leakage Current</strong> (Port 0, EA)</td>
<td></td>
<td>0.45 ≤ V&lt;sub&gt;IL&lt;/sub&gt; ≤ V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTICE:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Characteristics

**-40°C to 85°C, V<sub>CC</sub> = 5.0V ± 20% (unless otherwise noted)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Test Proc.</strong></td>
<td>V&lt;sub&gt;I&lt;/sub&gt;&lt;sub&gt;CC&lt;/sub&gt; = 25°C</td>
<td>10</td>
<td>10</td>
<td>pF</td>
</tr>
<tr>
<td><strong>Active Mode</strong></td>
<td>V&lt;sub&gt;I&lt;/sub&gt;&lt;sub&gt;CC&lt;/sub&gt; = 2.7 V</td>
<td>20</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td><strong>V&lt;sub&gt;CC&lt;/sub&gt; = 2 V</strong></td>
<td></td>
<td>100</td>
<td>40</td>
<td>µA</td>
</tr>
</tbody>
</table>

1. Under steady state (non-transient) conditions, I<sub>IL</sub> must be externally limited as follows:
   - Maximum I<sub>IL</sub> per port pin: 10 mA
   - Maximum I<sub>IL</sub> per 8-bit port: Port 0: 26 mA
   - Ports 1, 2, 3: 10 mA
   - Maximum total I<sub>IL</sub> for all output pins: 10 mA
   - If I<sub>IL</sub> exceeds the listed conditions, V<sub>IL</sub> may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V<sub>CC</sub> for Power-down is 2V.
AT89C51

Characteristics

Operating conditions, load capacitance for Port 0, ALE/PROG, and PSEN = 100 pF; load capacitance for all others = 80 pF.

Internal Program and Data Memory Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>12 MHz Oscillator</th>
<th>16 to 24 MHz Oscillator</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscillator Frequency</td>
<td>Min 0</td>
<td>Max 24</td>
<td>MHz</td>
</tr>
<tr>
<td>ALE Pulse Width</td>
<td>127</td>
<td>2(t_{\text{CLKL}})-40</td>
<td>ns</td>
</tr>
<tr>
<td>Address Valid to ALE Low</td>
<td>43</td>
<td>3(t_{\text{CLKL}})-13</td>
<td>ns</td>
</tr>
<tr>
<td>Address Hold After ALE Low</td>
<td>48</td>
<td>(2t_{\text{CLKL}})</td>
<td>ns</td>
</tr>
<tr>
<td>ALE Low to Valid Instruction In</td>
<td>233</td>
<td>4(t_{\text{CLKL}})-65</td>
<td>ns</td>
</tr>
<tr>
<td>ALE Low to PSEN Low</td>
<td>43</td>
<td>(t_{\text{CLKL}})-13</td>
<td>ns</td>
</tr>
<tr>
<td>PSEN Pulse Width</td>
<td>205</td>
<td>(3t_{\text{CLKL}})-20</td>
<td>ns</td>
</tr>
<tr>
<td>PSEN Low to Valid Instruction In</td>
<td>145</td>
<td>(3t_{\text{CLKL}})-45</td>
<td>ns</td>
</tr>
<tr>
<td>Input Instruction Hold After PSEN</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>Input Instruction Float After PSEN</td>
<td>59</td>
<td>(t_{\text{CLKL}})-10</td>
<td>ns</td>
</tr>
<tr>
<td>PSEN to Address Valid</td>
<td>75</td>
<td>(t_{\text{CLKL}})-8</td>
<td>ns</td>
</tr>
<tr>
<td>Address to Valid Instruction In</td>
<td>312</td>
<td>(5t_{\text{CLKL}})-55</td>
<td>ns</td>
</tr>
<tr>
<td>PSEN Low to Address Float</td>
<td>10</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>RD Pulse Width</td>
<td>400</td>
<td>(6t_{\text{CLKL}})-100</td>
<td>ns</td>
</tr>
<tr>
<td>WR Pulse Width</td>
<td>400</td>
<td>(6t_{\text{CLKL}})-100</td>
<td>ns</td>
</tr>
<tr>
<td>RD Low to Valid Data In</td>
<td>252</td>
<td>(5t_{\text{CLKL}})-90</td>
<td>ns</td>
</tr>
<tr>
<td>Data Hold After RD</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>Data Float After RD</td>
<td>97</td>
<td>(2t_{\text{CLKL}})-28</td>
<td>ns</td>
</tr>
<tr>
<td>ALE Low to Valid Data In</td>
<td>517</td>
<td>(8t_{\text{CLKL}})-150</td>
<td>ns</td>
</tr>
<tr>
<td>Address to Valid Data in</td>
<td>585</td>
<td>(9t_{\text{CLKL}})-165</td>
<td>ns</td>
</tr>
<tr>
<td>ALE Low to RD or WR Low</td>
<td>200</td>
<td>(3t_{\text{CLKL}})-50</td>
<td>ns</td>
</tr>
<tr>
<td>Address to RD or WR Low</td>
<td>203</td>
<td>(3t_{\text{CLKL}})-75</td>
<td>ns</td>
</tr>
<tr>
<td>Data Valid to WR Transition</td>
<td>23</td>
<td>(t_{\text{CLKL}})-20</td>
<td>ns</td>
</tr>
<tr>
<td>Data Valid to WR High</td>
<td>433</td>
<td>(7t_{\text{CLKL}})-120</td>
<td>ns</td>
</tr>
<tr>
<td>Data Hold After WR</td>
<td>33</td>
<td>(t_{\text{CLKL}})-20</td>
<td>ns</td>
</tr>
<tr>
<td>RD Low to Address Float</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>RD or WR High to ALE High</td>
<td>43</td>
<td>123</td>
<td>ns</td>
</tr>
</tbody>
</table>
AT89C51

External Program Memory Read Cycle

External Data Memory Read Cycle
**External Data Memory Write Cycle**

- **ALE**
- **PSEN**
- **WR**

**PORT 0**
- A0 - A7 FROM RI OR DPL
- DATA OUT
- A0 - A7 FROM PCL
- INSTR IN

**PORT 2**
- P2.0 - P2.7 OR A8 - A15 FROM DPH
- A8 - A15 FROM PCH

**External Clock Drive Waveforms**

- $V_{CC} - 0.5V$
- $0.7V_{CC}$
- $0.2V_{CC} - 0.1V$

**External Clock Drive**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscillator Frequency</td>
<td>0</td>
<td>24</td>
<td>MHz</td>
</tr>
<tr>
<td>Clock Period</td>
<td>41.6</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>High Time</td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Low Time</td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Rise Time</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Fall Time</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

**ATMEL**
Serial Port Timing: Shift Register Mode Test Conditions

= 5.0 V ± 20%; Load Capacitance = 80 pF

<table>
<thead>
<tr>
<th>mbol</th>
<th>Parameter</th>
<th>12 MHz Osc Min</th>
<th>12 MHz Osc Max</th>
<th>Variable Oscillator Min</th>
<th>Variable Oscillator Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cl</td>
<td>Serial Port Clock Cycle Time</td>
<td>1.0</td>
<td>12τCLC1</td>
<td>ns</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>XH</td>
<td>Output Data Setup to Clock Rising Edge</td>
<td>700</td>
<td>10τCLC1-133</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>QX</td>
<td>Output Data Hold After Clock Rising Edge</td>
<td>50</td>
<td>2τCLC1-117</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DX</td>
<td>Input Data Hold After Clock Rising Edge</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DN</td>
<td>Clock Rising Edge to Input Data Valid</td>
<td>700</td>
<td>10τCLC1-133</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Shift Register Mode Timing Waveforms

Testing Input/Output Waveforms (1)

AC Inputs during testing are driven at VCC - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at Vih min. for a logic 1 and Vil max. for a logic 0.

Float Waveforms (1)

Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded VOH/VOL level occurs.
# AT89C51 Ordering Information

<table>
<thead>
<tr>
<th>Speed (MHz)</th>
<th>Power Supply</th>
<th>Ordering Code</th>
<th>Package</th>
<th>Operation Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>5V ± 20%</td>
<td>AT89C51-12AC</td>
<td>44A</td>
<td>Commercial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12JC</td>
<td>44J</td>
<td>(0°C to 70°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12PC</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12QC</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12AI</td>
<td>44A</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12JI</td>
<td>44J</td>
<td>(-40°C to 85°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12PI</td>
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<td>AT89C51-12QI</td>
<td>44Q</td>
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<tr>
<td>16</td>
<td>5V ± 20%</td>
<td>AT89C51-16AC</td>
<td>44A</td>
<td>Commercial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16JC</td>
<td>44J</td>
<td>(0°C to 70°C)</td>
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<td>AT89C51-16AI</td>
<td>44A</td>
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</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16JI</td>
<td>44J</td>
<td>(-40°C to 85°C)</td>
</tr>
<tr>
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<td>AT89C51-16QI</td>
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<tr>
<td>20</td>
<td>5V ± 20%</td>
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<td>44J</td>
<td>(0°C to 70°C)</td>
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<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20AI</td>
<td>44A</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20JI</td>
<td>44J</td>
<td>(-40°C to 85°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20PI</td>
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<td>AT89C51-20QI</td>
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<td></td>
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<tr>
<td>24</td>
<td>5V ± 20%</td>
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<td>44A</td>
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<td></td>
<td></td>
<td>AT89C51-24JC</td>
<td>44J</td>
<td>(0°C to 70°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24PC</td>
<td>40P6</td>
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<td>AT89C51-24QC</td>
<td>44Q</td>
<td></td>
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<td>AT89C51-24AI</td>
<td>44A</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24JI</td>
<td>44J</td>
<td>(-40°C to 85°C)</td>
</tr>
<tr>
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<td></td>
<td>AT89C51-24PI</td>
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<td></td>
<td>AT89C51-24QI</td>
<td>44Q</td>
<td></td>
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</table>

## Package Type

- 44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
- 44-lead, Plastic J-Leaded Chip Carrier (PLCC)
- 40-lead, 0.600" Wide, Plastic Dual In-line Package (PDIP)
- 44-lead, Plastic Gull Wing Quad Flatpack (PQFP)
kaging Information

**44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flatpack (TQFP)**
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-026 ACB

**44J, 44-lead, Plastic J-leded Chip Carrier (PLCC)**
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AC

**44Q, 44-lead, Plastic Quad Flat Package (PQFP)**
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-022 AB

---

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0265G-02/004M
TLC272, TLC272A, TLC272B, TLC272Y, TLC277
LinCMOS™ PRECISION DUAL OPERATIONAL AMPLIFIERS

- Trimming Offset Voltage:
  TLC277 . . . 500 µV Max at 25°C, VDD = 5 V
- Input Offset Voltage Drift . . . Typically 0.1 µV/Month, Including the First 30 Days
- Wide Range of Supply Voltages Over Specified Temperature Range:
  0°C to 70°C: . . . 3 V to 16 V
  -40°C to 85°C: . . . 4 V to 16 V
  -55°C to 125°C: . . . 4 V to 16 V
- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)
- Low Noise . . . Typically 25 nV/√Hz at f = 1 kHz
- Output Voltage Range Includes Negative Rail
- High Input Impedance . . . 10¹² Ω Typ
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel
- Designed-in Latch-Up Immunity

description

The TLC272 and TLC277 precision dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching those of general-purpose BiFET devices.

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias current, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for BiFET and NFET products. Four offset voltage grades are available (C-suffix and I-suffix types) ranging from the low-cost TLC272 (10 mV) to the high-precision TLC277 (500 µV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

LinCMOS is a trademark of Texas Instruments.

DISTRIBUTION OF TLC277 INPUT OFFSET VOLTAGE

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LinCMOS is a trademark of Texas Instruments.
**TLC272, TLC272A, TLC272B, TLC272Y, TLC277**

**LinCMOS™ PRECISION DUAL OPERATIONAL AMPLIFIERS**


description (continued)

### AVAILABLE OPTIONS

<table>
<thead>
<tr>
<th>TA</th>
<th>$V_{O\text{max}}$ AT 25°C</th>
<th>SMALL OUTLINE</th>
<th>CHIP CARRIER</th>
<th>CERAMIC DIP</th>
<th>PLASTIC DIP</th>
<th>TSSOP</th>
<th>CHIP FORM</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>(D)</td>
<td>(FK)</td>
<td>(JG)</td>
<td>(P)</td>
<td></td>
<td>(Y)</td>
</tr>
<tr>
<td>0°C to 70°C</td>
<td>500 µV</td>
<td>TLC277CD</td>
<td>—</td>
<td>—</td>
<td>TLC277CP</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>2 mV</td>
<td>TLC272BCD</td>
<td>—</td>
<td>—</td>
<td>TLC272BCP</td>
<td>—</td>
<td>—</td>
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<tr>
<td></td>
<td>5 mV</td>
<td>TLC272ACD</td>
<td>—</td>
<td>—</td>
<td>TLC272ACP</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>10 mV</td>
<td>TLC272CD</td>
<td>—</td>
<td>—</td>
<td>TLC272CP</td>
<td>TLC272CFW</td>
<td>TLC272Y</td>
</tr>
<tr>
<td>-40°C to 85°C</td>
<td>500 µV</td>
<td>TLC277ID</td>
<td>—</td>
<td>—</td>
<td>TLC277IP</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>2 mV</td>
<td>TLC272BID</td>
<td>—</td>
<td>—</td>
<td>TLC272BIP</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>5 mV</td>
<td>TLC272AID</td>
<td>—</td>
<td>—</td>
<td>TLC272AIP</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>10 mV</td>
<td>TLC272ID</td>
<td>—</td>
<td>—</td>
<td>TLC272IP</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC277CDR).

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC272 and TLC277. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand $-100$-mA surge currents without sustaining latch-up.

The TLC272 and TLC277 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from -40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of -55°C to 125°C.
TLC272Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC272C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS

CHIP THICKNESS: 15 TYPICAL
BONDING PADS: 4 x 4 MINIMUM
Tₘₐₓ = 155°C
TOLERANCES ARE ±10%.
ALL DIMENSIONS ARE IN MILS.
PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

- Supply voltage, \( V_{DD} \) (see Note 1) ............................................................ 18 V
- Differential input voltage, \( V_{DD} \) (see Note 2) ................................................... ±\( V_{DD} \)
- Input voltage range, \( V_I \) (any input) ................................................... -0.3 V to \( V_{DD} \)
- Input current, \( I_I \) .......................................................................... ±5 mA
- Output current, \( I_O \) (each output) ........................................................... ±30 mA
- Total current into \( V_{DD} \) .................................................................... 45 mA
- Total current out of GND ........................................................................ 45 mA
- Duration of short-circuit current at (or below) 25°C (see Note 3) .............................. unlimited
- Continuous total dissipation .................................................................. See Dissipation Rating Table
- Operating free-air temperature, \( TA \): C suffix ........................................... 0°C to 70°C
  I suffix ........................................................................... -40°C to 85°C
  M suffix ........................................................................... -55°C to 125°C
- Storage temperature range ..................................................................... -65°C to 150°C
- Case temperature for 60 seconds: FK package ........................................ 260°C
- Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package 260°C
- Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: JG package .......... 300°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

OTES: 1. All voltage values, except differential voltages, are with respect to network ground.

2. Differential voltages are at IN- with respect to IN+.

3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

Dissipation Rating Table

<table>
<thead>
<tr>
<th>PACKAGE</th>
<th>( TA = 25°C ) POWER RATING</th>
<th>DERATING FACTOR ABOVE ( TA = 25°C )</th>
<th>( TA = 70°C ) POWER RATING</th>
<th>( TA = 85°C ) POWER RATING</th>
<th>( TA = 125°C ) POWER RATING</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>725 mW</td>
<td>5.6 mW/°C</td>
<td>464 mW</td>
<td>377 mW</td>
<td>N/A</td>
</tr>
<tr>
<td>FK</td>
<td>1375 mW</td>
<td>11 mW/°C</td>
<td>850 mW</td>
<td>715 mW</td>
<td>275 mW</td>
</tr>
<tr>
<td>JG</td>
<td>1050 mW</td>
<td>8.4 mW/°C</td>
<td>672 mW</td>
<td>546 mW</td>
<td>210 mW</td>
</tr>
<tr>
<td>P</td>
<td>1000 mW</td>
<td>8.0 mW/°C</td>
<td>640 mW</td>
<td>520 mW</td>
<td>N/A</td>
</tr>
<tr>
<td>PW</td>
<td>525 mW</td>
<td>4.2 mW/°C</td>
<td>335 mW</td>
<td>N/A</td>
<td>N/A</td>
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commended operating conditions

<table>
<thead>
<tr>
<th></th>
<th>C SUFFIX</th>
<th>I SUFFIX</th>
<th>M SUFFIX</th>
<th>UNIT</th>
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<tbody>
<tr>
<td>( V_{DD} )</td>
<td>MIN</td>
<td>MAX</td>
<td>MIN</td>
<td>MAX</td>
</tr>
<tr>
<td>( V_{DD} = 5 ) V</td>
<td>5</td>
<td>10</td>
<td>4</td>
<td>10</td>
</tr>
<tr>
<td>( V_{DD} = 10 ) V</td>
<td>-0.2</td>
<td>3.5</td>
<td>-0.2</td>
<td>3.5</td>
</tr>
<tr>
<td>( TA )</td>
<td>0</td>
<td>70</td>
<td>-40</td>
<td>85</td>
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</table>

Texas Instruments
##电气特性

###输入偏置电压

<table>
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<th>参数</th>
<th>测试条件</th>
<th>温度范围</th>
<th>TLC272C, TLC272AC, TLC272BC, TLC277C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IO}$</td>
<td>$V_O = 1.4 V, R_S = 50 \Omega, R_L = 10 \text{ k}\Omega$</td>
<td>$25^\circ C$</td>
<td>1.1 mV</td>
</tr>
<tr>
<td></td>
<td>$V_{IC} = 0$</td>
<td>Full range</td>
<td>10 mV</td>
</tr>
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</table>

###温度系数

<table>
<thead>
<tr>
<th>参数</th>
<th>测试条件</th>
<th>温度范围</th>
<th>TLC272C, TLC272AC, TLC272BC, TLC277C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\alpha_{V_{IO}}$</td>
<td>$V_O = 2.5 V$</td>
<td>$25^\circ C$ to $70^\circ C$</td>
<td>1.6 $\mu V/\circ C$</td>
</tr>
</tbody>
</table>

###输入偏置电流

<table>
<thead>
<tr>
<th>参数</th>
<th>测试条件</th>
<th>温度范围</th>
<th>TLC272C, TLC272AC, TLC272BC, TLC277C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{IO}$</td>
<td>$V_O = 2.5 V$</td>
<td>$25^\circ C$</td>
<td>0.1 nA</td>
</tr>
<tr>
<td></td>
<td>$V_{IC} = 2.5 V$</td>
<td>$70^\circ C$</td>
<td>60 nA</td>
</tr>
</tbody>
</table>

###输入偏置电流

<table>
<thead>
<tr>
<th>参数</th>
<th>测试条件</th>
<th>温度范围</th>
<th>TLC272C, TLC272AC, TLC272BC, TLC277C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{IB}$</td>
<td>$V_O = 2.5 V$</td>
<td>$25^\circ C$</td>
<td>0.1 nA</td>
</tr>
<tr>
<td></td>
<td>$V_{IC} = 2.5 V$</td>
<td>$70^\circ C$</td>
<td>60 nA</td>
</tr>
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###共模输入电压范围

<table>
<thead>
<tr>
<th>参数</th>
<th>测试条件</th>
<th>温度范围</th>
<th>TLC272C, TLC272AC, TLC272BC, TLC277C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{ICR}$</td>
<td>$V_O = 1.4 V, R_S = 50 \Omega, R_L = 10 \text{ k}\Omega$</td>
<td>$25^\circ C$</td>
<td>-0.2 V</td>
</tr>
<tr>
<td></td>
<td>$V_{IC} = 0$</td>
<td>Full range</td>
<td>4.2 V</td>
</tr>
</tbody>
</table>

###高电平输出电压

<table>
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<th>参数</th>
<th>测试条件</th>
<th>温度范围</th>
<th>TLC272C, TLC272AC, TLC272BC, TLC277C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>$V_{IO} = 100 \text{ mV}, R_L = 10 \text{ k}\Omega$</td>
<td>$25^\circ C$</td>
<td>3.2 V</td>
</tr>
<tr>
<td></td>
<td>$V_O = 2.5 V$</td>
<td>$0^\circ C$</td>
<td>3.5 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$70^\circ C$</td>
<td>3.6 V</td>
</tr>
</tbody>
</table>

###低电平输出电压

<table>
<thead>
<tr>
<th>参数</th>
<th>测试条件</th>
<th>温度范围</th>
<th>TLC272C, TLC272AC, TLC272BC, TLC277C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OL}$</td>
<td>$V_{IO} = -100 \text{ mV}, I_{OL} = 0$</td>
<td>$25^\circ C$</td>
<td>0 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$0^\circ C$</td>
<td>0 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$70^\circ C$</td>
<td>0 mV</td>
</tr>
</tbody>
</table>

###共模输入电压

<table>
<thead>
<tr>
<th>参数</th>
<th>测试条件</th>
<th>温度范围</th>
<th>TLC272C, TLC272AC, TLC272BC, TLC277C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_{V_{OD}}$</td>
<td>$V_O = 0.25 V$ to $2 V, R_L = 10 \text{ k}\Omega$</td>
<td>$25^\circ C$</td>
<td>5 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$0^\circ C$</td>
<td>7 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$70^\circ C$</td>
<td>20 V</td>
</tr>
</tbody>
</table>

###共模输入电压

<table>
<thead>
<tr>
<th>参数</th>
<th>测试条件</th>
<th>温度范围</th>
<th>TLC272C, TLC272AC, TLC272BC, TLC277C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$CMRR$</td>
<td>$V_{IC} = V_{ICR}$</td>
<td>$-25^\circ C$</td>
<td>65 dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-25^\circ C$</td>
<td>80 dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-25^\circ C$</td>
<td>3.5 dB</td>
</tr>
</tbody>
</table>

###共模输入电压

<table>
<thead>
<tr>
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<th>TLC272C, TLC272AC, TLC272BC, TLC277C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$KSVR$</td>
<td>$V_{DD} = 5 V$ to $12 V, V_{IO} = 1.4 V$</td>
<td>$25^\circ C$</td>
<td>60 dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$0^\circ C$</td>
<td>60 dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$70^\circ C$</td>
<td>65 dB</td>
</tr>
</tbody>
</table>

###电流消耗

<table>
<thead>
<tr>
<th>参数</th>
<th>测试条件</th>
<th>温度范围</th>
<th>TLC272C, TLC272AC, TLC272BC, TLC277C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$IDD$</td>
<td>$V_O = -0.2 V, V_{IO} = 5 V$</td>
<td>$25^\circ C$</td>
<td>1.4 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$0^\circ C$</td>
<td>1.8 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$70^\circ C$</td>
<td>2.6 mA</td>
</tr>
</tbody>
</table>

###注意事项

1. 全范围是指0°C到70°C。
2. 《Texas Instruments》
3. 高级物料与上面的电路相关。
The table lists the electrical characteristics of TLC272, TLC272A, TLC272B, TLC272Y, and TLC277 LinCMOS™ Precision Dual Operational Amplifiers. The characteristics are measured at specified free-air temperature, $V_{DD} = 10\,\text{V}$ (unless otherwise noted). The table includes test conditions, parameter values, and units for parameters such as input offset voltage ($V_{IO}$), temperature coefficient of input offset voltage ($AVIO$), input offset current ($I_{IO}$), input bias current ($I_{IB}$), common-mode input voltage range ($V_{CMR}$), high-level output voltage ($V_{OH}$), low-level output voltage ($V_{OL}$), large-signal differential voltage amplification ($AVD$), common-mode rejection ratio ($CMRR$), supply-voltage rejection ratio ($SVRR$), and supply current ($I_{sup}$). The table also includes temperature ranges and voltage levels for the parameters.

**NOTES:**
4. The typical values of input bias current and input offset current below $5\,\mu\text{A}$ were determined mathematically.
5. This range also applies to each input individually.
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