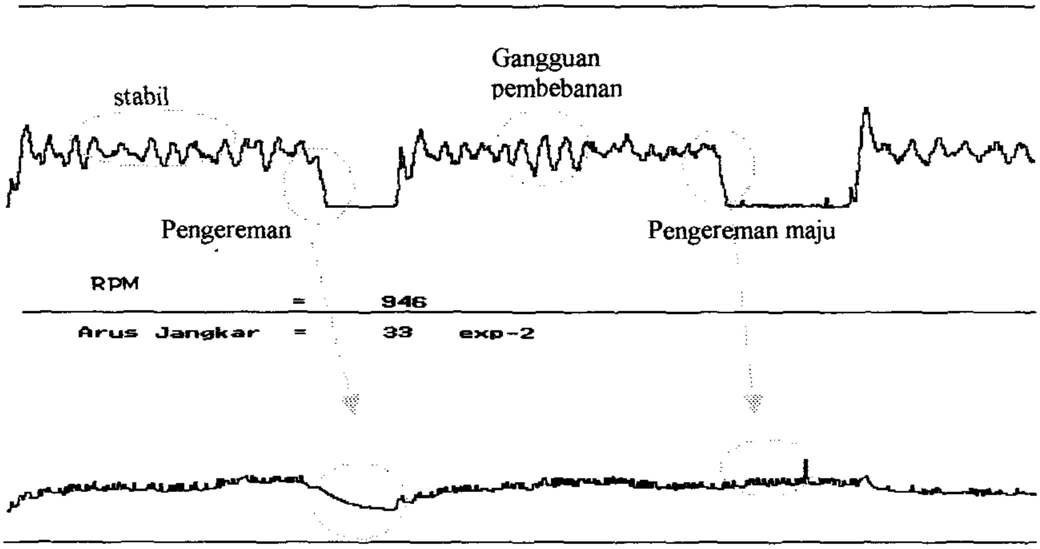
LAMPIRAN

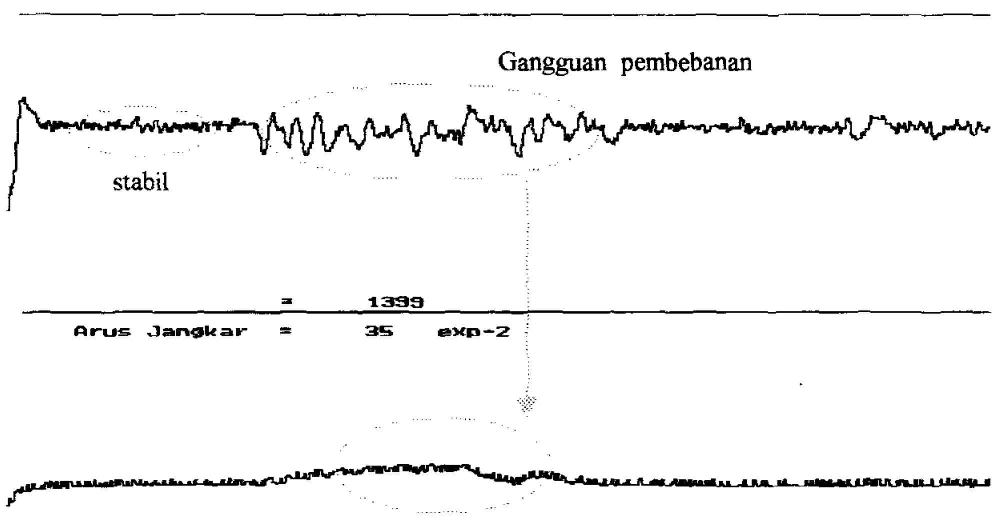
LAMPIRAN

a. Tampilan Respon Pada PC

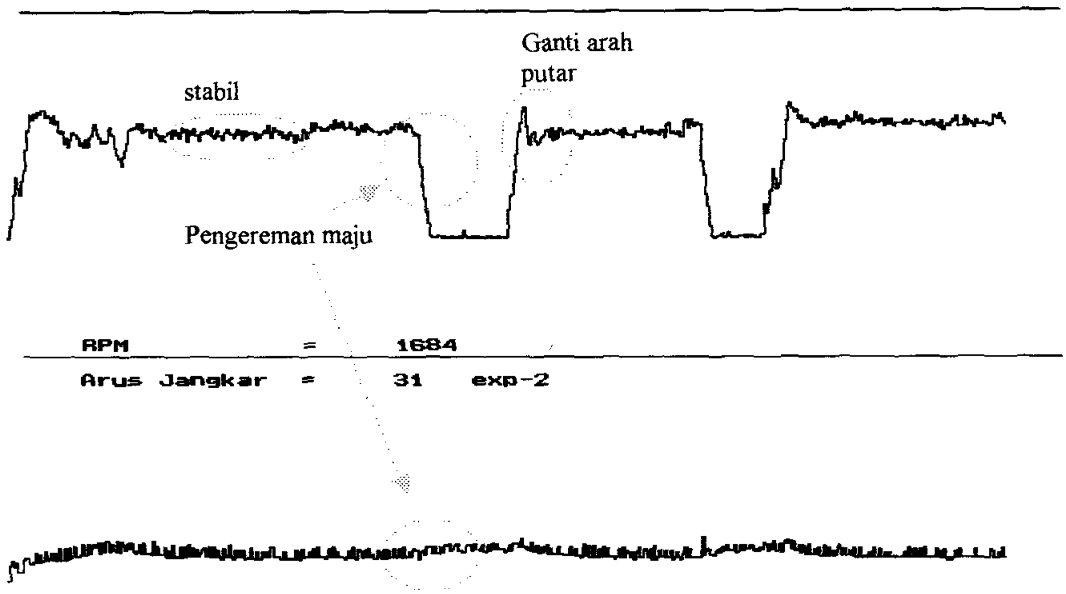
Grafik a.1.Tampilan layar Monitor PC saat motor berputar 950 RPM



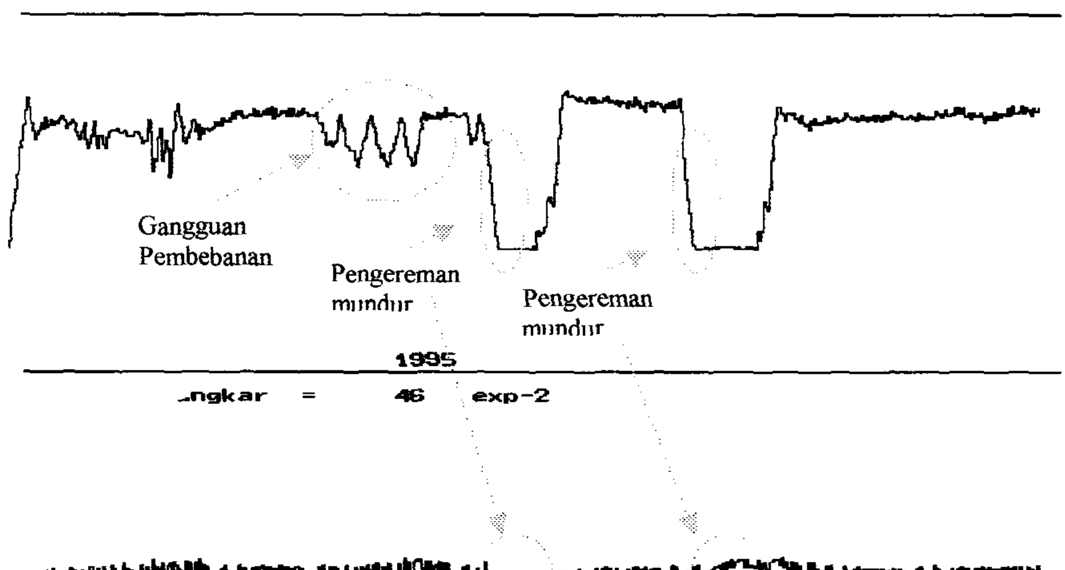
Grafik a.2.Tampilan layar Monitor PC saat motor berputar 1400 RPM



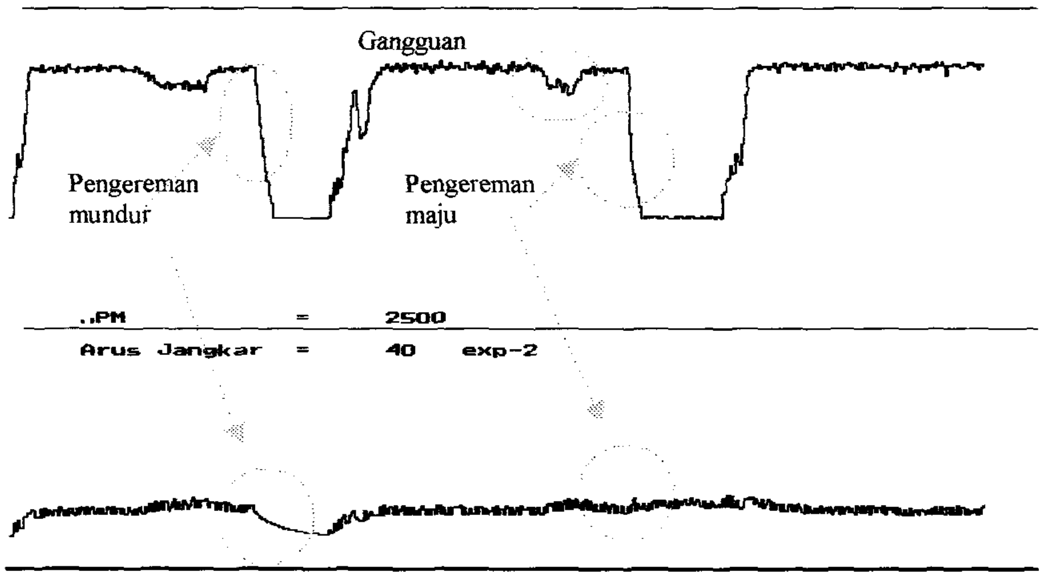
Grafik a.3.Tampilan layar Monitor PC saat motor berputar 1400 RPM



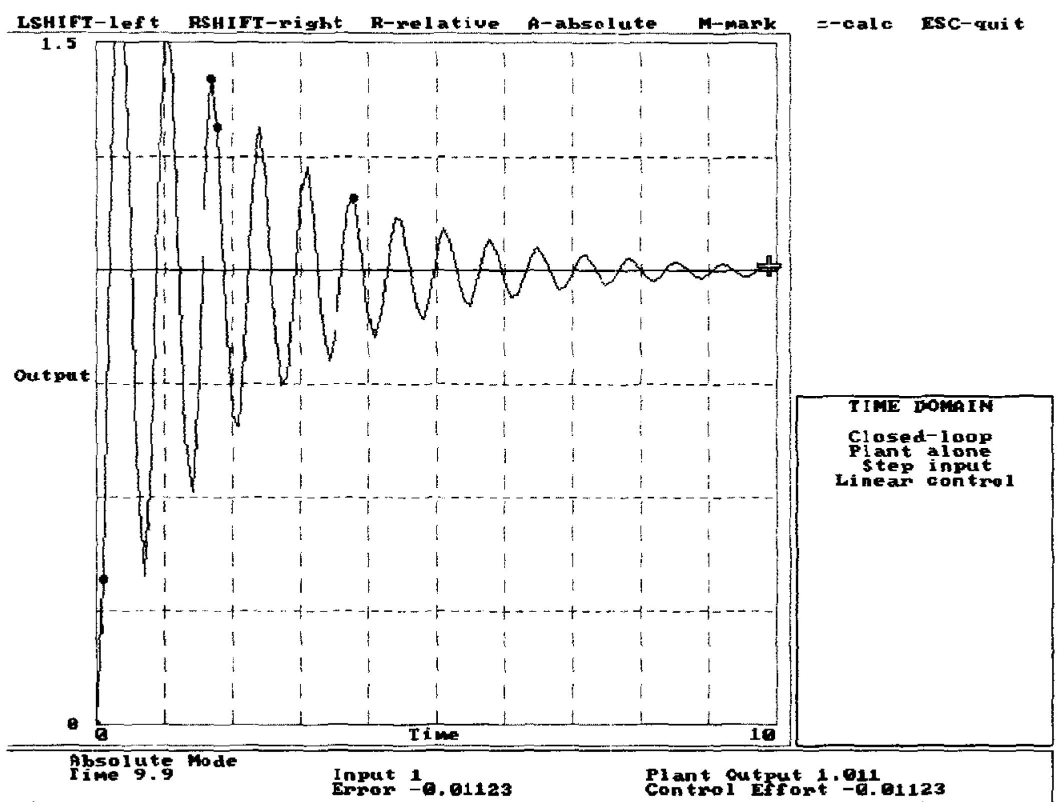
Grafik a.4.Tampilan layar Monitor PC saat motor berputar 2000 RPM



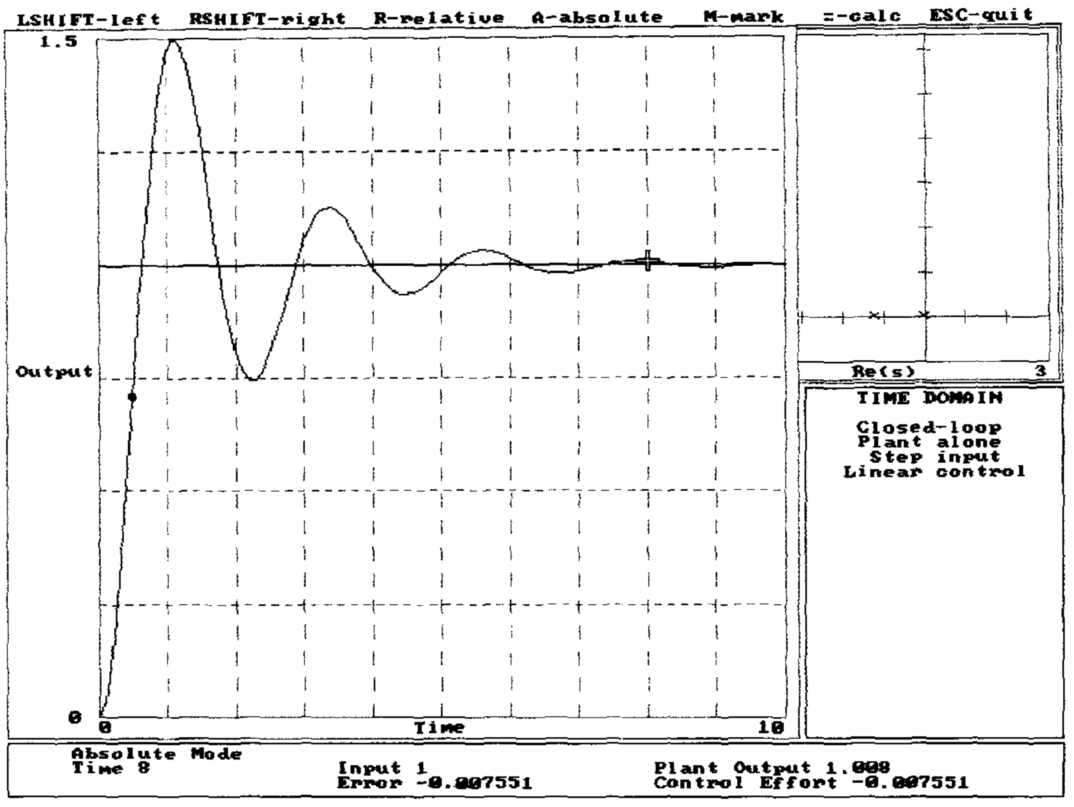
Grafik a.5.Tampilan layar Monitor PC saat motor berputar 2500 RPM



b. Simulasi Codas



Gambar b.1. Respon Transfer Function Motor Servo DC tanpa Sistem Pengendali



Gambar b.2. Respon Transfer Function Motor Servo DC dengan Sistem Pengendali

Tabel Pengukuran Awal Motor Servo Dc

Duty Cycle	Teg. PWM	RPM (1)	RPM (2)	RPM (3)	Arus Ia(1)	Arus Ia (2)	Arus Ia (3)	RPM rata-rata	Arus Ia rata2	w	Kb	PI	J
10%	1.2	182	190	175	0.34	0.33	0.34	182.3333333	0.336666667	19.0842222	0.0381816	0.2453178	0.012854
20%	2.4	487	481	464	0.36	0.36	0.36	477.3333333	0.36	49.9608889	0.0379497	0.68256	0.013662
30%	3.6	794	784	749	0.38	0.37	0.38	775.6666667	0.376666667	81.1884444	0.037847	1.1573711	0.014256
40%	4.8	1038	1068	1031	0.4	0.4	0.39	1045.666667	0.396666667	109.446444	0.038783	1.6837178	0.015384
50%	6	1358	1345	1327	0.42	0.41	0.41	1343.333333	0.413333333	140.602222	0.0385579	2.2408178	0.015937
60%	7.2	1667	1642	1606	0.43	0.43	0.42	1638.333333	0.426666667	171.478889	0.0385043	2.8171378	0.016428
70%	8.4	1931	1953	1925	0.45	0.45	0.44	1936.333333	0.446666667	202.669556	0.0383613	3.4726844	0.017135
80%	9.6	2234	2226	2125	0.45	0.46	0.46	2195	0.456666667	229.743333	0.0390029	4.0920378	0.017811
90%	10.8	2534	2508	2525	0.47	0.47	0.47	2522.333333	0.47	264.004222	0.0384161	4.76674	0.018056
100%	12	2832	2825	2820	0.48	0.48	0.47	2825.666667	0.476666667	295.753111	0.038318	5.4019044	0.018265
	Jumlah Teg.							Jumlah RPM	Jumlah Arus Ia	Jumlah w	Jumlah Kb		Jumlah J
	66							14942	4.16	1563.92933	0.3077906		0.159788
	rata-rata							**rata-rata**	**rata-rata**	**rata-rata**	**rata-rata**		**rata-rata**
	6.6							**1494.2**	**0.416**	**156.392933**	**0.0307791**		**0.015979**

Kb = **0.030779** Vs/rad

Kg = 0.030779 Nm/A

J = 0.0159788 Kg/m2

f = 0.0159788 Nms/rad

Tabel Pengukuran Sistem Pengaturan Motor Servo DC

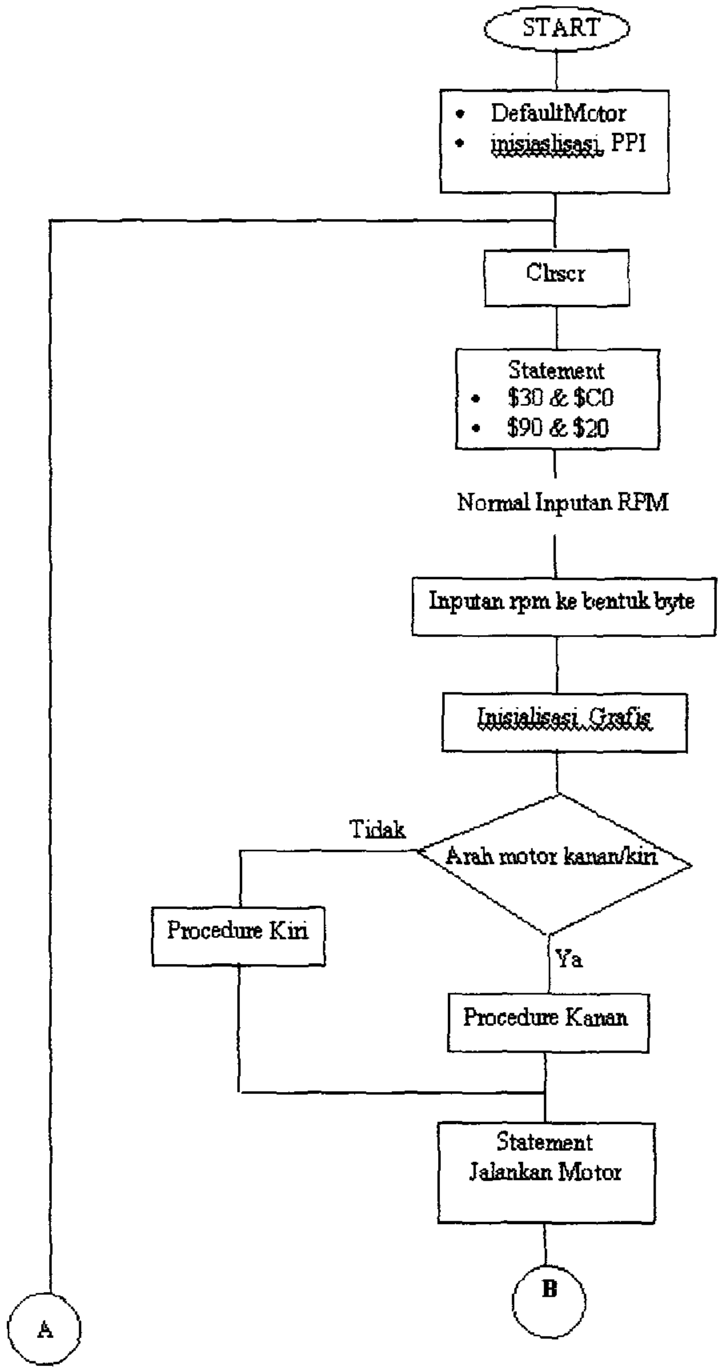
input	rpm 1	rpm2	duty cycle	dutycycle2	Ia1	Ia2	Z (La)	rpm rata2	kec. Radial
900	864	890	26%	27%	0.28	0.28	0.1239201	877	91.79266667
1000	1027	1010	34.00%	33.67%	0.29	0.29	0.1439141	1018.5	106.603
1100	1112	1097	35.00%	34.67%	0.3	0.3	0.1560659	1104.5	115.6043333
1200	1224	1230	36.00%	36.33%	0.31	0.31	0.1733751	1227	128.426
1300	1267	1268	36.70%	36.70%	0.31	0.31	0.1790978	1267.5	132.665
1400	1439	1399	37.30%	37.00%	0.32	0.32	0.2005047	1419	148.522
1500	1512	1502	39.30%	38.67%	0.32	0.32	0.2129391	1507	157.7326667
1600	1608	1638	40.60%	40.33%	0.32	0.32	0.2293299	1623	169.874
1700	1714	1714	42.00%	42.00%	0.33	0.33	0.2421882	1714	179.3986667
1800	1824	1824	42.60%	42.60%	0.34	0.34	0.2577312	1824	190.912
1900	1923	1920	44.00%	44.00%	0.34	0.34	0.271508	1921.5	201.117
2000	2019	2030	46.00%	46.00%	0.34	0.34	0.2860619	2024.5	211.8976667
2100	2144	2128	46.67%	46.67%	0.34	0.34	0.3018168	2136	223.568
2200	2245	2220	47.33%	47.33%	0.34	0.34	0.3154523	2232.5	233.6683333
2300	2310	2327	49.33%	49.33%	0.34	0.34	0.3276041	2318.5	242.6696667
2400	2388	2427	52.00%	52.00%	0.34	0.34	0.3401798	2407.5	251.985
2500	2489	2468	56.00%	56.00%	0.34	0.34	0.3502121	2478.5	259.4163333
2600	2598	2570	59.33%	59.00%	0.34	0.34	0.3651192	2584	270.4586667
2700	0	0	0.00%	0.00%	0	0	#REF!	0	0
2800	0	0	0.00%	0.00%	0	0	#REF!	0	0
					0.32444				

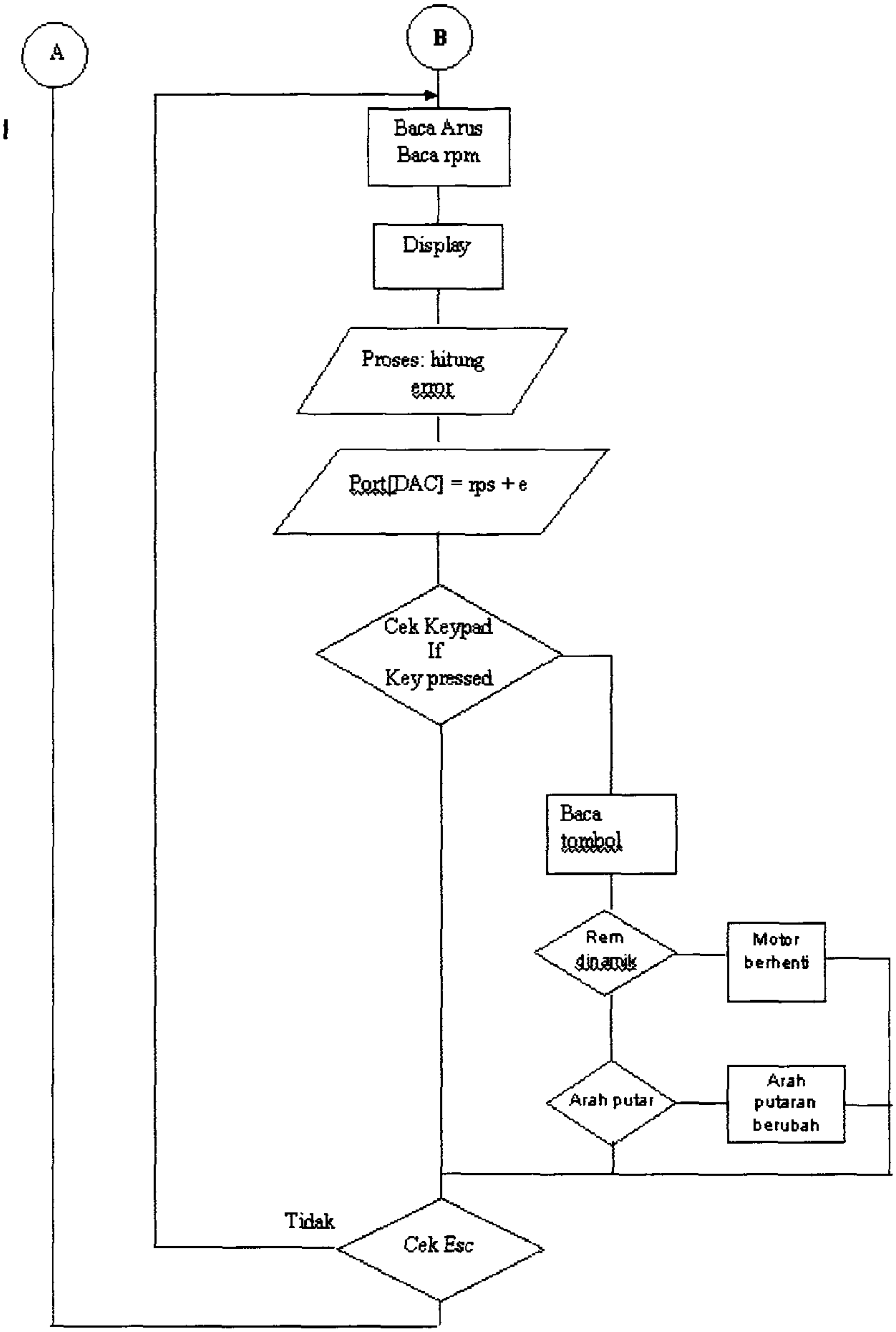
Tabel Pengukuran Sistem Pengaturan Motor Servo DC

Vpwm	Ra*Ia	dc rata2	Vpwm-ra*ia	Kb	Ia2*Ra	Vpwm*Ia	Pi	J	f=J
3.18	0.392	0.265	2.788	0.030372797	0.10976	0.8904	0.78064	0.0085044	0.008504383
4.0602	0.406	0.33835	3.6542	0.034278585	0.11774	1.177458	1.059718	0.0099408	0.00994079
4.1802	0.42	0.34835	3.7602	0.032526462	0.126	1.25406	1.12806	0.0097579	0.009757939
4.3398	0.434	0.36165	3.9058	0.030412845	0.13454	1.345338	1.210798	0.009428	0.009427982
4.404	0.434	0.367	3.97	0.029924999	0.13454	1.36524	1.2307	0.0092767	0.00927675
4.458	0.448	0.3715	4.01	0.026999367	0.14336	1.42656	1.2832	0.0086398	0.008639797
4.6782	0.448	0.38985	4.2302	0.026818795	0.14336	1.497024	1.353664	0.008582	0.008582014
4.8558	0.448	0.40465	4.4078	0.025947467	0.14336	1.553856	1.410496	0.0083032	0.008303189
5.04	0.462	0.42	4.578	0.025518584	0.15246	1.6632	1.51074	0.0084211	0.008421133
5.112	0.476	0.426	4.636	0.024283439	0.16184	1.73808	1.57624	0.0082564	0.008256369
5.28	0.476	0.44	4.804	0.023886593	0.16184	1.7952	1.63336	0.0081214	0.008121442
5.52	0.476	0.46	5.044	0.023803943	0.16184	1.8768	1.71496	0.0080933	0.008093341
5.6004	0.476	0.4667	5.1244	0.02292099	0.16184	1.904136	1.742296	0.0077931	0.007793137
5.6796	0.476	0.4733	5.2036	0.022269171	0.16184	1.931064	1.769224	0.0075715	0.007571518
5.9196	0.476	0.4933	5.4436	0.02243214	0.16184	2.012664	1.850824	0.0076269	0.007626928
6.24	0.476	0.52	5.764	0.022874377	0.16184	2.1216	1.95976	0.0077773	0.007777288
6.72	0.476	0.56	6.244	0.024069417	0.16184	2.2848	2.12296	0.0081836	0.008183602
7.0998	0.476	0.59165	6.6238	0.024490988	0.16184	2.413932	2.252092	0.0083269	0.008326936
V pwm Ttl				Kb Total				J total	f Total
92.368				**0.473830961**				**0.1526045**	**0.152604538**
Vpwm RT2				Kb Total RT2				J Rata2	f rata 2
5.1315				**0.026323942**				**0.008478**	**0.00847803**

Kb = 0.0263 Vs/rad
Kg = 0.0263 Nm/A
J = 0.0085 Kg/m2
f = 0.0085 Nms/rad

LAMPIRAN FLOWCRAT :




A
B
Baca Arus
Baca rpm
Display
Proses: hitung error
Port[DAC] = rps + e
Cek Keypad
If
Key pressed
Baca tombol
Rem dinamik
Motor berhenti
Arah putar
Arah putaran berubah
Tidak
Cek Esc

LAMPIRAN PROGRAM

```
uses crt,graph;
const                           { inisialisasi port PPI }
   adc     = $300;
   dac     = $301;
   port_C  = $302;
   port_CW = $303;
   CW      = $90;               { PPI aktiv pada mode o}
rem_dinamic_1 = $20;            {set rem maju}
rem_dinamic_2 = $90;            {set rem mundur}
putar_kanan   = $30;            {set arah putar motor}
putar_kiri    = $C0;


var  a_jangkar, V_tacho,arus : real;     {pemberian nilai variabel}
   ch,direct                 : char;
   selesai,true,false        : boolean;
   e,status                  : byte;
   data_va,data_ia,putaran   :integer;
   tunda,gd,gm,x,y,x1        :integer;
   rpm2,rpm1                 :byte;
   e1,arus1,rpm,arusl1       :real;
   int ,int2,putaranl1       :integer;

procedure fjdosij;
      begin
      delay(1);
      end;

procedure level_a;                 { prosedure pembagian level RPM masukan}
begin
rpm:=rpm - 110 ;
end;

procedure level_b;
begin
rpm:=rpm - (180 + (0.01*rpm)) ;
end;

procedure level_c;
begin
rpm:=rpm -  (2 + (0.22*rpm));
end;

procedure level_d;
begin
rpm:=rpm -  ( 46 + (0.249*rpm)) ;
end;

procedure level_e;
begin
rpm:=rpm -  (30 + (0.29*rpm)) ;
end;
```

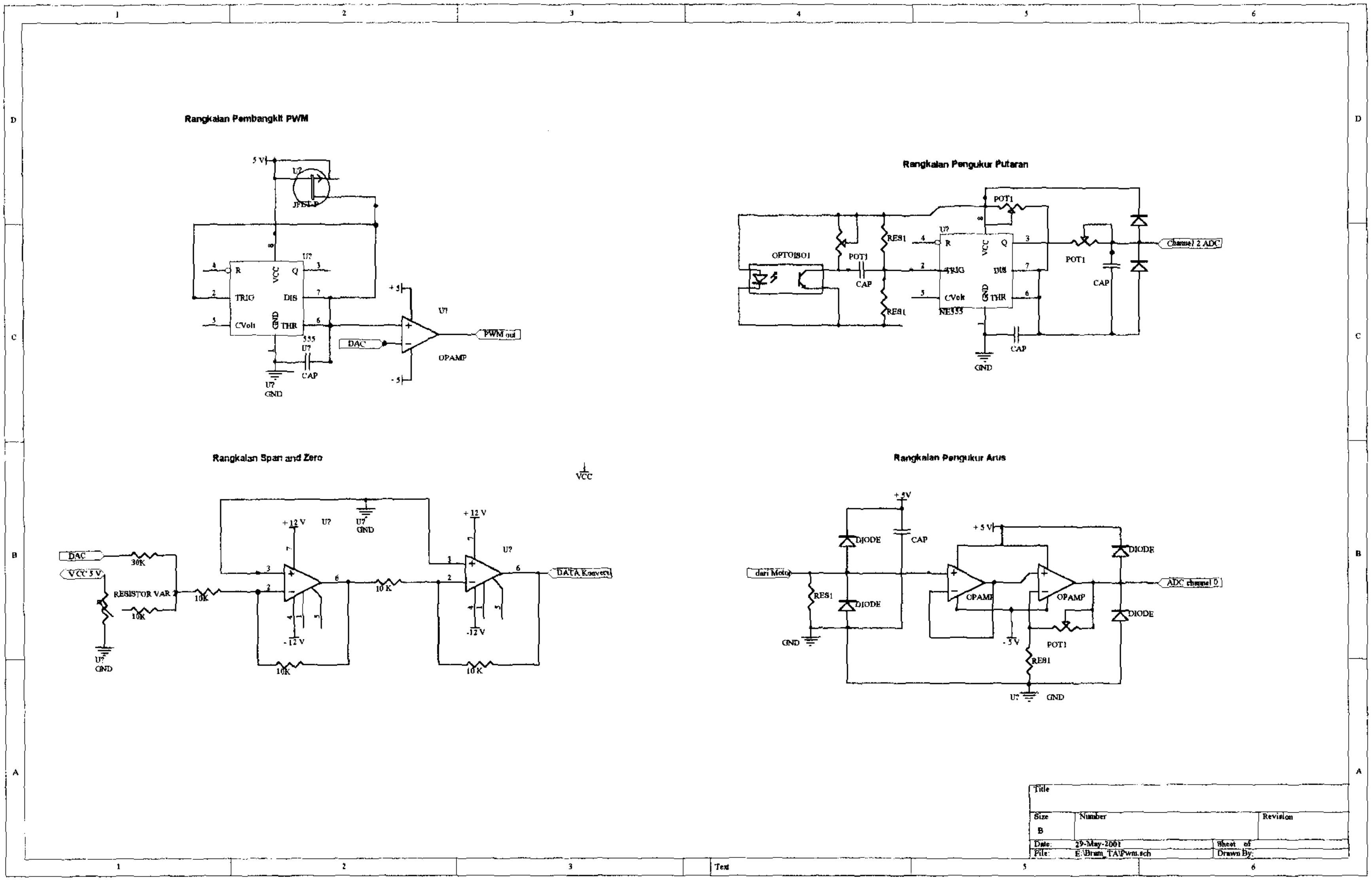
```
procedure level_f;
begin
rpm:=rpm -  (110 + (0.28*rpm))  ;
end;

procedure level_g;
begin
rpm:=rpm -  (144 + (0.299*rpm)) ;
end;

procedure level_h;
begin
rpm:=rpm -  (142 + (0.3*rpm)) ;
end;

procedure level_i;
begin
rpm:=rpm -  (72 + (0.28*rpm)) ;
end;

procedure level_j;
begin
rpm:=rpm -  (20 + (0.26*rpm)) ;
end;


 procedure saluran_0;                    { prosedure untuk pembacaan data oleh
       begin                                    channel ADC0808 (multiplekser )}
        status := port[port_C];
        status := status AND $F8;
        port[port_c]:=status;
        status := status OR $00;
        port[port_C] := status;
        status:= status or $04;
        port[port_C] := status;
        delay(1);
        end;

procedure saluran_1;
        begin
        status := port[port_C];
        status := status AND $F8;
        port[port_c]:=status;
        status := status OR $01;
        port[port_C] := status;
        status:= status or $04;
        port[port_C] := status;
        delay(1);
        end;
```

```
procedure rem1;                                  { prosedure pengaturan motor }
        begin
        status := port[port_C];
        status := $0F AND status;
        status := rem_dinamic_1 OR status;
        port[port_C] := status;
        end;

procedure rem2;
        begin
        status := port[port_C];
        status := $0F AND status;
        status := rem_dinamic_2 OR status;
        port[port_C] := status;
        end;

procedure kanan;
        begin
        status := port[port_C];
        status := $0F AND status;
        status := putar_kanan OR status;
        port[port_C] := status;
        end;

procedure kiri;
        begin
        status := port[port_C];
        status := status and $0f;
        status := putar_kiri OR status;
        port[port_C] :=status;
        end;

procedure initgrafik;                                    {prosedure tampilan grafis}
        begin
        Gd:=Detect;
        InitGraph(Gd, Gm, ' ');
        if GraphResult <> grOk then
        Halt(1);
        end;

function IntToStr(I: Longint): String;
{ Convert any integer type to a string }
var
 S: string[11];
begin
 Str(I, S);
 IntToStr := S;
end;

begin                                                          {main program}
   selesai := false;
   port[port_cw] :=cw;                                    {default stop motor}
   port[dac] := $00;
   port[port_C] := $00;
```

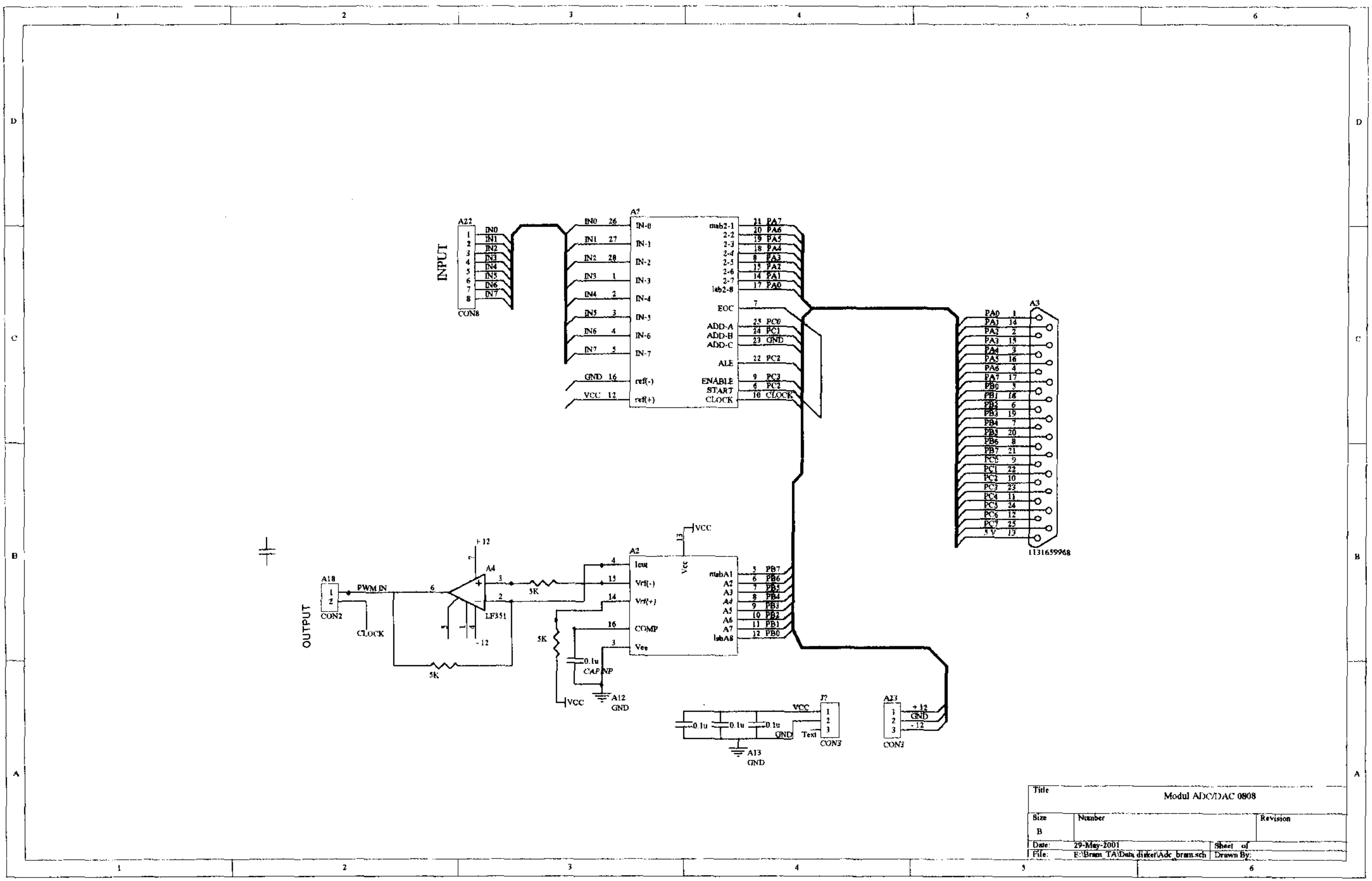
```
repeat  { baca ADC }
   clrscr;
   write(' Arah putaran motor : ');
   readln(direct);
   write(' Berapa RPM - nya   : ');    readln(rpm);

        if(( rpm>800) and ( rpm<= 1050)) then                          {penyesuai nilai input}
           begin
           level_a;
           end
     else
        if(( rpm>1050) and ( rpm<= 1250)) then
           begin
           level_b;
           end
     else
        if(( rpm>1250) and ( rpm<= 1450)) then
           begin
           level_c;
           end
     else
         if(( rpm>1450) and ( rpm<= 1650)) then
           begin
           level_d;
           end
     else
         if(( rpm>1650) and ( rpm<= 1850)) then
           begin
           level_e;
           end
     else
          if(( rpm>1850) and ( rpm<= 2050)) then
           begin
           level_f;
           end
     else
          if(( rpm>2050) and ( rpm<= 2250)) then
           begin
           level_g;
           end

     else
          if(( rpm>2250) and ( rpm<= 2450)) then
           begin
           level_h;
           end

     else
          if(( rpm>2450) and ( rpm<= 2650)) then
           begin
           level_i;
           end

     else
          if(( rpm>2650) and ( rpm<= 2850)) then
```

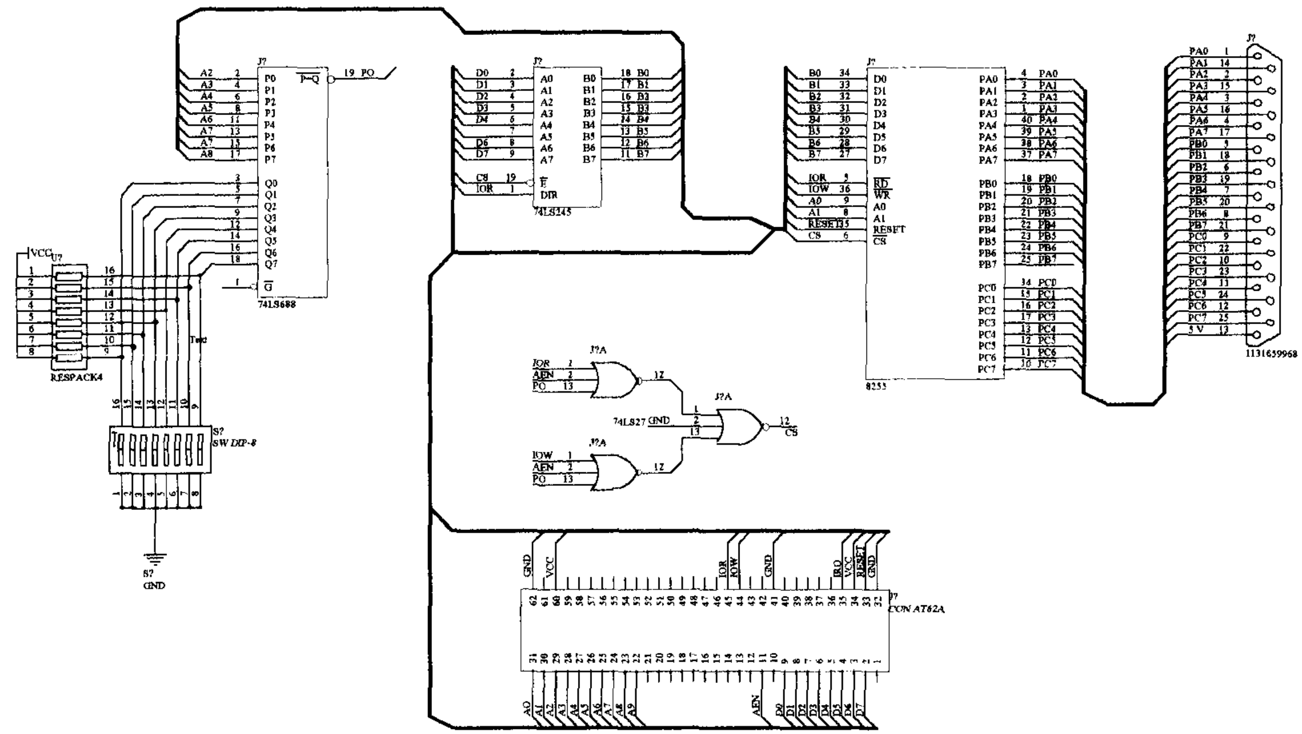
```
          begin
          level_j;
          end


     else
          begin
          port[dac]:=0;
          end;

rpm2:=round(rpm*(255/2850));                    {pengubah nilai desimal rpm ke heksa}
rpm1:=rpm2;
writeln(' ',rpm1);
initgrafik;

if upcase(direct)='R' then kanan                 {inputan pilihan arah putar}
else kiri;
port[dac]:=rpm1;
{delay(500); }
ch:=#0;
x:=1;
x1:=1;
repeat
    line(10,20,600,20);
    saluran_1;
    data_la := port[adc];
    delay(5);
    Arus    := data_la;
    arus1   := arus;
    saluran_2;
    putaran := port[adc];            {rpm}
    e:=round(abs(putaran*(255/220)-rpm2));            {penghitungan nilai error}
    {delay(5); }
    gotoxy(10,10);
    writeln('   ',putaran*(84/110):4:2,'      ',rpm1,'      ');

    if putaran<rpm2 then                        {proses penyesuaian e=0}
      begin
      if (rpm1)>=255 then rpm1:=255
      else
         begin
         rpm1:=rpm1+e;
         port[dac]:=rpm1;
          delay(3);
         end;
     { port[dac]:=$ff;}
      end
    else
       begin
       if rpm1<=rpm2 then rpm1:=rpm2
       else
          begin
          rpm1:=rpm1-e;
          port[dac]:=rpm1;
          delay(3);
```

```
            end;
          end;

        inc(x);
        if x=600 then
          begin
          x:=1;
          cleardevice;
          end;

      setviewport(1,1,600,240,true);                      {tampilan grafis dua layar}
      moveto(x,150-round(putaranl1)div 2);
      lineto(x,150-round(putaran)div 2);
      setviewport(1,200,600,400,true);
      moveto(x,150-round(arusl1));
      lineto(x,150-round(arus1));
      arusl1:=arus1;
      putaranl1:=putaran;
      setcolor(black);

        outtextxy(40,10,'RPM          =');
        outtextxy(40,30,'Arus Jangkar  =');
        outtextxy(200,10,inttostr(int));
        outtextxy(240,30,'exp-3');
        outtextxy(200,30,inttostr(int2));
        int:=round(putaran*(2850/220));                   {tampilan nilai RPM}
        int2:=round(arus*(255/255)*2.2);                  {tampilan nilai arus}
        delay(10);
        setcolor(white);
        outtextxy(40,10,'RPM          =');
        outtextxy(40,30,'Arus Jangkar  =');
        outtextxy(200,10,inttostr(int));
        outtextxy(240,30,'exp-2');
        outtextxy(200,30,inttostr(int2));

        if keypressed then                                {pilihan pengaturan lanjut}
          begin
          ch:=readkey ;
            case ch of
            #80:rem1;
            #72:rem2;
            #75:kanan;
            #77:kiri;
            end;
          end;
    until ch=#27;                                         {kembali ke program utama}
    closegraph;
    port[dac]:=0;
    writeln('Setting');
    ch:=readkey;
    until ch=#27;
    port[dac]:=0;
end.
```



Rangkaian Pembangkit PWM
Rangkaian Pengukur Putaran
Rangkaian Span and Zero
Rangkaian Pengukur Arus
5 V
U2
JFET-P
U?
R
TRIG
CVolt
VCC
GND
Q
DIS
THR
555
CAP
DAC
PWM out
OPAMP
OPTOISO1
POT1
RES1
NE555
Channel 2 ADC
VCC
VCC 5 V
30K
10K
RESISTOR VAR 2
+12 V
-12 V
10 K
DATA Konversi
+5V
DIODE
dari Motor
ADC channel 0
-5V
Title
Size
B
Number
Revision
Date:
29-May-2001
File:
E:\Bram_TA\Pwm.sch
Sheet of
Drawn By:


INPUT
A22
CON8
A?
A3
1131659968
A2
A4
LF351
5K
A18
CON2
PWM IN
CLOCK
OUTPUT
A12
GND
A13
GND
J?
CON3
A23
CON3
VCC
+12
-12
0.1u
CAP NP
Title
Modul ADC/DAC 0808
Size
B
Number
Revision
Date:
29-May-2001
Sheet of
File:
E:\Bram_TA\Data disket\Adc_bram.sch
Drawn By:



Title	PPI CARD 8255	
Size: B	Number	Revision
Date: 29-May-2001		Sheet of
File: E:\Bram_TA\Data disket\Ppi.sch		Drawn By:

19-4325; Rev 2; 10/94

MAXIM

Quad, High-Side MOSFET Drivers

MAX620/MAX621

General Description

The MAX620/MAX621 incorporate four MOSFET drivers and a charge-pump high-side power supply to power high-side switching and control circuits. The charge pump delivers a regulated output voltage 11V greater than V_{CC} to the drivers, which then translate a TTL/CMOS input signal to a noninverted output that swings from ground to the high-side voltage. The outputs drive N-channel FETs in high-side or low-side switching applications, including a wide range of line- and battery-powered applications.

The MAX620/MAX621 are microprocessor compatible and feature undervoltage lockout capability. This lockout feature inhibits the FET driver outputs until the high-side voltage reaches the proper level, as indicated by a Power-Ready output.

The MAX620 requires three inexpensive charge-pump capacitors. The MAX621 has internal capacitors—no external components are needed.

Applications

Portable Computer Battery Load Management

High-Side Power, N-Channel MOSFET Switching

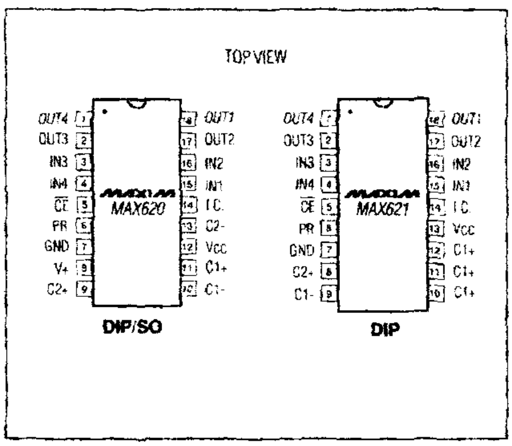
Low-Side Switching from Low Supply Voltages

Quad-Latching Level Translators

H-Bridge Motor Drivers

Stepper Motor Drivers

Pin Configurations



Features

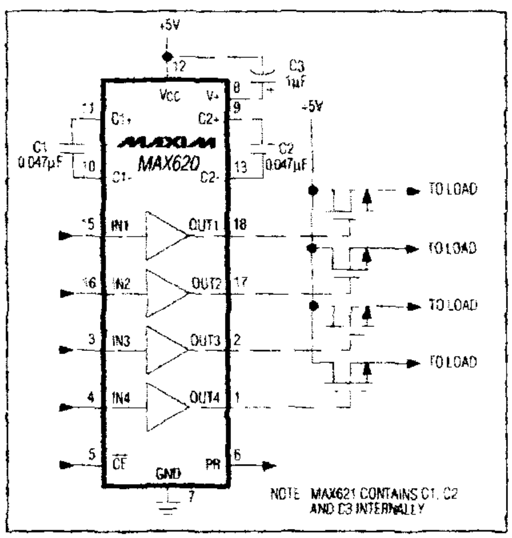
- ♦ Wide Operating Voltage Range
- ♦ Minimum Component Count
- ♦ Output Voltage Regulated to V_{CC} Plus 11V (Typ)
- ♦ Low Quiescent Current – 70µA (Typ)
- ♦ Undervoltage Lockout
- ♦ Power-Ready Output
- ♦ Internal Quad Latch

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX620CPN	0°C to +70°C	18 Plastic DIP
MAX620CWN	0°C to +70°C	18 Wide SO
MAX620C/D	0°C to +70°C	Dice*
MAX620EPN	-40°C to +85°C	18 Plastic DIP
MAX620EWN	-40°C to +85°C	18 Wide SO
MAX621CPN	0°C to +70°C	18 Plastic DIP
MAX621EPN	-40°C to +85°C	18 Plastic DIP

*Contact factory for dice specifications.

Typical Operating Circuit



Quad, High-Side MOSFET Drivers

ABSOLUTE MAXIMUM RATINGS

V_{CC} 17V
V+ to GND 30V
Inputs and Driver Outputs .... (GND-0.3V) to (V+ + 0.3V)
PR Output .... (GND-0.3V) to (V_{CC} + 0.3V)
Continuous Driver Output Current 25mA
V+ Output Current (MAX620 Only) 25mA
Continuous Power Dissipation (T_A = +70°C)
  Plastic DIP (derate 8mW/°C above +70°C) 640mW
  Wide SO (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges:
  MAX62_C_ _ .... 0°C to +70°C
  MAX62_E_ _ .... -40°C to +85°C
Storage Temperature Range .... -65°C to +160°C
Lead Temperature (Soldering, 10 sec) .... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.5		16.5	V
High-Side Voltage (Note 1)	V+	I_{OUT} = 0, V_{CC} = 4.5V, C1 = C2 = 0.047µF, C3 = 1µF	14.5	15.5	17.5	V
		I_{OUT} = 0, V_{CC} = 16.5V, C1 = C2 = 0.01µF, C3 = 1µF (Note 2)	26.5	27.5	29.5	
		I_{OUT} = 250µA, V_{CC} = 5V, C1 = C2 = 0.047µF, C3 = 1µF	15	16	18	
		I_{OUT} = 500µA, V_{CC} = 16.5V, C1 = C2 = 0.01µF, C3 = 1µF (Note 2)	26.5	27.5	29.5	
Power-Ready Threshold	PRT	I_{OUT} = 100µA Sink (Notes 3, 4)	12.0	13.5	14.5	V
Power-Ready Output High	PR_{OH}	I_{SOURCE} = 100µA (Note 4)	3.8	4.7	5.0	V
Power-Ready Output Low	PR_{OL}	I_{SINK} = 1mA (Note 4)		0.1	0.4	V
Switching Frequency	f_O	I_{OUT} = 0, T_A = +25°C		70		kHz
Quiescent Supply Current	I_Q	MAX620: V_{CC} = 5V, C1 = C2 = 0.047µF, C3 = 1µF, T_A = +25°C, I_{OUT} = 0		70	500	µA
		MAX621: V_{CC} = 5V, T_A = +25°C, I_{OUT} = 0				
		MAX620: V_{CC} = 16.5V, C1 = C2 = 0.01µF, C3 = 1µF, T_A = +25°C, I_{OUT} = 0 (Note 5)		50	350	
		MAX621: V_{CC} = 16.5V, T_A = +25°C, I_{OUT} = 0				

ELECTRICAL CHARACTERISTICS (continued)

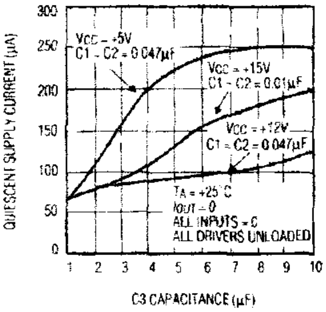
(V_{CC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-SIDE DRIVERS						
Input Threshold Low	V_{TL}				0.8	V
Input Threshold High	V_{TH}		2.4			V
Input Bias Current	I_B	0V < V_{IN} < 5V	-100		100	nA
Chip Enable Threshold Low	CE_{LO}				0.8	V
Chip Enable Threshold High	CE_{HI}		2.4			V
Minimum $\overline{CE}$ Pulse Duration	T_{CE}		100	50		ns
Pull-Down Current	I_{CE}			10		µA
Data-Hold Time	T_{DH}			-10	10	ns
Data Set-Up Time	T_{SU}			50	100	ns
Data-Delay Time	T_{OD}	V_{CE} = 0V, C_L = 12pF		150		ns
Driver Output Rise Time	T_R	C_L = 1000pF		1.7		µs
Driver Output Fall Time	T_F	C_L = 1000pF		2.5		µs

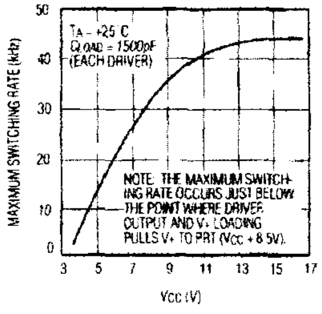
Note 1: High-Side Voltage (V+) is available only on the MAX620 and is measured with respect to GND. V+ on the MAX621 is measured at an unloaded output. Capacitor values listed in the test conditions apply to the MAX620 only.
Note 2: *For V_{CC} > +13V, on the MAX620 only, use C1 = C2 = 0.01µF, C3 = 1µF.*
Note 3: Power-Ready Threshold is the voltage with respect to GND at V+ when PR switches high (PR_{OH} = V_{CC}).
Note 4: For the MAX621, the Power-Ready levels are tested at wafer sort only.
Note 5: The MAX620 is tested for quiescent current at +16.5V using C1 = C2 = 0.047µF to minimize test time. In normal operation above +13V, C1 and C2 must not exceed 0.01µF.

Typical Operating Characteristics

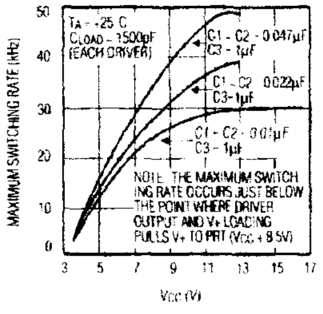
MAX620 QUIESCENT SUPPLY CURRENT vs. C3 CAPACITANCE



MAX621 MAXIMUM SWITCHING RATE vs. V_{CC} SYNCHRONOUSLY DRIVING ALL FOUR INPUTS



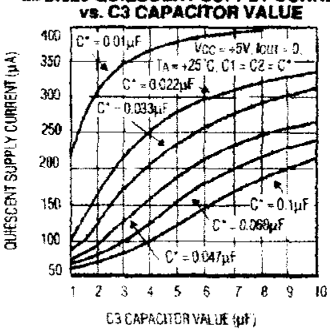
MAX620 MAXIMUM SWITCHING RATE vs. V_{CC} SYNCHRONOUSLY DRIVING ALL FOUR INPUTS



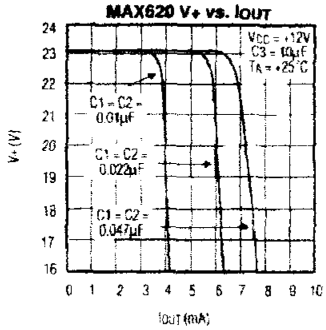
Quad, High-Side MOSFET Drivers

Typical Operating Characteristics (continued)

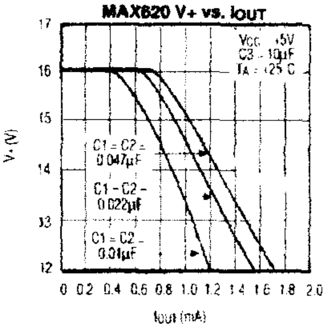
MAX620 QUIESCENT SUPPLY CURRENT vs. C3 CAPACITOR VALUE



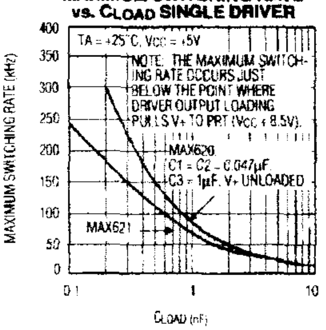
MAX620 V+ vs. IOUT



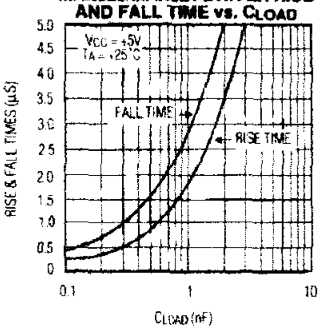
MAX620 V+ vs. IOUT



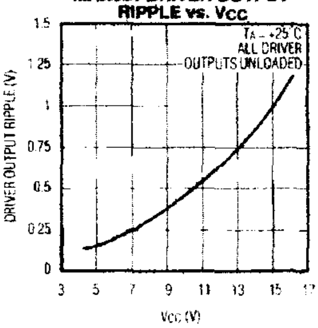
MAXIMUM SWITCHING RATE vs. CLOAD SINGLE DRIVER



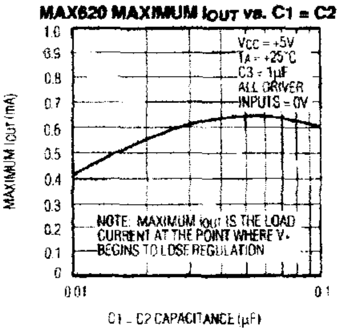
MAX620/MAX621 DRIVER RISE AND FALL TIME vs. CLOAD



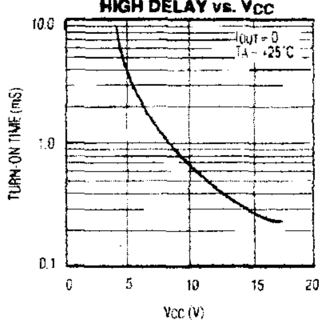
MAX621 DRIVER OUTPUT RIPPLE vs. VCC



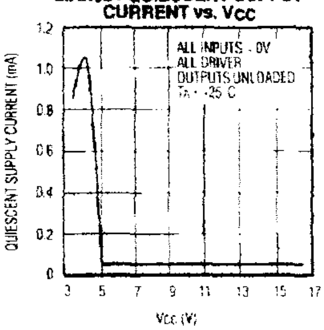
MAX620 MAXIMUM IOUT vs. C1 = C2



VCC TO POWER-READY HIGH DELAY vs. VCC



MAX621 QUIESCENT SUPPLY CURRENT vs. VCC



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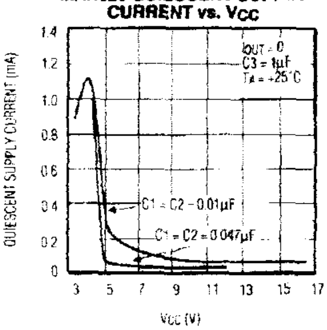
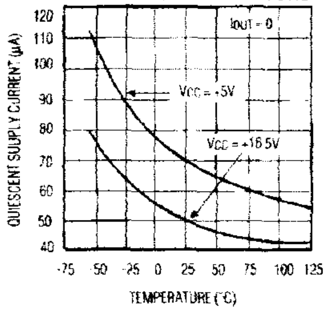
Typical Operating Characteristics (continued)

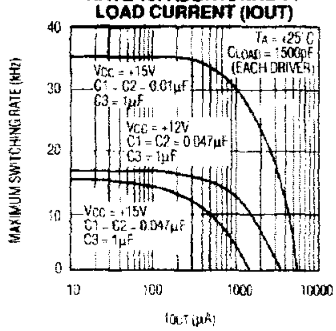
MAX620 QUIESCENT SUPPLY CURRENT vs. V_{CC}



MAX620/621 QUIESCENT SUPPLY CURRENT vs. TEMPERATURE

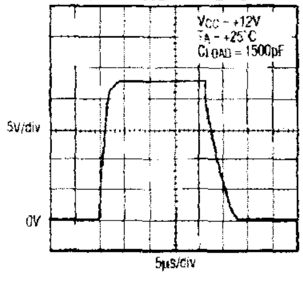


MAX620 MAXIMUM SWITCHING RATE vs. ADDITIONAL V+ LOAD CURRENT (IOUT)

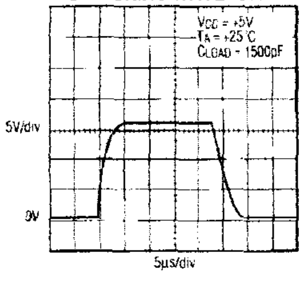


NOTE: THE MAXIMUM SWITCHING RATE OCCURS JUST BELOW THE POINT WHERE DRIVER OUTPUT AND V+ LOADING PULLS V+ TO PRT (VCC + 8.5V).

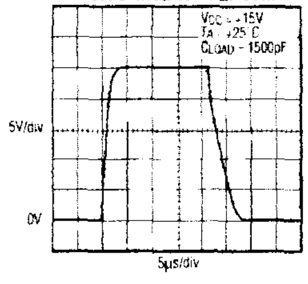
DRIVER OUTPUT SWITCHING WAVEFORM



DRIVER OUTPUT SWITCHING WAVEFORM



DRIVER OUTPUT SWITCHING WAVEFORM



Quad, High-Side MOSFET Drivers

Pin Description

PIN		NAME	FUNCTION
MAX620	MAX621		
1	1	OUT4	Driver Output 4
2	2	OUT3	Driver Output 3
3	3	IN3	TTL/CMOS Compatible Input to Driver 3. Connect to GND if unused.
4	4	IN4	TTL/CMOS Compatible Input to Driver 4. Connect to GND if unused.
5	5	CE	Chip Enable. Logic high inhibits input data. Logic low transfers input data to the quad latch and driver outputs. $\overline{CE}$ pulse must be at least 100ns. Connect to GND for direct data transfer to driver outputs.
6	6	PR	Power-Ready Output is a logic high equal to V_{CC} when V+ ≥ (V_{CC} plus 8.5V)
7	7	GND	Ground
8		V+	High-side voltage out. Equal to approximately V_{CC} plus 11V.
	8	C2+	Internally connected to secondary charge-pump capacitor. Make no connection to this pin.
9		C2+	Positive terminal to secondary charge-pump capacitor. Connect to 0.047µF capacitor. For V_{CC} > 13V, connect to 0.01µF.
	9	C1-	Internallly connected to primary charge-pump capacitor. Make no connection to this pin.
10		C1-	Negative terminal to primary charge-pump capacitor. Connect to 0.047µF capacitor. For V_{CC} > 13V, connect to 0.01µF.
	10-12	C1+	Internally connected to primary charge-pump capacitor. Make no connection to these pins.
11		C1+	Positive terminal to primary charge-pump capacitor. Connect to 0.047µF capacitor. For V_{CC} > 13V, connect to 0.01µF.
12	13	V_{CC}	Supply Voltage. Connect to positive supply.
13		C2-	Negative terminal to secondary charge-pump capacitor. Connect to 0.047µF capacitor. For V_{CC} > 13V, connect to 0.01µF.
14	14	I.C.	Internal Connection. Make no connection to this pin.
15	15	IN1	TTL/CMOS Compatible Input to Driver 1. Connect to GND if unused.
16	16	IN2	TTL/CMOS Compatible Input to Driver 2. Connect to GND if unused.
17	17	OUT2	Driver Output 2
18	18	OUT1	Driver Output 1

National Semiconductor

May 1999

DAC0808
8-Bit D/A Converter

General Description

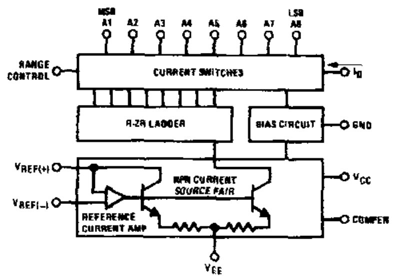
The DAC0808 is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 I_{REF}/256. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 µA provides 8-bit zero accuracy for I_{REF}≥2 mA. The power supply currents of the DAC0808 is independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

Features

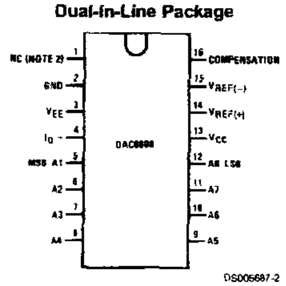
- Relative accuracy: ±0.19% error maximum
- Full scale current match: ±1 LSB typ
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/µs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

Block and Connection Diagrams



DS005687-1

Dual-In-Line Package



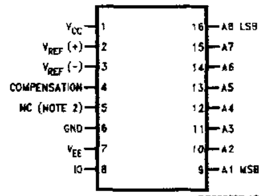
DS005687-2

Top View
Order Number DAC0808
See NS Package M16A or N16A

 DS005687

Block and Connection Diagrams (Continued)

Small-Outline Package



DS005687-13

Ordering Information

ACCURACY	OPERATING TEMPERATURE RANGE	N PACKAGE (N16A) (Note 1)		SO PACKAGE (M16A)
8-bit	$0^{\circ}C \leq T_A \leq +75^{\circ}C$	DAC0808LCN	MC1408P8	DAC0808LCM

Note 1: Devices may be ordered by using either order number.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage	
V_{CC}	+18 V_{DC}
V_{EE}	−18 V_{DC}
Digital Input Voltage, V5–V12	−10 V_{DC} to +18 V_{DC}
Applied Output Voltage, V_O	−11 V_{DC} to +18 V_{DC}
Reference Current, I_{14}	5 mA
Reference Amplifier Inputs, V14, V15	V_{CC}, V_{EE}
Power Dissipation (Note 4)	1000 mW
ESD Susceptibility (Note 5)	TBD
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
DAC0808	$0 \le T_A \le +75°C$

Electrical Characteristics

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, V_{REF}/R14 = 2 mA, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
E_r	Relative Accuracy (Error Relative to Full Scale I_O)	(*Figure 4*)				%
	DAC0808LC (LM1408-8)				±0.19	%
	Settling Time to Within ½ LSB (Includes t_{PLH})	T_A=25°C (Note 7), (*Figure 5*)		150		ns
t_{PLH}, t_{PHL}	Propagation Delay Time	T_A = 25°C, (*Figure 5*)		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		ppm/°C
MSB	Digital Input Logic Levels	(*Figure 3*)				
V_{IH}	High Level, Logic "1"		2			V_{DC}
V_{IL}	Low Level, Logic "0"				0.8	V_{DC}
MSB	Digital Input Current	(*Figure 3*)				
	High Level	V_{IH} = 5V		0	0.040	mA
	Low Level	V_{IL} = 0.8V		−0.003	−0.8	mA
I_{15}	Reference Input Bias Current	(*Figure 3*)		−1	−3	µA
	Output Current Range	(*Figure 3*)				
		V_{EE} = −5V	0	2.0	2.1	mA
		V_{EE} = −15V, T_A = 25°C	0	2.0	4.2	mA
I_O	Output Current	V_{REF} = 2.000V, R14 = 1000Ω, (*Figure 3*)	1.9	1.99	2.1	mA
	Output Current, All Bits Low	(*Figure 3*)		0	4	µA
	Output Voltage Compliance (Note 3)	$E_r \le 0.19\%$, T_A = 25°C				
	V_{EE}=−5V, I_{REF}=1 mA				−0.55, +0.4	V_{DC}
	V_{EE} Below −10V				−5.0, +0.4	V_{DC}
SRI_{REF}	Reference Current Slew Rate	(*Figure 6*)	4	8		mA/µs
	Output Current Power Supply Sensitivity	$-5V \le V_{EE} \le -16.5V$		0.05	2.7	µA/V
	Power Supply Current (All Bits Low)	(*Figure 3*)				
I_{CC}				2.3	22	mA
I_{EE}				−4.3	−13	mA
	Power Supply Voltage Range	T_A = 25°C, (*Figure 3*)				
V_{CC}			4.5	5.0	5.5	V_{DC}
V_{EE}			−4.5	−15	−16.5	V_{DC}
	Power Dissipation					

Electrical Characteristics (Continued)

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, V_{REF}/R14 = 2 mA, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	All Bits Low	V_{CC} = 5V, V_{EE} = −5V		33	170	mW
		V_{CC} = 5V, V_{EE} = −15V		106	305	mW
	All Bits High	V_{CC} = 15V, V_{EE} = −5V		90		mW
		V_{CC} = 15V, V_{EE} = −15V		160		mW

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 3: Range control is not required.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maixmum Ratings, whichever is lower. For this device, T_{JMAX} = 125°C, and the typical junction-to-ambient thermal resistance of the dual-in-line J package when the board mounted is 100°C/W. For the dual-in-line N package, this number increases to 175°C/W and for the small outline M package this number is 100°C/W.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: All current switches are tested to guarantee at least 50% of rated current.

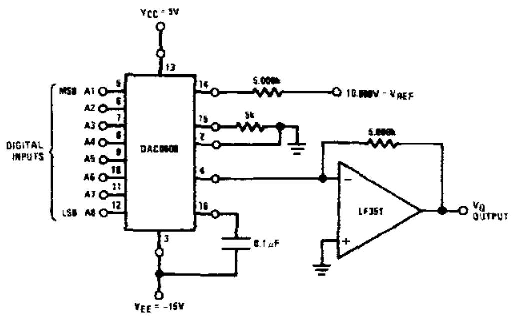
Note 7: All bits switched.

Note 8: *Pin-out numbers for the DAL080X represent the dual-in-line package. The small outline package pinout differs from the dual-in-line package.*

Typical Application

$$V_O = 10V\left(\frac{A1}{2} + \frac{A2}{4} + \cdots \frac{A8}{256}\right)$$

DS006687-23

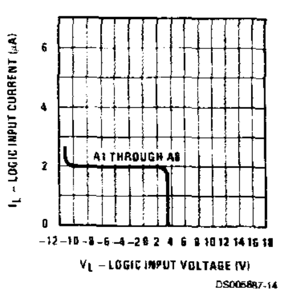


DS006687-3

FIGURE 1. +10V Output Digital to Analog Converter (Note 8)

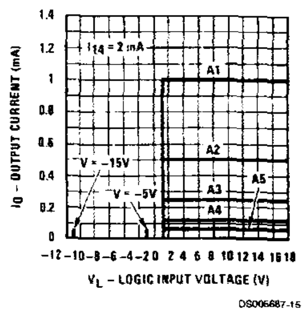
Typical Performance Characteristics V_{CC} = 5V, V_{EE} = −15V, T_A = 25°C, *unless otherwise noted*

Logic Input Current vs Input Voltage



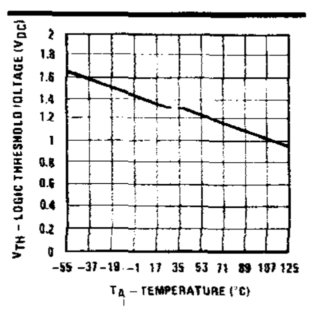
DS006687-14

Bit Transfer Characteristics



DS006687-15

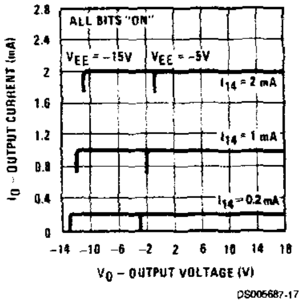
Logic Threshold Voltage vs Temperature



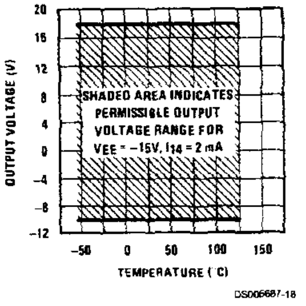
DS006687-16

Typical Performance Characteristics V_{CC} = 5V, V_{EE} = −15V, T_A = 25˚C, unless otherwise noted (Continued)

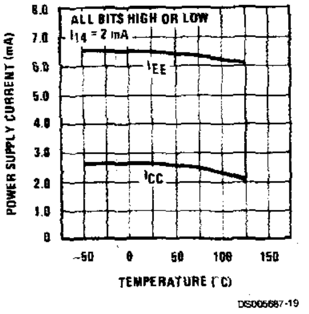
Output Current vs Output Voltage (Output Voltage Compliance)



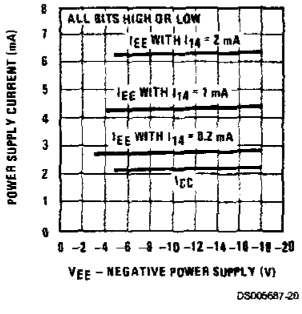
Output Voltage Compliance vs Temperature



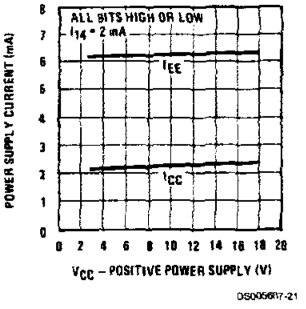
Typical Power Supply Current vs Temperature



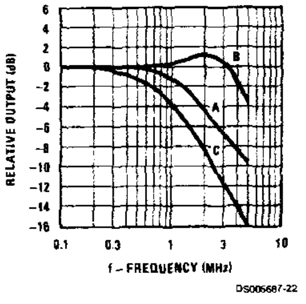
Typical Power Supply Current vs V_{EE}



Typical Power Supply Current vs V_{CC}



Reference Input Frequency Response



Unless otherwise specified: R14 = R15 = 1 kΩ, C = 15 pF, pin 16 to V_{EE}; R_L = 50Ω, pin 4 to ground.

Curve A: Large Signal Bandwidth Method of *Figure 7*, V_{REF} = 2 Vp-p offset 1V above ground.

Curve B: Small Signal Bandwidth Method of *Figure 7*, R_L = 250Ω, V_{REF} = 50 mVp-p offset 200 mV above ground.

Curve C: Large and Small Signal Bandwidth Method of *Figure 9* (no op amp, R_L = 50Ω), R_S = 50Ω, V_{REF} = 2V, V_S = 100 mVp-p centered at 0V.

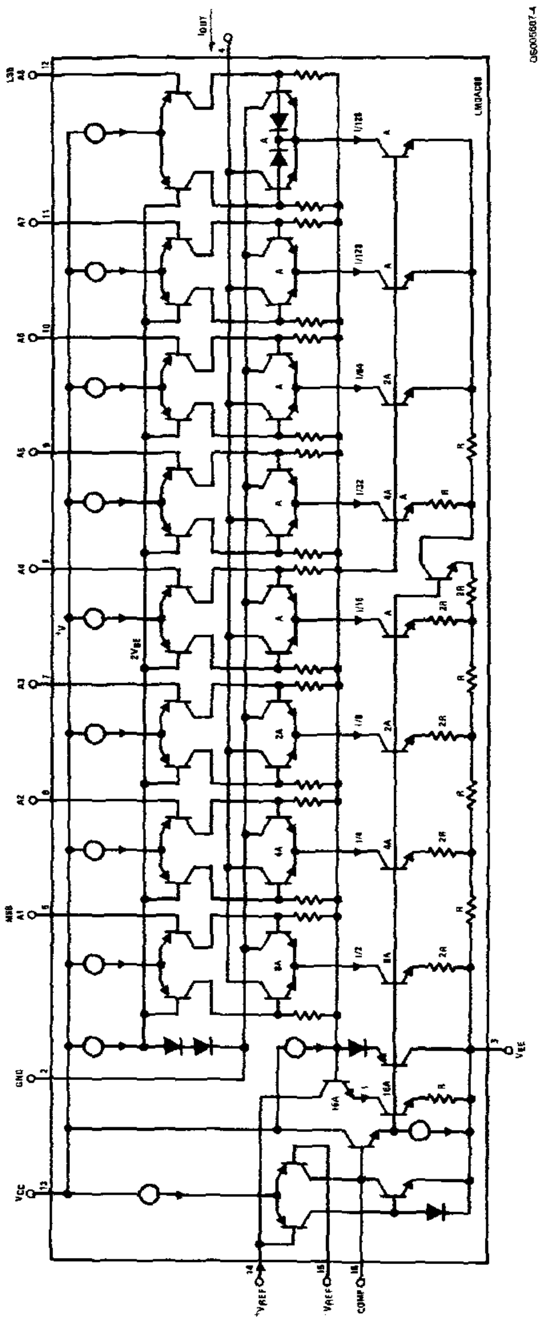


FIGURE 2. Equivalent Circuit of the DAC0808 Series (Note 8)

National Semiconductor

ADC0808/ADC0809 8-Bit μP Compatible A/D Converters with 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.)

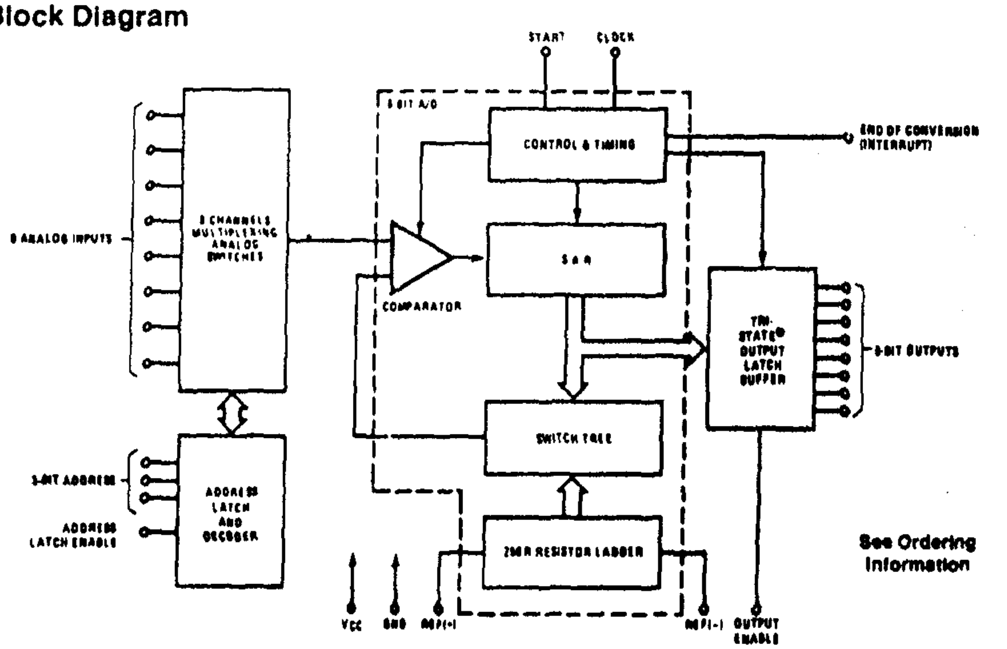
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- No zero or full-scale adjust required
- 8-channel multiplexer with address logic
- 0V to 5V input range with single 5V power supply
- Outputs meet TTL voltage level specifications
- Standard hermetic or molded 28-pin DIP package
- 28-pin molded chip carrier package
- ADC0808 equivalent to MM74C949
- ADC0809 equivalent to MM74C949-1

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	100 μs

Block Diagram



See Ordering Information

TL/H/5672-1

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin	−0.3V to (V_{CC} + 0.3V)
Except Control Inputs	
Voltage at Control Inputs	−0.3V to +15V
(START, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Molded Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 11)	400V

Operating Conditions (Notes 1 & 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0808CJ	−55°C ≤ T_A ≤ +125°C
ADC0808CCJ, ADC0808CCN, ADC0809CCN	−40°C ≤ T_A ≤ +85°C
ADC0808CCV, ADC0809CCV	−40°C ≤ T_A ≤ +85°C
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}

Electrical Characteristics

Converter Specifications: V_{CC} = 5 V_{DC} = V_{REF+}, $V_{REF(-)}$ = GND, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808 Total Unadjusted Error (Note 5)	25°C T_{MIN} to T_{MAX}			±½ ±¾	LSB LSB
	ADC0809 Total Unadjusted Error (Note 5)	0°C to 70°C T_{MIN} to T_{MAX}			±1 ±1¼	LSB LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	2.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		V_{CC}/2−0.1	V_{CC}/2	V_{CC}/2+0.1	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
I_{IN}	Comparator Input Current	f_c = 640 kHz, (Note 6)	−2	±0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0808CJ 4.5V ≤ V_{CC} ≤ 5.5V, −55°C ≤ T_A ≤ +125°C unless otherwise noted ADC0808CCJ, ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, 4.75 ≤ V_{CC} ≤ 5.25V, −40°C ≤ T_A ≤ +85°C unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
$I_{OFF(+)}$	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 5V, T_A = 25°C T_{MIN} to T_{MAX}		10	200 1.0	nA μA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 0, T_A = 25°C T_{MIN} to T_{MAX}	−200 −1.0	−10		nA μA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0808CJ $4.5V \le V_{CC} \le 5.5V$, $-55°C \le T_A \le +125°C$ unless otherwise noted ADC0808CCJ, ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, $4.75 \le V_{CC} \le 5.25V$, $-40°C \le T_A \le +85°C$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	$V_{IN}=15V$			1.0	µA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	$V_{IN}=0$	−1.0			µA
I_{CC}	Supply Current	$f_{CLK}=640$ kHz		0.3	3.0	mA
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O=-360$ µA	$V_{CC}-0.4$			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O=1.6$ mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	$I_O=1.2$ mA			0.45	V
I_{OUT}	TRI-STATE Output Current	$V_O=5V$			3	µA
		$V_O=0$	3			µA

Electrical Characteristics

Timing Specifications $V_{CC}=V_{REF(+)}=5V$, $V_{REF(-)}=GND$, $t_r=t_f=20$ ns and $T_A=25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	*(Figure 5)*		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*		100	200	ns
t_s	Minimum Address Set-Up Time	*(Figure 5)*		25	50	ns
t_H	Minimum Address Hold Time	*(Figure 5)*		25	50	ns
t_D	Analog MUX Delay Time From ALE	$R_S=0\Omega$ *(Figure 5)*		1	2.5	µS
t_{H1}, t_{H0}	OE Control to Q Logic State	$C_L=50$ pF, $R_L=10k$ *(Figure 8)*		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	$C_L=10$ pF, $R_L=10k$ *(Figure 8)*		125	250	ns
t_c	Conversion Time	$f_c=640$ kHz, *(Figure 5)* (Note 7)	90	100	116	µS
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	0		8+2 µS	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs, (Note 12)		10	15	pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions

Note 2: All voltages are measured with respect to GND, unless othewise specified

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC}n supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence *(Figure 6)*. See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Note 8: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Functional Description

Multiplexer. The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table I shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit *analog-to-digital converter*. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached + ½ LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

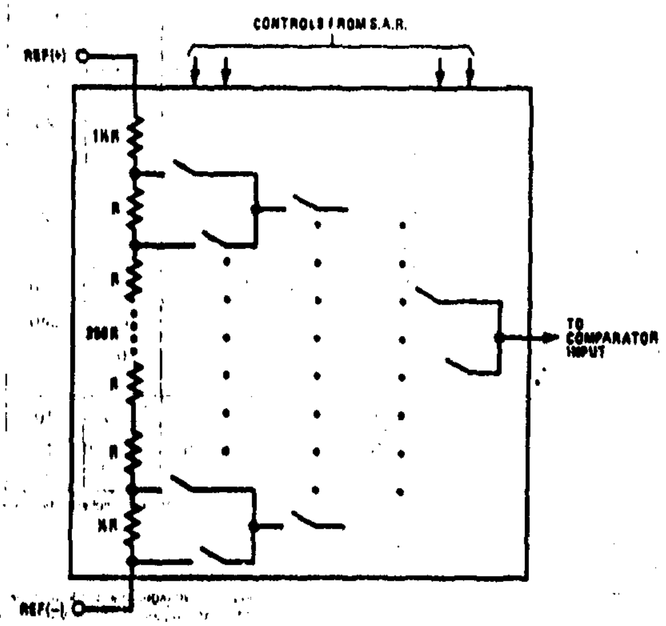


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FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed throught a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

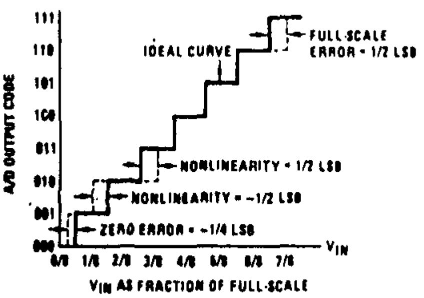

FIGURE 2. 3-Bit A/D Transfer Curve

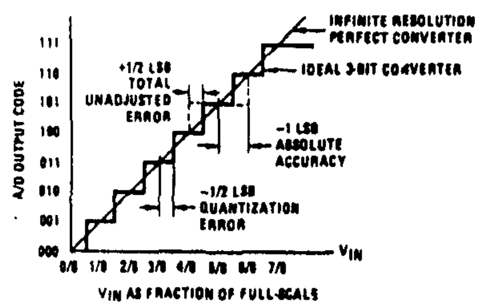

FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

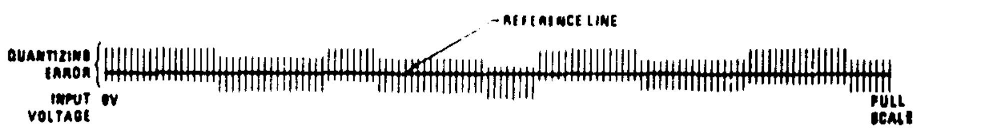

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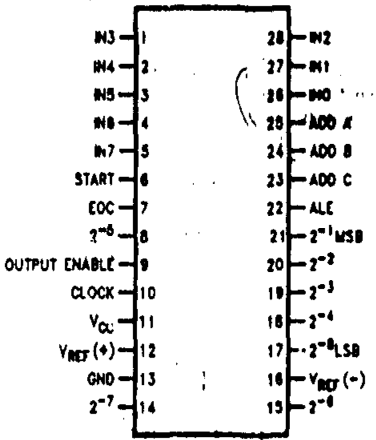
FIGURE 4. Typical Error Curve

Connection Diagrams

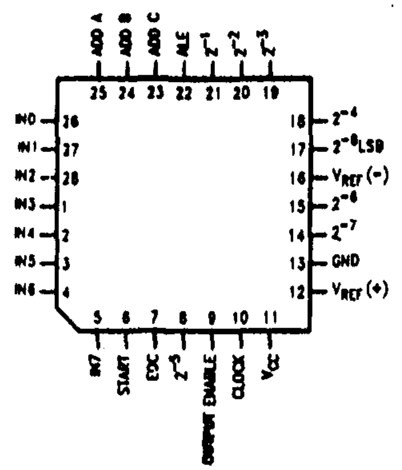
Dual-In-Line Package



TL/H/5672-11

Order Number ADC0808CCN, ADC0809CCN, ADC0808CCJ or ADC0809CCJ See NS Package J28A or N28A

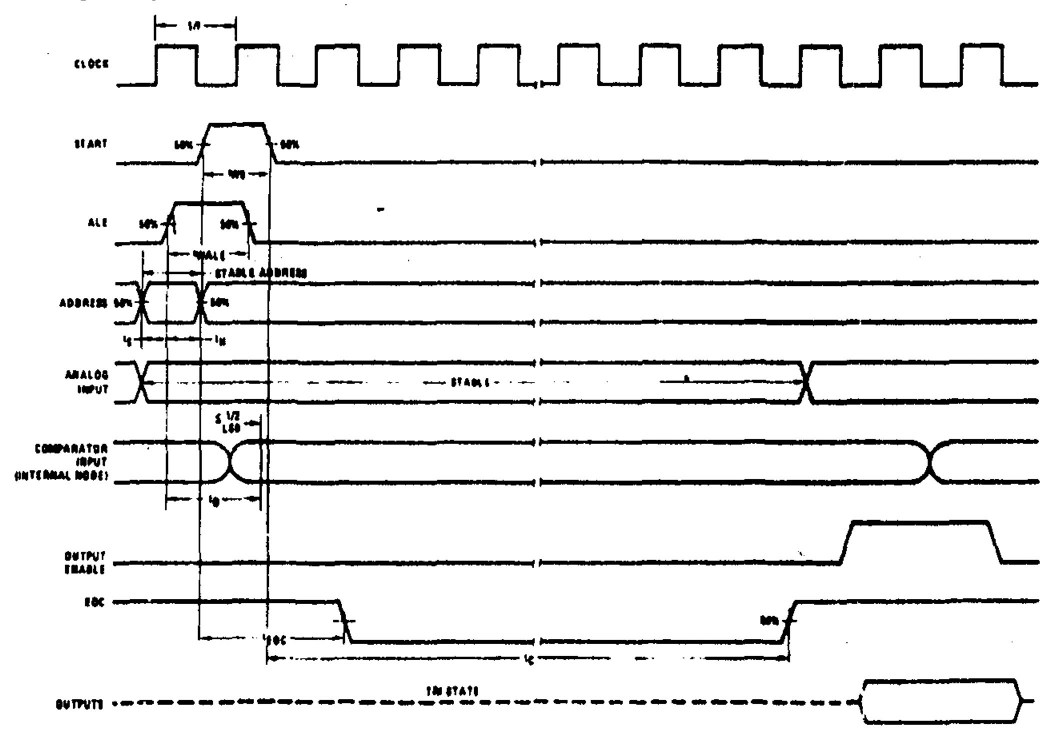
Molded Chip Carrier Package



TL/H/5672-12

Order Number ADC0808CCV or ADC0809CCV See NS Package V28A

Timing Diagram



TL/H/5672-4

FIGURE 5

BIODATA

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