LAMPIRAN
Foto Alat Keseluruhan

Ket: Frekuensi Input 1 KHz
Tampilan Oscilloscope Input dari Audio Generator (Chanel 1) dan Output alat (Chanel 2)
START

INISIALISASI STACK POINTER, LCD

BACA DATA EQUALISER

KIRIM DATA EQUALISER KE ANALOG SWITCH

TIDAK

APA TOMBOL KANAN DITEKAN

APA TOMBOL KIRI DITEKAN

TAMBAHKAN BAND DAN TAMPILKAN KE LCD

BACA PROSEDUR SESUAI DENGAN KANAL

TAMBAHKAN SETINGAN DENGAN DENGAN 1

SIMPAN SETINGAN KE SERIAL MEMORY

TAMPILKAN KE LCD
PROGRAM MICROCONTROLLER AT89C51

\( \text{p1.0} = \text{sclck} \)
\( \text{p1.1} = \text{rclik} \)
\( \text{p1.2} = \text{serch12} \)
\( \text{p1.3} = \text{serch34} \)
\( \text{p1.4} = \text{serch56} \)
\( \text{p1.5} = \text{serch78} \)
\( \text{p1.6} = \text{clk I2C} \)
\( \text{p1.7} = \text{sda I2C} \)

\( \text{pa} = \text{simulasi lcd} = \text{p2} \)
\( \text{pb} = \text{simulasi tombol} = \text{p3.3 & p3.4} \)

\[ \begin{align*}
\text{pa} & \text{ equ } 4000h \\
\text{pb} & \text{ equ } 4001h \\
\text{pc} & \text{ equ } 4002h \\
\text{pcw} & \text{ equ } 4003h \\
\text{cw} & \text{ equ } 82h \\
\text{ch12} & \text{ equ } 08h \\
\text{ch34} & \text{ equ } 09h \\
\text{ch56} & \text{ equ } 0ah \\
\text{ch78} & \text{ equ } 0bh \\
\text{band} & \text{ equ } 0ch \\
\text{free} & \text{ equ } 0dh \\
\text{data} & \text{ equ } 0eh \\
\text{memory} & \text{ equ } 0fh
\end{align*} \]

\[ \begin{align*}
\text{org} & \ 2000h \\
\text{ajmp} & \ \text{mulai} \\
\text{org} & \ 2100h
\end{align*} \]

\[ \begin{align*}
\text{DELAY 4 ms} \\
\text{---------------}
\end{align*} \]

\[ \begin{align*}
\text{DELAY4M} & \ \text{MOV} \ R7,\#70 \\
\text{DEL4M} & \ \text{MOV} \ R6,\#250 \\
\text{DJNZ} & \ R6,\$ \\
\text{DJNZ} & \ R7,\text{DEL4M} \\
\text{RET}
\end{align*} \]
START

SETB P1.7 ; START CONDITION / SCLOCK HIGH
CLR P1.6 ;
SETB P1.6 ; SCLOCK HI TO START CONDITION
CLR P1.7 ; SDA HI TO LOW TO START CONDITION
CLR P1.6 ;
RET

STOP

SETB P1.6 ; STOP CONDITION / SCLOCK HIGH
SETB P1.7 ;
RET

PROTOCOL WRITE

PROTOCOL MOV R2,#8
TERUS RLC A
MOV P1.7,C
SETB P1.6
CLR P1.6
DJNZ R2,TERUS
SETB P1.7
SETB P1.6
MOV C,P1.7 ; "ACK" SAVED IN CARRY
CLR P1.6
CLR P1.7
RET

WRITE

ACALL START
MOV A,#0A0H ; CODE WRITE MEMORY
ACALL PROTOCOL
MOV A, MEMORY
ACALL PROTOCOL
MOV A, DATA
ACALL PROTOCOL
ACALL STOP
MOV R7,#250 ; DELAY WRITE TO SERIAL MEMORY
DJNZ R7,$
RET

; READ

READ ACALL START
MOV A,#0A0H ;CODE WRITE UTK MENENTUKAN ALAMAT
ACALL PROTOCOL
MOV A,MEMORY
ACALL PROTOCOL
ACALL START
MOV A,#0A1H ;CODE BACA MEMORY
ACALL PROTOCOL
MOV R2,#8
SETB P1.7 ;SDA --> INPUT
BACA
SETB P1.6
MOV C,P1.7
RLC A
CLR P1.6
DJNZ R2,BACA
SETB P1.7 ;CEK "NO ACK"
SETB P1.6
CLR P1.6
CLR P1.7
ACALL STOP
MOV DATA,A
RET

; DELAY ( 2 SECON )

-----------------------
DELAY2 MOV R5,#3
DEL5 MOV R6,#250
DEL6 MOV R7,#250
DJNZ R7,$
DJNZ R6,DEL6
DJNZ R5,DEL5
RET

; ENABLE PULSE for LCD

-----------------------
ENABLE MOV DPTR,#PA
ANL A,#0FH
MOvik @DPTR,A
ORL A,#20H
MOVX @DPTR,A
ANL A,#0FH
MOVX @DPTR,A
ACALL DELAY4M
RET

; CONTROL LCD

-------------------------------
LCDCONTROL MOV FREE,A
SWAP A
ACALL ENABLE
MOV A,FREE
ACALL ENABLE
RET

; INISILISASI LCD 4 BIT

INITL4BIT MOV DPTR,#PA
MOV R5,#3
WAIT MOV A,#3H
MOVX @DPTR,A
ORL A,#20H
MOVX @DPTR,A
ANL A,#0FH
MOVX @DPTR,A
ACALL DELAY4M
DJNZ R5,WAIT

WAITFUNCTION MOV A,#2H ;FUNCTION SET
MOVX @DPTR,A
ORL A,#20H
MOVX @DPTR,A
ANL A,#0FH
MOVX @DPTR,A
ACALL DELAY4M

MOV A,#2FH ;FUNCTION SET
ACALL LCDCONTROL
MOV A,#0CH ;DISPLAY ON
ACALL LCDCONTROL
MOV A,#01H ;DISPLAY CLEAR
ACALL LCDCONTROL
MOV A,#06H ;ENTRY
ACALL  LCDCONTROL
RET

; CETAK TO LCD
CETAK  ANL  A,#0FH
ORL  A,#10H
MO VX  @DPTR,A
ORL  A,#20H
MO VX  @DPTR,A
ANL  A,#1FH
MO VX  @DPTR,A
MOV  R7,#50
DJNZ  R7,$
RET

; DISPLAY LCD
LCD  MOV  DPTR,#PA
MOV  FREE,A
SWAP  A
ACALL  CETAK
MOV  A, FREE
ACALL  CETAK
RET

; delay
delay  mov  R7,#250
dela  mov  R6,#250
djnz  R6,$
djnz  R7,dela
RET

; loading data equaliser
loading  mov  R6,#4
         mov  memory,#10h ;offset address 10h l2C
         mov  R0,#08h
nextload  acall  read
inc  memory
mov  @$R0, data
inc r0
djnz r6,nextload
ret

; value of set saved into I2C
;-------------------------------
saveto_i2c mov r0,#08h
    mov r6,#4
    mov memory,#10h
nextsave mov data,@r0
    acall write
    inc r0
    inc memory
djnz r6,nextsave
ret

; serial output
;-------------------------------
serial_out mov r7,#8
nextserial mov a,ch12
    rlc a
    mov a,ch12,c
    rl a
    mov ch12,a
    mov a,ch34
    rlc a
    mov a,ch34,c
    rl a
    mov ch34,a
    mov a,ch56
    rlc a
    mov a,ch56,c
    rl a
    mov ch56,a
    mov a,ch78
    rlc a
    mov a,ch78,c
    mov a,ch78
rl a
mov ch78,a
clr p1.0  ; pulse serclock
setb p1.0
djnz r7,nextserial
clr p1.1  ; lacth enable
setb p1.1
ret

;-------------------------------
; set equiliser
;-------------------------------
set mov a,band
jz back
mov dptr,#jumptable
mov c,acc.0
mov psw.1,c
clr c
dec a
rrc a
mov b,#2
mul ab
jmp @a+dptr
back ret
jumptable ajmp band_ch12
ajmp band_ch34
ajmp band_ch56
ajmp band_ch78

;-------------------------------
Band 1 & 2 -------------------------------
band_ch12 mov a,ch12
jnb psw.1,ch_even12
inc ch12
jnb acc.3,pass_ch12 ; cek apakah ch1 = 7 ?
anl ch12,#0f0h
ajmp back

ch_even12 swap a
inc a
swap a
mov ch12,a
jnb acc.7,pass_ch12 ; cek apakah ch2 = 7 ?
anl ch12,#0fh
ajmp back
pass_ch12 ajmp back

;-------------------------------
Band 3 & 4 -------------------------------
band_ch34  mov  a,ch34
        jnb  psw.1,ch_even34
        inc  ch34
        jnb  acc.3,pass_ch34 ;cek apakah ch3 = 7 ?
        anl  ch34,#0fh
        ajmp  back

ch_even34  swap  a
        inc  a
        swap  a
        mov  ch34,a
        jnb  acc.7,pass_ch34 ;cek apakah ch4 = 7 ?
        anl  ch34,#0fh
        pass_ch34 ajmp  back

pass_ch34  ;------------------------------- Band 5 & 6 -------------------------------

band_ch56  mov  a,ch56
        jnb  psw.1,ch_even56
        inc  ch56
        jnb  acc.3,pass_ch56 ;cek apakah ch1 = 7 ?
        anl  ch56,#0fh
        ajmp  back

ch_even56  swap  a
        inc  a
        swap  a
        mov  ch56,a
        jnb  acc.7,pass_ch56
        anl  ch56,#0fh
        pass_ch56 ajmp  back

pass_ch56  ;------------------------------------------------- Band 7 & 8 -------------------------------

band_ch78  mov  a,ch78
        jnb  psw.1,ch_even78
        inc  ch78
        jnb  acc.3,pass_ch78 ;cek apakah ch1 = 7 ?
        anl  ch78,#0fh
        ajmp  back

ch_even78  swap  a
        inc  a
        swap  a
        mov  ch78,a
        jnb  acc.7,pass_ch78
        anl  ch78,#0fh
        pass_ch78 ajmp  back
; select band equaliser

select_band inc band
    mov a.band
    cjne a, #9, sel_bandpres
    mov band,#0

sel_bandpres jnb p1.6,$ ; wait until not keypressed
    ret

; display lcd

display mov a, #80h
    acall lcdcontrol ; baris 1
    mov a, band
    mov b, #16
    mul ab

    mov dpdr, #table_kata
    add a, dpl
    mov dpl, a
    mov a, #0
    addc a, dph
    mov dph, a
    mov r2, #16

nextchar mov a, #0
    movc a, @a+dpdr
    push dph
    push dpl
    acall lcd
    pop dpl
    pop dph
    inc dpdr
    djnz r2, nextchar

mov a, #0c0h ; line 2
    acall lcdcontrol
    mov r2, #7

dispblank mov a, #20h ; disp 7th times
    acall lcd
    djnz r2, dispblank

mov a, band
    jnz nilai_set ; if no band selection then
    mov r2, #10 ; lcd line 2 blank
printblank mov a,#20h ; cetak space
acall lcd
djnz r2, printblank
ajmp escdisplay

nilai_set ; mov c, acc.0
; mov psw.1, c
; clr c
; dec a
; rrc a
; mov b, #2
; mul ab
; mov dptr, #tabledisp_ch
; jmp @a+dptr

escdisplay ret

table_kata db 'No Band Selected'
db ' Band 1 '
db ' Band 2 '
db ' Band 3 '
db ' Band 4 '
db ' Band 5 '
db ' Band 6 '
db ' Band 7 '
db ' Band 8 '

tabledisp_ch ajmp loadch12
ajmp loadch34
ajmp loadch56
ajmp loadch78

;------------------------ load value ch12 to lcd ------------------------
loadch12 jnb psw.1, evench12 ; ch1 or ch2 ?
mov a, ch12
ani a, #0fh
orl a, #30h ; disp number in ASCII
acall lcd
ajmp tabledisp_ch

evench12 mov a, ch12
swap a
ani a, #0fh
orl a, #30h
acall lcd
ajmp tabledisp_ch

;------------------------ load value ch34 to lcd ------------------------
loadch34 jnb psw.1, evench34 ; ch3 or ch4 ?
mov a,ch34
ani a,#0fh
orl a,#30h
; disp number in ASCII

acall lcd
ajmp tabledisp_ch
evench34
mov a,ch34
swap a
ani a,#0fh
orl a,#30h
acall lcd
ajmp tabledisp_ch

;--------------------------- load value ch56 to lcd ---------------------------
loadch56
jnb psw.1,evench56 ; ch5 or ch6 ?
mov a,ch56
ani a,#0fh
orl a,#30h
; disp number in ASCII

acall lcd
ajmp tabledisp_ch
evench56
mov a,ch56
swap a
ani a,#0fh
orl a,#30h
acall lcd
ajmp tabledisp_ch

;------------------------------- load value ch78 to lcd -------------------------------
loadch78
jnb psw.1,evench78 ; ch7 or ch8 ?
mov a,ch78
ani a,#0fh
orl a,#30h
; disp number in ASCII

acall lcd
ajmp tabledisp_ch
evench78
mov a,ch78
swap a
ani a,#0fh
orl a,#30h
acall lcd
ajmp tabledisp_ch

; main program

mulai
mov sp,#40h
acall delay
mov dptr,#pcw
mov a,#cw
movx @dptr,a
acall initlcd4bit
acall loading
acall serial_out
mov band,#1
acall display
setb p1.6
setb p1.7

ulang mov dptr,#pb
movx a,@dptr
jb acc.0,cek_set ;tombol band ditekan ?
;jb p1.6,cek_set ;tombol band ditekan ?
acall select_band
acall display
ajmp ulang

cek_set jb acc.1,ulang
;jb p1.7,pas ;tombol set ditekan ?
acall set
acall serial_out
acall display
acall saveto_i2c

pas ajmp ulang
Features
- Write Protect Pin for Hardware Data Protection
- Utilizes Different Array Protection Compared to the AT24C02/04/08
- 5.0 (V_{CC} = 4.5V to 5.5V)
- 2.7 (V_{CC} = 2.7V to 5.5V)
- 2.5 (V_{CC} = 2.5V to 5.5V)
- 1.8 (V_{CC} = 1.8V to 5.5V)
- Wire Serial Interface
  - write Trigger, Filtered Inputs for Noise Suppression
  - Directional Data Transfer Protocol
  - 0 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Clock Rate
- Partial Page Writes are Allowed
- If-timed Write Cycle (10 ms max)
- Endurance: One Million Write Cycles
- Data Retention: 100 Years
- ESD Protection: >3000V
- Automotive Grade and Extended Temperature Devices Available
- Available in 8-pin PDIP, 8-lead SOIC, and 8-lead TSSOP Packages

Description
AT24C02A/04A/08A provides 2048/4096/8192 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 256/512/1024 words bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C02A/04A/08A is available in space saving 8-pin PDIP, 8-lead JEDEC SOIC, and 8-lead TSSOP (AT24C02A/04A) packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), 2.5V (2.5V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

Configurations

<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>A2</td>
<td>Address Inputs</td>
</tr>
<tr>
<td>/</td>
<td>Serial Data</td>
</tr>
<tr>
<td>\</td>
<td>Serial Clock Input</td>
</tr>
<tr>
<td></td>
<td>Write Protect</td>
</tr>
<tr>
<td></td>
<td>No Connect</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>8-pin PDIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0 1</td>
</tr>
<tr>
<td>A1 2</td>
</tr>
<tr>
<td>A2 3</td>
</tr>
<tr>
<td>GND 4</td>
</tr>
<tr>
<td>8 VCC</td>
</tr>
<tr>
<td>7 WP</td>
</tr>
<tr>
<td>6 SCL</td>
</tr>
<tr>
<td>5 SDA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>8-lead SOIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0 1</td>
</tr>
<tr>
<td>A1 2</td>
</tr>
<tr>
<td>A2 3</td>
</tr>
<tr>
<td>GND 4</td>
</tr>
<tr>
<td>8 VCC</td>
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<tr>
<td>7 WP</td>
</tr>
<tr>
<td>6 SCL</td>
</tr>
<tr>
<td>5 SDA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>8-lead TSSOP</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0 1</td>
</tr>
<tr>
<td>A1 2</td>
</tr>
<tr>
<td>A2 3</td>
</tr>
<tr>
<td>GND 4</td>
</tr>
<tr>
<td>8 VCC</td>
</tr>
<tr>
<td>7 WP</td>
</tr>
<tr>
<td>6 SCL</td>
</tr>
<tr>
<td>5 SDA</td>
</tr>
</tbody>
</table>
**Absolute Maximum Ratings**

- Operating Temperature: -55°C to +125°C
- Storage Temperature: -65°C to +150°C
- Voltage on Any Pin with Respect to Ground: -1.0V to +7.0V
- Maximum Operating Voltage: 6.25V
- Output Current: 5.0 mA

*N.TICE*: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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**Block Diagram**

![Block Diagram](image)

**Pin Description**

**SERIAL CLOCK (SCL):** The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

**SERIAL DATA (SDA):** The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may wire-ORed with any number of other open-drain or open collector devices.

**DEVICE/PAGE ADDRESSES (A2, A1, A0):** The A2, A1 and A0 pins are device address inputs that are hard wired to the AT24C02A. As many as eight 2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

The AT24C04A uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no connect.

The AT24C08A only uses the A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects.

**WRITE PROTECT (WP):** The AT24C02A/04A/08A has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect

**AT24C02A/04A/08A**
Features
- Compatible with MCS-51™ Products
- 4 Kbytes of In-System Reprogrammable Flash Memory
  Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

Description
The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4 Kbytes of Flash Programmable and Erasable Read Only Memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

Pin Configurations
(continued)
description (Continued)

The AT89C51 provides the following standard features: 4 bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports no software selectable power saving modes. The Idle mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but eezes the oscillator disabling all other chip functions until the next hardware reset.

Port 0
Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1
Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL) because of the internal pullups.

Port 1 also receives the low-order address bytes during Flash programming and program verification.

Port 2
Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3
Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

<table>
<thead>
<tr>
<th>Port Pin</th>
<th>Alternate Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>P3.0</td>
<td>RXD (serial input port)</td>
</tr>
<tr>
<td>P3.1</td>
<td>TXD (serial output port)</td>
</tr>
<tr>
<td>P3.2</td>
<td>INT0 (external interrupt 0)</td>
</tr>
<tr>
<td>P3.3</td>
<td>INT1 (external interrupt 1)</td>
</tr>
<tr>
<td>P3.4</td>
<td>T0 (timer 0 external input)</td>
</tr>
<tr>
<td>P3.5</td>
<td>T1 (timer 1 external input)</td>
</tr>
<tr>
<td>P3.6</td>
<td>WR (external data memory write strobe)</td>
</tr>
<tr>
<td>P3.7</td>
<td>RD (external data memory read strobe)</td>
</tr>
</tbody>
</table>

Port 3 also receives some control signals for Flash programming and programming verification.

RST
Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/PROG
Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8E8. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

PSEN
Program Store Enable is the read strobe to external program memory.

(continued)
in Description (Continued)

When the AT89C51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

**XENP**

*External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to EFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset.**

*: should be strapped to VCC for internal program executions.

*This pin also receives the 12-volt programming enable voltage (Vpp) during Flash programming, for parts that require 12-volt Vpp.

**TAL1**

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

**TAL2**

Output from the inverting oscillator amplifier.

**Oscillator Characteristics**

(TAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal locking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

**Idle Mode**

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hard-

**Figure 1. Oscillator Connections**

![Oscillator Connections Diagram]

Notes: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

**Figure 2. External Clock Drive Configuration**

![External Clock Drive Configuration Diagram]

**Status of External Pins During Idle and Power Down**

<table>
<thead>
<tr>
<th>Mode</th>
<th>Program Memory</th>
<th>ALE</th>
<th>PSEN</th>
<th>PORT0</th>
<th>PORT1</th>
<th>PORT2</th>
<th>PORT3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Idle</td>
<td>Internal</td>
<td>1</td>
<td>1</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
<tr>
<td>Idle</td>
<td>External</td>
<td>1</td>
<td>1</td>
<td>Float</td>
<td>Data</td>
<td>Address</td>
<td>Data</td>
</tr>
<tr>
<td>Power Down</td>
<td>Internal</td>
<td>0</td>
<td>0</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
<tr>
<td>Power Down</td>
<td>External</td>
<td>0</td>
<td>0</td>
<td>Float</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
</tbody>
</table>

4 AT89C51
Advance Information

Analog Multiplexers/ Demultiplexers

High-Performance Silicon-Gate CMOS

The MC54/74HC4051, MC54/74HC4052, and MC54/74HC4053 utilize silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from VCC to VEE).

The HC4051, HC4052, and HC4053 are identical in pinout to the metal gate MC14051B, MC14052B, and MC14053B. The Channel Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is high, all analog switches are turned off.

The Channel-Select and Enable inputs are compatible with standard CMOS outputs, with pullup resistors, they are compatible with LSTTL outputs.

These devices have been designed so that the ON resistance (RON) is more linear over input voltage than RON of metal-gate CMOS analog switches:

For multiplexers/demultiplexers with channel select latches, see HC4251, HC4252, and HC4253.

- Fast Switching and Propagation Speeds
- Low Crosskast Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range (VCC – VEE) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range (VCC – GND) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance than Metal-Gate CMOS Analog Switches
- Low Noise
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: HC4051 = 184 FETs or 46 Equivalent Gates
  HC4052 = 184 FETs or 42 Equivalent Gates
  HC4053 = 184 FETs or 39 Equivalent Gates

LOGIC DIAGRAM

MC54/74HC4051
Single-Pole, 8-Position Plus Common Off

FUNCTION TABLE

<table>
<thead>
<tr>
<th>Enable</th>
<th>Select</th>
<th>ON Channels</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>B</td>
<td>A</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>A</td>
<td>X</td>
</tr>
<tr>
<td>H</td>
<td>A</td>
<td>X</td>
</tr>
</tbody>
</table>

The document contains information on new products. Specifications and item numbers are subject to change without notice.
MC54/74HC4051 • MC54/74HC4052 • MC54/74HC4053

MC54/74HC4052
Double Pole, 4-Position
Plus Common Off

LOGIC DIAGRAM

PIN ASSIGNMENT

FUNCTION TABLE

MC54/74HC4053
Triple Single Pole, Double-Position
Plus Common Off

LOGIC DIAGRAM

PIN ASSIGNMENT

FUNCTION TABLE

NOTE: This device allows independent control of each switch. Channel Select input A controls the X Switch, input B controls the Y Switch, and input C controls the Z Switch.
### MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Positive DC Supply Voltage (Ref. to GND)</td>
<td>-0.5 to +7.0</td>
<td>V</td>
</tr>
<tr>
<td>VEE</td>
<td>Negative DC Supply Voltage (Ref. to GND)</td>
<td>-0.5 to 14.0</td>
<td>V</td>
</tr>
<tr>
<td>IDC</td>
<td>Analog Input Voltage</td>
<td>-7.0 to +0.5</td>
<td>V</td>
</tr>
<tr>
<td>VCC</td>
<td>Digital Input Voltage (Ref. to GND)</td>
<td>-1.5 to VEE + 1.5</td>
<td>V</td>
</tr>
<tr>
<td>ICC</td>
<td>DC Current into or Out of Any Pin</td>
<td>1.25</td>
<td>mA</td>
</tr>
<tr>
<td>Tst</td>
<td>Power Dissipation in SOT Air</td>
<td>500</td>
<td>mW</td>
</tr>
<tr>
<td>Tst</td>
<td>Storage Temperature</td>
<td>-65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>Tst</td>
<td>Lead Temperature, 1 mm from Case</td>
<td>200</td>
<td>°C</td>
</tr>
</tbody>
</table>

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.*

### RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Positive DC Supply Voltage (Ref. to GND)</td>
<td>2.0</td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td>VEE</td>
<td>Negative DC Supply Voltage (Ref. to GND)</td>
<td>-5.0</td>
<td>GND</td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Analog Input Voltage</td>
<td>VEE</td>
<td>VCC</td>
<td>V</td>
</tr>
<tr>
<td>VIO</td>
<td>Digital Input Voltage (Ref. to GND)</td>
<td>1.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>TA</td>
<td>Operating Temperature, All Package Types</td>
<td>-56 to +125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>k</td>
<td>Input Rise and Fall Time, Input</td>
<td>0</td>
<td>1000</td>
<td>ns</td>
</tr>
</tbody>
</table>

*For voltage drops across the switch greater than 1.2 V (switch on), excessive VCC current may be drawn; i.e., the current out of the switch may contain both VCC and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.*

### DC ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>VCC</th>
<th>Guaranteed Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VRH</td>
<td>Minimum High-Level Input Voltage, Channel-Select or Enable Inputs</td>
<td>Rth = Per Spec</td>
<td>2.0</td>
<td>1.5</td>
</tr>
<tr>
<td>VRH</td>
<td>Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs</td>
<td>Rth = Per Spec</td>
<td>4.5</td>
<td>3.15</td>
</tr>
<tr>
<td>VRH</td>
<td>Maximum Input Leakage Current, Channel-Select or Enable Inputs</td>
<td>VCC = VCC or GND, VEE = -8.5 V</td>
<td>6.0</td>
<td>2.0</td>
</tr>
<tr>
<td>ICC</td>
<td>Maximum Operating Supply Current (per Package)</td>
<td>Channel Select = VCC or GND Enable = VCC or GND</td>
<td>VCC = VCC or GND</td>
<td>VEE = 0 V</td>
</tr>
</tbody>
</table>

*NOTE: Information on typical parameter values can be found in Chapter 4.*

**MC54/74HC4051**

MOTOROLA HIGH-SPEED CMOS LOGIC DATA

5-554
### DC Electrical Characteristics

**Analog Section**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>VCC</th>
<th>VEE</th>
<th>Guaranteed Limit</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{on}$</td>
<td>Maximum &quot;ON&quot; Resistance</td>
<td>$V_{in} = V_{IL} \text{ or } V_{IH}$</td>
<td>4.5</td>
<td>0.0</td>
<td>190</td>
<td>100 to 125</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{in} = V_{CC} \text{ or } V_{EE}$</td>
<td>4.5</td>
<td>-4.5</td>
<td>120</td>
<td>100 to 125</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{g} \leq 2.0 \text{ mA}$ (Figures 1, 2)</td>
<td>6.0</td>
<td>-8.0</td>
<td>100</td>
<td>100 to 125</td>
</tr>
<tr>
<td>$3R_{on}$</td>
<td>Maximum Difference in &quot;ON&quot; Resistance Between Any Two Channels in the Same Package</td>
<td>$V_{in} = V_{IL} \text{ or } V_{IH}$</td>
<td>4.5</td>
<td>0.0</td>
<td>150</td>
<td>100 to 125</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{in} = V_{CC} \text{ or } V_{EE}$ (Endpoints)</td>
<td>4.5</td>
<td>-4.5</td>
<td>100</td>
<td>100 to 125</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{g} \leq 2.0 \text{ mA}$ (Figures 1, 2)</td>
<td>8.0</td>
<td>-8.0</td>
<td>80</td>
<td>80 to 100</td>
</tr>
<tr>
<td>$I_{on}$</td>
<td>Maximum On-Channel Leakage Current, Any One Channel</td>
<td>$V_{in} = V_{IL} \text{ or } V_{IH}$</td>
<td>8.0</td>
<td>-6.0</td>
<td>0.1</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{in} = V_{CC} \text{ or } V_{EE}$</td>
<td>8.0</td>
<td>-6.0</td>
<td>0.2</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{in} = V_{CC} \text{ or } V_{EE}$</td>
<td>8.0</td>
<td>-6.0</td>
<td>0.1</td>
<td>1.0</td>
</tr>
</tbody>
</table>

### AC Electrical Characteristics

($C_{i} = 50 \text{ pF}, \text{ Input } t_{i} = 1 \times 8 \text{ ns}$)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>VCC</th>
<th>Guaranteed Limit</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PLH}$</td>
<td>Maximum Propagation Delay, Channel-Select to Analog Output (Figure 5)</td>
<td>2.0</td>
<td>370</td>
<td>465</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5</td>
<td>74</td>
<td>93</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8.0</td>
<td>63</td>
<td>75</td>
</tr>
<tr>
<td></td>
<td>Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)</td>
<td>2.0</td>
<td>80</td>
<td>95</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5</td>
<td>12</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8.0</td>
<td>10</td>
<td>13</td>
</tr>
<tr>
<td>$t_{PLZ}$</td>
<td>Maximum Propagation Delay, Enable to Analog Output (Figure 11)</td>
<td>2.0</td>
<td>200</td>
<td>264</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5</td>
<td>58</td>
<td>73</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8.0</td>
<td>69</td>
<td>82</td>
</tr>
<tr>
<td></td>
<td>Maximum Propagation Delay, Enable to Analog Output (Figure 11)</td>
<td>2.0</td>
<td>345</td>
<td>435</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5</td>
<td>69</td>
<td>87</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8.0</td>
<td>59</td>
<td>74</td>
</tr>
<tr>
<td>$C_{in}$</td>
<td>Maximum Input Capacitance, Channel Select or Enable Inputs</td>
<td></td>
<td>-</td>
<td>10</td>
</tr>
<tr>
<td>$C_{J0}$</td>
<td>Maximum Capacitance, Analog I/O, All Switches Off</td>
<td>Common O/I: HC4051</td>
<td>-</td>
<td>35</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HC4052</td>
<td>-</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HC4053</td>
<td>-</td>
<td>50</td>
</tr>
</tbody>
</table>

**Notes:**
1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

### Power Dissipation

**Power Disipation Capacitance (Per Package) (Figure 13)**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Power Dissipation Capacitance (Per Package) (Figure 13)</th>
<th>Typical @ 35°C, VCC = 5.0 V, VEE = 0 V</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$C_{PD}$</td>
<td>$C_{PD} = C_{PD} \times VCC^2 + \Delta V \times VCC$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>For load considerations, see Chapter 4.</td>
</tr>
</tbody>
</table>

**Typical Values:**

- 45 (HC4051)
- 80 (HC4052)
- 45 (HC4053)

---

MOTOROLA HIGH-SPEED CMOS LOGIC DATA
### ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0.0 V)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>VCC V</th>
<th>VEE V</th>
<th>Limit*</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW</td>
<td>Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 8)</td>
<td>$f_{IN} = 1$ MHz Sine Wave</td>
<td>2.25</td>
<td>2.25</td>
<td>80 95 120</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Adjust $f_{IN}$ Voltage to Obtain 6 dBm at VGS</td>
<td>4.50</td>
<td>4.50</td>
<td>80 95 120</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Increase $f_{IN}$ Frequency Until dB Meter</td>
<td>6.00</td>
<td>6.00</td>
<td>80 95 120</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Reads - 3 dB</td>
<td>$RL = 50$ Q, $CL = 10$ pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Off Channel Feedthrough Isolation (Figure 7)</td>
<td>$f_{IN} = 1$ MHz Sine Wave</td>
<td>2.25</td>
<td>2.25</td>
<td>-50</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Adjust $f_{IN}$ Voltage to Obtain 0 dBm at VGS</td>
<td>4.50</td>
<td>4.50</td>
<td>-50</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{IN} = 10$ kHz, $RL = 800$ Q, $CL = 50$ pF</td>
<td>6.00</td>
<td>6.00</td>
<td>-50</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Feedthrough Noise, Channel Select Input to Common G/I (Figure 8)</td>
<td>$f_{IN} = 1$ MHz Square Wave</td>
<td>2.25</td>
<td>2.25</td>
<td>80 95 120</td>
<td>mvpp</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Adjust $RL$ at Setups so that $IG = 0$ A</td>
<td>4.50</td>
<td>4.50</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Enable G/VD</td>
<td>6.00</td>
<td>6.00</td>
<td>120</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$RL = 800$ Q, $CL = 50$ pF</td>
<td>6.00</td>
<td>6.00</td>
<td>150</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$RL = 10$ kHz, $CL = 10$ pF</td>
<td>6.00</td>
<td>6.00</td>
<td>150</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CrossTalk Between Any Two Switches (Figure 12)</td>
<td>$f_{IN} = 1$ MHz Sine Wave</td>
<td>2.25</td>
<td>2.25</td>
<td>-50</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Adjust $f_{IN}$ Voltage to Obtain 0 dBm at VGS</td>
<td>4.50</td>
<td>4.50</td>
<td>-50</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{IN} = 10$ kHz, $RL = 600$ Q, $CL = 50$ pF</td>
<td>6.00</td>
<td>6.00</td>
<td>-50</td>
<td></td>
</tr>
<tr>
<td></td>
<td>THD</td>
<td>Total Harmonic Distortion (Figure 14)</td>
<td>2.25</td>
<td>2.25</td>
<td>0.10</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{IN} = 1$ kHz, $RL = 10$ kHz, $CL = 50$ pF</td>
<td>4.50</td>
<td>4.50</td>
<td>0.08</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>THD = THDMeasured + THDSource</td>
<td>6.00</td>
<td>6.00</td>
<td>0.05</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>VGS = 4.0 Vpp sine wave</td>
<td>2.25</td>
<td>2.25</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>VGS = 8.0 Vpp sine wave</td>
<td>4.50</td>
<td>4.50</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>VGS = 11.0 Vpp sine wave</td>
<td>6.00</td>
<td>6.00</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* limits not tested. determined by design and verified by qualification.
Figure 1a. Typical On Resistance, $V_{CC} - V_{EE} = 2.0$ V

Figure 1b. Typical On Resistance, $V_{CC} - V_{EE} = 4.5$ V

Figure 1c. Typical On Resistance, $V_{CC} - V_{EE} = 6.0$ V

Figure 1d. Typical On Resistance, $V_{CC} - V_{EE} = 9.0$ V

Figure 1e. Typical On Resistance, $V_{CC} - V_{EE} = 12.0$ V

Figure 2. On Resistance Test Set-Up
MC54/74HC4051 • MC54/74HC4052 • MC54/74HC4053

Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up

Figure 6. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

Figure 7. Off-Channel Feedthrough Isolation, Test Set-Up

Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set-Up

MOTOROLA HIGH-SPEED CMOS LOGIC DATA
5-558
Figure 9a. Propagation Delays, Channel Select to Analog Out

Figure 9b. Propagation Delay, Test Set-Up Channel Select to Analog Out

Figure 10a. Propagation Delays, Analog In to Analog Out

Figure 10b. Propagation Delay, Test Set-Up Analog In to Analog Out

Figure 11a. Propagation Delays, Enable to Analog Out

Figure 11b. Propagation Delay, Test Set-Up Enable to Analog Out

MOTOROLA HIGH-SPEED CMOS LOGIC DATA
MC54/74HC4051·MC54/74HC4052·MC54/74HC4053

*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set-Up

*Includes all probe and jig capacitance.

Figure 14a. Total Harmonic Distortion, Test Set-Up

Figure 13. Power Dissipation Capacitance, Test Set-Up

Figure 14b. Plot, Harmonic Distortion

MOTORO FRIEND CMOS LOGIC DATA

5-560
APPLICATIONS INFORMATION

The channel Select and Enable control pins should be at digital CMOS logic levels. VCC being recognized as a logic high and GND (GND) logic level as a logic low in this example.

\[ VCC \approx 5 \text{ V logic high} \]
\[ \text{GND} \approx 0 \text{ V logic low} \]

The maximum analog voltage swings are determined by the supply voltages, VCC and VEE. The positive peak analog voltage should not exceed VCC. Similarly, the negative peak analog voltage should not go below VEE. In this example, the difference between VEE and VCC is ten volts. Therefore, using the configuration in Figure 15, a maximum analog signal of ten volts peak to peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to VCC or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

\[ VCC - \text{GND} = 2 \text{ to } 8 \text{ volts} \]
\[ VEE - \text{GND} = 0 \text{ to } -8 \text{ volts} \]
\[ VCC - VEE = 2 \text{ to } 12 \text{ volts} \]
\[ \text{and VEE }\text{s GND} \]

When voltage transients above VCC and/or below VEE are anticipated on the analog channels, external Germanium or Schottky diodes (D4) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

---

**Figure 15. Application Example**

**Figure 16. External Germanium or Schottky Clipping Diodes**

**Figure 17. Interfacing LSTTL/NMOS to CMOS Inputs**

---

MOTOROLLA HIGH-SPEED CMOS LOGIC DATA
FUNCTION DIAGRAM, HC4051

FUNCTION DIAGRAM, HC4052

MOTOROLA HIGH-SPEED CMOS LOGIC DATA
5-562
SN54AHCT595, SN74AHCT595
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS
SCL3744A - MAY 1997 - REVISED JUNE 1997

*Inputs Are TTL-Voltage Compatible
• EPIC™ (Enhanced-Performance Implanted CMOS) Process
• 8-Bit Serial-In, Parallel-Out Shift
• Shift Register Has Direct Clear
• Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

Description

The 'AHCT595 contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear (SRCLR) input, serial (SER) input, and serial outputs for cascading. When the output-enable (OE) input is high, the outputs are in the high-impedance state.

Both the shift register clock (RCLK) and storage register clock (SRCLK) are positive-edge triggered. If both clocks are connected together, the shift register is always one clock pulse ahead of the storage register.

The SN54AHCT595 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74AHCT595 is characterized for operation from -40°C to 85°C.

SN54AHCT595... J OR W PACKAGE
SN74AHCT595... D, DB, N, OR PW PACKAGE

(TOP VIEW)
SN54AHCT595, SN74AHCT595
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS
SCL374A - MAY 1997 - REVISED JUNE 1997

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, DB, J, N, PW, and W packages.
logic diagram (positive logic)

Pin numbers shown are for the D, DB, J, N, PW, and W packages.

Texas Instruments
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
3–463
absolute maximum ratings over operating free-air temperature range†

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage range, VCC</td>
<td>-0.5 V</td>
<td>7 V</td>
<td>-0.5 V</td>
<td>7 V</td>
</tr>
<tr>
<td>Input voltage range, VIL (see Note 1)</td>
<td>-0.5 V to VCC + 0.5 V</td>
<td>-20 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Typical output current, IO (VOL = 0 to VCC)</td>
<td>125 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Continuous current through VCC or GND</td>
<td>150 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Storage temperature range, T-storage       | -65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SN54AHCT595</th>
<th>SN74AHCT595</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC Supply voltage</td>
<td>4.5 V</td>
<td>4.5 V</td>
</tr>
<tr>
<td>VIL High-level input voltage</td>
<td>0.8 V</td>
<td>0.8 V</td>
</tr>
<tr>
<td>VIL Low-level input voltage</td>
<td>0 V</td>
<td>0 V</td>
</tr>
<tr>
<td>VIL Input voltage</td>
<td>0.8 V</td>
<td>0.8 V</td>
</tr>
<tr>
<td>VO Output voltage</td>
<td>0 VCC</td>
<td>0 VCC</td>
</tr>
<tr>
<td>VOH High-level output current</td>
<td>-8 mA</td>
<td>-8 mA</td>
</tr>
<tr>
<td>VOL Low-level output current</td>
<td>8 mA</td>
<td>8 mA</td>
</tr>
<tr>
<td>Input transition rise or fall rate</td>
<td>20 ns</td>
<td>20 ns</td>
</tr>
<tr>
<td>Operating free-air temperature</td>
<td>-55°C</td>
<td>125°C</td>
</tr>
</tbody>
</table>

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>TEST CONDITIONS</th>
<th>VCC</th>
<th>T_A = 25°C</th>
<th>SN54AHCT595</th>
<th>SN74AHCT595</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOH</td>
<td>IQH = -50 µA</td>
<td>4.5 V</td>
<td>4.4</td>
<td>4.5</td>
<td>4.4</td>
<td>4.4</td>
</tr>
<tr>
<td>VOL</td>
<td>IQL = 50 µA</td>
<td>4.5 V</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>L</td>
<td>VI = VCC or GND</td>
<td>5.5 V</td>
<td>0.36</td>
<td>0.44</td>
<td>0.44</td>
<td>μA</td>
</tr>
<tr>
<td>ICC</td>
<td>VI = VCC or GND, IO = 0</td>
<td>5.5 V</td>
<td>4</td>
<td>10</td>
<td>40</td>
<td>μA</td>
</tr>
<tr>
<td>ΔICC†</td>
<td>One input at 3.4 V, Other inputs at VCC or GND</td>
<td>5.5 V</td>
<td>1.35</td>
<td>1.5</td>
<td>1.5</td>
<td>mA</td>
</tr>
<tr>
<td>Ci</td>
<td>VI = VCC or GND</td>
<td>5.5 V</td>
<td>2</td>
<td>10</td>
<td>10</td>
<td>pF</td>
</tr>
</tbody>
</table>

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or VCC.
SN54AHCT595, SN74AHCT595
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS

SCLS374A - MAY 1997 - REVISED JUNE 1997

Timing requirements over recommended operating free-air temperature range,
$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Action</th>
<th>$I_w$</th>
<th>$I_{su}$</th>
<th>$I_h$</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRCLK high or low</td>
<td>Pulse duration</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>RCLK high or low</td>
<td></td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>SRCLR low</td>
<td></td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>SR before SRCLKT</td>
<td>Setup time</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>SRCLKT before RCLKT</td>
<td></td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>SRCLK low before RCLKT</td>
<td></td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>SRCLK high (inactive) before SRCLKT</td>
<td></td>
<td>2.5</td>
<td>2.5</td>
<td>2.5</td>
</tr>
<tr>
<td>SRCLR low before RCLKT</td>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>SRCLKT low after RCLKT</td>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Timing requirements over recommended operating free-air temperature range,
$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

Switching characteristics over recommended operating free-air temperature range,
$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>LOAD CAPACITANCE</th>
<th>$T_A = 25^\circ\text{C}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{max}$</td>
<td>$OE$</td>
<td>$Q_{A\rightarrow OH}$</td>
<td>$CL = 15 \text{pF}$</td>
<td>135</td>
</tr>
<tr>
<td>$TP_{HL}$</td>
<td>RCLK</td>
<td>$Q_{A\rightarrow OH}$</td>
<td>$CL = 15 \text{pF}$</td>
<td>5.4</td>
</tr>
<tr>
<td>$TP_{LH}$</td>
<td>SRCLK</td>
<td>$O_{Y\rightarrow}$</td>
<td>$CL = 15 \text{pF}$</td>
<td>6.2</td>
</tr>
<tr>
<td>$TP_{HL}$</td>
<td>SRCLR</td>
<td>$Q_{A\rightarrow OH}$</td>
<td>$CL = 15 \text{pF}$</td>
<td>5.9</td>
</tr>
<tr>
<td>$TP_{ZT}$</td>
<td>$OE$</td>
<td>$Q_{A\rightarrow OH}$</td>
<td>$CL = 15 \text{pF}$</td>
<td>4.8</td>
</tr>
<tr>
<td>$TP_{ZL}$</td>
<td>$OE$</td>
<td>$Q_{A\rightarrow OH}$</td>
<td>$CL = 15 \text{pF}$</td>
<td>4.8</td>
</tr>
<tr>
<td>$PL_H$</td>
<td>RCLK</td>
<td>$Q_{A\rightarrow OH}$</td>
<td>$CL = 50 \text{pF}$</td>
<td>6.9</td>
</tr>
<tr>
<td>$PL_L$</td>
<td>SRCLK</td>
<td>$O_{Y\rightarrow}$</td>
<td>$CL = 50 \text{pF}$</td>
<td>7.7</td>
</tr>
<tr>
<td>$PL_H$</td>
<td>SRCLR</td>
<td>$O_{Y\rightarrow}$</td>
<td>$CL = 50 \text{pF}$</td>
<td>7.4</td>
</tr>
<tr>
<td>$PL_Z$</td>
<td>$OE$</td>
<td>$Q_{A\rightarrow OH}$</td>
<td>$CL = 50 \text{pF}$</td>
<td>8.3</td>
</tr>
<tr>
<td>$PL_Z$</td>
<td>$OE$</td>
<td>$Q_{A\rightarrow OH}$</td>
<td>$CL = 50 \text{pF}$</td>
<td>7.6</td>
</tr>
</tbody>
</table>

* On products compliant to MIL-PRF-36535, this parameter is ensured but not production tested.

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3-465
SN54AHCT595, SN74AHCT595
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS
SCL3274A - MAY 1997 - REVISED JUNE 1997

switching characteristics over recommended operating free-air temperature range, 
\( V_{CC} = 5 \, \text{V} \pm 0.5 \, \text{V} \) (unless otherwise noted) (see Figure 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>LOAD CAPACITANCE</th>
<th>( T_A = 25 , ^\circ \text{C} )</th>
<th>( V_{CC} = 5 , \text{V} \pm 0.5 , \text{V} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{\text{PLH}} )</td>
<td>RCLK</td>
<td>( Q_A-Q_H )</td>
<td>( C_L = 15 , \text{pF} )</td>
<td>135</td>
<td>155</td>
</tr>
<tr>
<td>( t_{\text{PHL}} )</td>
<td>RCLK</td>
<td>( Q_H )</td>
<td>( C_L = 50 , \text{pF} )</td>
<td>95</td>
<td>115</td>
</tr>
<tr>
<td>( t_{\text{PHZ}} )</td>
<td>OE</td>
<td>( Q_A-Q_H )</td>
<td>( C_L = 15 , \text{pF} )</td>
<td>4.8</td>
<td>6.6</td>
</tr>
<tr>
<td>( t_{\text{PHL}} )</td>
<td>OE</td>
<td>( Q_H )</td>
<td>( C_L = 50 , \text{pF} )</td>
<td>4.8</td>
<td>6.6</td>
</tr>
<tr>
<td>( t_{\text{PZH}} )</td>
<td>OE</td>
<td>( Q_A-Q_H )</td>
<td>( C_L = 15 , \text{pF} )</td>
<td>4.8</td>
<td>6.6</td>
</tr>
<tr>
<td>( t_{\text{PZH}} )</td>
<td>OE</td>
<td>( Q_H )</td>
<td>( C_L = 50 , \text{pF} )</td>
<td>4.8</td>
<td>6.6</td>
</tr>
</tbody>
</table>

output-skew characteristics, \( C_L = 50 \, \text{pF} \) (see Note 4)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>( V_{CC} )</th>
<th>( T_A = 25 , ^\circ \text{C} )</th>
<th>( V_{CE} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{\text{skew}} )</td>
<td>Output skew</td>
<td>5 V \pm 0.5 V</td>
<td>1 , 1 ns</td>
</tr>
</tbody>
</table>

noise characteristics, \( V_{CC} = 5 \, \text{V}, \, C_L = 50 \, \text{pF}, \, T_A = 25^\circ \text{C} \) (see Note 5)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>( V_{CC} )</th>
<th>( T_A = 25 , ^\circ \text{C} )</th>
<th>( V_{CE} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OL} )</td>
<td>Quiet output, maximum dynamic ( V_{OL} )</td>
<td>0.8 V</td>
<td>-0.8 V</td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Quiet output, minimum dynamic ( V_{OL} )</td>
<td>-0.8 V</td>
<td>0.8 V</td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>Quiet output, minimum dynamic ( V_{OH} )</td>
<td>2 V</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>High-level dynamic input voltage</td>
<td>0.8 V</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>Low-level dynamic input voltage</td>
<td>0.8 V</td>
<td>V</td>
</tr>
</tbody>
</table>

operating characteristics, \( V_{CC} = 5 \, \text{V}, \, T_A = 25^\circ \text{C} \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>TYP</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{\text{OFF}} )</td>
<td>Forward blocking current ( I_{\text{OFF}} )</td>
<td>No load</td>
<td>1 , 1 MHz</td>
</tr>
</tbody>
</table>
PARAMETER MEASUREMENT INFORMATION

<table>
<thead>
<tr>
<th>TEST</th>
<th>S1</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPLH/tPHL</td>
<td>Open</td>
</tr>
<tr>
<td>tPLH/tPHL</td>
<td>VCC</td>
</tr>
<tr>
<td>tPHZ/tPZH</td>
<td>GND</td>
</tr>
</tbody>
</table>

Timing Input

- 1.5 V
- 0 V

Data Input

- 1.5 V
- 1.5 V
- 3 V
- 0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

Output Control

(1) Low-level enabling

Output Waveform 1

- S1 at VCC

Waveform 2

- S1 at GND

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_o = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms
BIODATA

NAMA : RONALDUS FANCY D.
NRP : 5103096056
TEMPAT / TGL LAHIR : RUTENG-FLORES,
                        21 NOVEMBER 1976
ALAMAT : JL. RUNGKUT ASRI BARAT 1/54
          SURABAYA
NO. TELEPON : 8706629

RIWAYAT PENDIDIKAN :

• TAHUN 1990 LULUS SDK KUMBA I RUTENG
• TAHUN 1993 LULUS SMPK IMMACULATA RUTENG
• TAHUN 1996 LULUS SMA NEGERI 17 SURABAYA
• TAHUN 2001 LULUS SARJANA FAKULTAS TEKNIK JURUSAN TEKNIK
  ELEKTRO UNIVERSITAS KATOLIK WIDYA MANDALA