LAMPIRAN
DIAGRAM ALUR SOFTWARE
METRONOME DAN STEM FLUTE DIGITAL

Start

Inisialisasi

Tampilan Awal

Scan Keypad

Tombol 'MEN'

ya

CHOOSE MENUS

tidak

Tombol 'CAN'

tidak
Tampilan I
Press <- or ->

Menu = Menu + 1

Tampilan menu ke X

Scan Keypad

Tombol <- (bawah)

Tidak

Tombol -> (atas)

Tombol 'CAN'

Tombol 'MEN'

Tombol 'ENT'

Start

A

B
Menu 1

Tampilkan Menu 1 Stem Flute

Scan Keypad

Tombol "#" yang telah ditekan

Tombol '1' yang telah ditekan?

Tombol '2' yang telah ditekan?

Tampilkan Do = C#

Bunyi Nada C#

Matikan tanda #

Tampilkan Do = C

Bunyi Nada C

Matikan tanda #

Tampilkan Do = D#

Bunyi Nada D#

Matikan tanda #

Tampilkan Do = D

Bunyi Nada D

D
Menu 2

Tampilan Menu 2 Metronome

Scan Keypad

Tombol <-
(bawah)
ya
Tampilkan Tempo +1
tidak
Tombol ->
(atas)
ya
Tempo = Tempo -1
tidak

Start

Tombol 'CAN'
tidak

Choose menus

Tombol 'MEN'
tidak

Tombol 'ENT'

Prosedur Tempo

ya

 tidak

 tidak
Menu 3

Tampilan Menu 3
Flute & Metronome

Scan Keypad

Tombol <- (bawah)

Tombol -> (atas)

Tombol 'CAN'

Tombol 'MEN'

Tombol 'ENT'

E

If F

Tempo = Tempo +1

Tempo = Tempo -1

Tampilkan Tempo X dan Nada Do =

ya

Start

Choose menus

ya

Prosedur Tempo
Prosedur Tempo

Inisialisasi Timer 0 Nada & Tempo

Scan Keypad

RET (Akhir prosedur)

Stop Timer0

Yes

Tombol 0

Tidak

Interrupt Timer 0

Bunyi Nada=

RETI (akhir interrupt timer0)
porta equ 2000h
portb equ 2001h
portc equ 2002h
portcw equ 2003h
nada equ 08h
simpan# equ 09h
tombol equ 0ah
simpanmenu equ 0bh
simpan tempo equ 0ch
simpan nada equ 0dh
bea equ 0eh

LCD equ 6000h ; LCD Address
LCD0 equ LCD+0 ; LCD CONTROL OPERATION
LCD1 equ LCD+1 ; LCD DATA OPERATION

;------------------------------------------
; INISIALISASI LCD
;------------------------------------------
DISPCLR equ 00000001B ; DISPLAY CLEAR
FUNCS1 equ 00111000B ; INTERFACE DATA LENGTH : 8 BITS
ENTMOD equ 00000110B ; INCREMENT, NO DISPLAY SHIFT
DISPB1 equ 00001100B ; DISPLAY ON, CURSOR OFF, BLINK OFF
CURSOR equ 00001110B ; DISPLAY ON, CURSOR ON, BLINK OFF
BLINK equ 00001101B ; DISPLAY ON, CURSOR OFF, BLINK ON

ORG 00h
JMP setawai
ORG 36h

; Procedure LCD Display
;--------------------
POSISI2.1: MOV A,R7 ; KOLOM
POSISI2: ADD A,#11000000B ; POSISI DI BARIS 2
SMP POSISI1.SUB
POSISI1.1: MOV A,R6 ; KOLOM
POSISI1: ADD A,#10000000B ; POSISI DI BARIS 1
POSISI1.SUB: DEC A ; AWALAN POSISI KOLOM DIMULAI DARI 0
ACALL CONTROL0UT ; KIRIM SEBAGAI OPERASI KONTROL
RET

PRINTSTRING2: ACALL POSISI2.1 ; CETAK STRING DI BARIS 2 KOLOM 1
SMP PRINTSTRING
PRINTSTRING1: ACALL POSISI1.1 ; CETAK STRING
PRINTSTRING: SMP OUTSTRING
PRINTSTRING1OOP: ACALL DATAOUT ; KIRIM SEBAGAI OPERASI DATA
INC DPTR ; AMBIL DATA DULU
OUTSTRING: CLR A
MOVC A,@A+DPTR
JNZ PRINTSTRING1OOP ; AFAKAN MASIH ADA DATA BERIKUTNYA

;-------------------------------
; CETAK STRING DI BARIS 2 KOLOM 1
; CETAK STRING
; CETAK STRING
; CETAK STRING
; AMBIL DATA DULU
; KIRIM SEBAGAI OPERASI DATA
; POSISI DATA BERIKUTNYA
; POINTER=0
; AMBIL DATA BERDASARKAN DPTR
; AFAKAN MASIH ADA DATA BERIKUTNYA
CONTROLOUT: PUSH DPH
PUSH DPL
MOV DPTR, #LCD0
SJMP LCD.OUT

DATAOUT: PUSH DPH
PUSH DPL
MOV DPTR, #LCD1

LCD.OUT: MOVX @DPTR, A

DELAY.LCD: MOV A, #250
DJNZ A, $;
POP DPL
POP DPH
RET

DELAY.INIT.LCD:

MOV R1, #020h
DJNZ R2, S
DJNZ R1, DLY.LCD.LP
RET

DLY.LCD.LP:
MOV R2, #0
DJNZ R2, S
DJNZ R1, DLY.LCD.LP
RET

INIT.LCD: MOV A, #DISPCLR
ACALL CONTROLOUT
ACALL DELAY.INIT.LCD
MOV A, #FUNCSET
ACALL CONTROLOUT
MOV A, #DISPON
ACALL CONTROLOUT
MOV A, #ENTRMOD
ACALL CONTROLOUT
RET

BUNYI:
masuki: SETB P1.0
ACALL DELAYnada
CLR P1.0
ACALL DELAYnada
RET

Delay3: MOV R2, #0aH
MOV R3, #0aH
DJNZ R3, $
DJNZ R2, Del2
RET

Del2: MOV R2, #0aH
MOV R3, #0aH
DJNZ R3, $
DJNZ R2, Del2
RET

DELAYnada MOV R5, nada

LAGI
MOV TMOD, #21h
MOV TH0, #0FFH
MOV TL0, #0FFH
SETB TR0

ULANG
NOP
JBC TF0, HITUNG
SJMP ULANG
HI TUNG

djnz R5, LAG1
RET

DELAY:
MOV r1, #10

DEL:
MOV r2, #30
DJNZ r2, $
DJNZ r1, DEL
RET

okedeh:
acall scankeypad
mov r0, tombol
cjne r0, #0', lanjutx
ajmp selasai

lanjutx
mov r3, #80
acall oke
ACALL delaybeat
ajmp okedeh

selasai
RET

delaybeat
MOV R4, beat
mov r2, #20
lagilagi:
MOV TMOL, #11h
MOV TH1, #00h
MOV TL1, #00h
SETB TR1

ULANGe
NOP
JBC TF1, HITUNGe
SJMP ULANGe

HITUNGe
djnz r2, lagilagi
djnz R4,LAGIx
RET

siltek: DB ' METRONOME ', 0
sil: DB ' STEM FLUTE ', 0
m12: DB ' Menu 1 ', 0
m22: DB ' Menu 2 ', 0
m32: DB ' Menu 3 ', 0
m42: DB ' Menu 4 ', 0
m1: DB ' Stem Flute ', 0
m2: DB ' Metronome ', 0
m3: DB ' Flute-Metronome ', 0
m4: DB ' Song Example ', 0
menu: DB ' Choose Menus ', 0
press$: DB ' Press <- or -> ', 0
silcob1: DB ' Press 1,2,3,... ', 0
silcob2: DB ' CAN for cancel ', 0
silcob3: DB '... u/ Nada ', 0
silcob4: DB ' <- or -> u/ Tempo', 0
doc: DB ' DO = C ', 0
dod: db ' DO = D', 0
doe: db ' DO = E', 0
dof: db ' DO = F', 0
dog: db ' DO = G', 0
doa: db ' DO = A', 0
dob: db ' DO = B', 0
doct: db ' DO = C1', 0
dock: db ' DO = C#', 0
dodk: db ' DO = D#', 0
dofk: db ' DO = F#', 0
dogk: db ' DO = G#', 0
doak: db ' DO = A#', 0
ekosong: db ' 0
tem1 db ' LARGO', 0
tem2 db ' LENTO', 0
tem3 db ' ADAGIO', 0
tem4 db ' LARGHETTO', 0
tem5 db ' ADAGIETTO', 0
tem6 db ' ANDANTE', 0
tem7 db ' ANDANTINO', 0
tem8 db ' MAESTOSO', 0
kaspo3 db 'langan ditulisi', 0
tem10 db ' ALLEGRETO', 0
tem11 db ' ANIMATO', 0
tem12 db ' ALLEGRO', 0
tem13 db ' ASSAI', 0
tem14 db ' VIVACE', 0
tem15 db ' PRESTO', 0
tem16 db ' PRESTISSIMO', 0
tem9 db ' MODERATO', 0
tem1a db ' ( 44 - 46 )', 0
tem2a db ' ( 52 - 54 )', 0
tem3a db ' ( 56 - 58 )', 0
tem4a db ' ( 60 - 63 )', 0
tem5a db ' ( 66 - 69 )', 0
tem6a db ' ( 72 - 76 )', 0
tem7a db ' ( 80 - 84 )', 0
tem9a db ' ( 96 - 100 )', 0
tem10a db ' ( 108 - 112 )', 0
tem11a db ' ( 120 - 126 )', 0
tem12a db ' ( 132 - 138 )', 0
tem13a db ' ( 144 - 152 )', 0
tem14a db ' ( 160 - 168 )', 0
tem15a db ' ( 184 - 192 )', 0
tem16a db ' ( 208 )', 0
judo1 db 'JOYFUL, JOYFUL...', 0
judo12 db ' -beethoven-', 0

;------------------------------------------
INITIALISASI PPI 8255
;------------------------------------------
init.ppi MOV DPTR,#PORTcw
MOV A,#081h
MOVX @DPTR,A
ret

; scan keypad
;-----------------------------
scankeypad:
mov tombol, #20h
MOV A, #01110000B
MOV DPTR, #portc
MOVX @DPTR, A
CLR A

mov dptr, #portc
MOVX A, @dptr
mov r1, a
anl a, #00001111b
cjne a, #0eh, cek_0

mov tombol, '#0'
ajmp ketemu

cek_0
mov a, r1
anl a, #00001111b
cjne a, #0dh, cek_ENT

mov tombol, '#E'
ajmp ketemu

cek_ENT
mov a, r1
anl a, #00001111b
cjne a, #07h, kosong2

mov tombol, '#b'
ajmp ketemu

kosong2:
MOV A, #10110000B
MOV DPTR, #portc
MOVX @DPTR, A
CLR A

mov dptr, #portc
MOVX A, @dptr
mov r1, a
anl a, #00001111b
cjne a, #0eh, cek_8

mov tombol, '#7'
ajmp ketemu

cek_8:
mov a, r1
anl a, #00001111b
cjne a, #0dh, cek_9

mov tombol, '#8'
cek_9:
    mov a, rl
    anl a, #00001111b
    cjne a, #0bh, cek_A
    mov tombol, #9'
    ajmp ketemu

cek_A:
    mov a, rl
    anl a, #00001111b
    cjne a, #07h, kosong3
    mov tombol, #A'
    ajmp ketemu

kosong3:
    MOV A, #11010000B  ; scan baris 3
    MOV DPT, #portc
    MOVX @DPT, A
    CLR A
    mov dptr, #portc
    MOVX A, @DPT
    mov r1, a
    anl a, #00001111b
    cjne a, #0eh, cek_5
    mov tombol, #4'
    ajmp ketemu

cek_5:
    mov a, rl
    anl a, #00001111b
    cjne a, #0dh, cek_6
    mov tombol, #5'
    ajmp ketemu

cek_6:
    mov a, rl
    anl a, #00001111b
    cjne a, #0dh, cek_C
    mov tombol, #6'
    ajmp ketemu

cek_C:
    mov a, rl
    anl a, #00001111b
    cjne a, #97h, kosong4
    mov tombol, #C'
    ajmp ketemu

kosong4:
    MOV A, #11100000B  ; scan baris 4
    MOV DPT, #portc
    MOVX @DPT, A
    CLR A
    mov dptr, #portc
    MOVX A, @DPT
cek_2:
mov a, rl
anl a, #00001111b
cjne a, #00h, cek_2
mov tombol, #'1'
ajmp ketemu

cek_3:
mov a, rl
anl a, #00001111b
cjne a, #01h, cek_3
mov tombol, #'2'
ajmp ketemu

cek_MENU
mov 45h, #03h ;standa belum dipencet
mov a, rl
anl a, #00001111b
cjne a, #05h, cek_MENU
mov tombol, #'3'
ajmp ketemu

ketemu:
ret

cek:
ulul1:
acall bunyi
djnz r3, ulul1
ret

tam_menu_1:
mov r7, #05h
ulul3a:
mov r6, #0ffh
ulul2a:
acall delay3
djnz r6, ulul2a
djnz r7, ulul3a

mov a, simpanmenu
cjne a, #01h, lancek0
acall tam_menu1
ajmp lancek3
lancek0

cjne a, #02h, lancek1
acall tam_menu2
ajmp lancek3
lancek1

cjne a, #03h, lancek2
acall tam_menu3
ajmp lancek3
lancek2

cjne a, #04h, lancek3
acall tam_menu4
lancek3
ret

tam_menu1:
mov r6, #1
mov r7, #1
mov dptr, #ml2
acall printstring1
mov dptr,#m1
acall printstring2
ret

tam_menu2:  mov r6,#1
mov r7,#1
mov dptr,#m41
acall printstring1
mov dptr,#m2
acall printstring7
ret

tam_menu3:  mov r6,#1
mov r7,#1
mov dptr,#m32
acall printstring1
mov dptr,#m3
acall printstring2
ret

tam_menu4:  mov r6,#1
mov r7,#1
mov dptr,#m42
acall printstring1
mov dptr,#m4
acall printstring2
ret

tam_menu5:  mov r6,#1
mov r7,#1
mov dptr,#menu
acall printstring1
mov dptr,#pressb
acall printstring2
ret

choose_menu:  acall tam_menu5
ulang2:  acall scankeypad
mov r9,tombol
cjne r0,'#b',cmenul
inc simpanmenu
mov r0,simpanmenu
cjne r0,#05h,belum4
mov simpanmenu,#00h

belum4:  acall tam_menu_ke
ajmp ulang2

cmenul
mov r0,tombol
cjne r0,'#A',cmenu2
dec simpanmenu
mov r1,simpanmenu
cjne r1,#0ffh,trussl:
mov simpanmenu,#09h

trussl:  mov r0,simpanmenu
cjne r0,#00h,belum5
mov simpanmenu,#04h
belum0: 
acall tam_menu_ke
ajmp ulang2

cmenu2 
mov r0, tombol
cjne r0, #'C', cmenu3
ljmp setawal

cmenu3 
mov r0, tombol
cjne r0, #'E', cmenu4

; 
mov r0, simpanmenu
mov a, simpanmenu
cjne a, #01h, lancek0x
acall menu1
ajmp lancek3
lancek0x 
cjne a, #02h, lancek1x
icall menu2
ajmp lancek3
lancek1x 
cjne a, #03h, lancek2x
icall menu3
ajmp lancek3
lancek2x 
cjne a, #04h, lancek3x
icall menu4
lancek3x 
ljmp setawal

cmenu4 
mov r0, tombol
cjne r0, #'M', cmenu5
ajmp choose_menu

cmenu5 
ajmp ulang2
ret

tulis_kosong:
mov r7, #1
mov dptr, #kosong
acall printstring2
ret

menu1: 
acall tam_menu1
; tampilan menu 1
mov r6, #1
mov r7, #1
mov dptr, #silcobl
acall printstring1
mov dptr, #silcobl
acall printstring2

menu1x1: 
acall scankeypad
; reset jika cancel
mov r0, tombol
cjne r0, #'C', menu1bal0
ljmp setawal

menu1bal0: 
mov r0, tombol
; standi jika # ditekan
mov r0, #', menu1bal1
ljmp setawal

menu1bal1: 
mov r0, tombol
simpan#, #0AAh
mov r0, #1, menu1bal2
mov r1, simpan#
cjne r1, #0AAh, kres1
; cek kres dipitek
mov r6, #1
mov dptr,#doek
acall printstring1
acall tuliskosong
mov r3,#200
mov nada,#74       ;set delay untuk nada kres
mov simpan#,#00h
ajmp okedol

kres1:
mov r6,#1       ;nada biasa tanpa kres
mov dptr,#doc
acall printstring1
acall tuliskosong
mov r3,#200
mov nada,#78
okedol: acall oke
mov dptr,#portc
MOVx A,@dptr
mov r1,a
anl a,#00001111b
cjne a,#00001111b
ajmp okedol

menulbal2:
mov r0,tombol     ;idem menulbal
cjne r0,'#2',menulbal3
mov r1,simpan#
 cjne r1,#0AAh,kres2
mov r6,#1
mov dptr,#dodk
acall printstring1
acall tuliskosong
mov r3,#200
mov nada,#66
mov simpan#,#00h
ajmp okedel2

kres2 mov r6,#1
mov dptr,#dod
acall printstring1
acall tuliskosong
mov r3,#200
mov nada,#71
okedel2 acall oke
mov dptr,#portc
MOVx A,@dptr
mov r1,a
anl a,#00001111b
cjne a,#00001111b
ajmp okedel2

menulbal3: mov r0,tombol
cjne r0,'#3',menulbal4
mov r6,#1
mov dptr,#doe
acall printstring1
```
acall tuliskosong
mov r3,#200
mov nada,#62
acall oke
mov dptr,#portc
MOX A,@dptr
mov r1,a
ani a,#00001111b
cjne a,#00h,menulba5
ajmp okedox1

menulba5:
  mov r0,tombol
  cjne r0,#'4',menulba5
  mov r1,simpan#
  cjne r1,#0AHh,kres4
  mov r6,#1
  mov dptr,#do4k
  lcall printstring1
  lcall tuliskosong
  mov r3,#250
  mov nada,#44
  mov simpan#,#00h
  ljmp okedox4

kres4:
  mov r6,#1
  mov dptr,#dofk
  lcall printstring1
  lcall tuliskosong
  mov r3,#250
  mov nada,#59
  mov simpan#,#00h
  ljmp okedox4

kedox3:
  mov r6,#1
  mov dptr,#dofk
  lcall printstring1
  lcall tuliskosong
  mov r3,#250
  mov nada,#59
  mov simpan#,#00h
  ljmp okedox3

kedox3:
  mov dptr,#dofk
  lcall printstring1
  lcall tuliskosong
  mov r3,#250
  mov nada,#59
  mov simpan#,#00h
  ljmp okedox4

kedox3:
  mov dptr,#dofk
  lcall printstring1
  lcall tuliskosong
  mov r3,#250
  mov nada,#59
  mov simpan#,#00h
  ljmp okedox4

kedox3:
  mov dptr,#dofk
  lcall printstring1
  lcall tuliskosong
  mov r3,#250
  mov nada,#59
  mov simpan#,#00h
  ljmp okedox4

kedox3:
  mov dptr,#dofk
  lcall printstring1
  lcall tuliskosong
  mov r3,#250
  mov nada,#59
  mov simpan#,#00h
  ljmp okedox4
```

lcall printstringl
lcall tuliskosong
mov r3,#250
mov nada,#52
okedo4
lcall oke
mov dptr,#portc
MOVx A,@dptr
mov r1,a
ani a,#0000111b
cjne a,#0dh,menu1bal6
ajmp okedo4

menulbal6:
mov r0,tombol
cjne r0,#'6',menulbal7
mov r1,simpan#
cjne r1,#0AAh,kres5
mov r6,#1
mov dptr,#doak
lcall printstringl
lcall tuliskosong
mov r3,#250
mov nada,#44
mov simpan#,#00h
ajmp okedo5

kres5:
mov r6,#1
mov dptr,#doa
lcall printstringl
lcall tuliskosong
mov r3,#250
mov nada,#46
okedo5
lcall oke
mov dptr,#portc
MOVx A,@dptr
mov r1,a
ani a,#0000111b
cjne a,#0bh,menu1bal7
ajmp okedo5

menulbal7:
mov r0,tombol
cjne r0,#'7',menulbal8
mov r6,#1
mov dptr,#dob
lcall printstringl
lcall tuliskosong
mov r3,#230
mov nada,#41
okedo2
lcall oke
mov dptr,#portc
MOVx A,@dptr
mov r1,a
ani a,#0000111b
cjne a,#0eh,menu1bal8
menubal8:
  mov r0, tombol
  cjne r0, '#9', menubal9
  mov r6, #1
  mov dptr, #doct
  lcall printstring1
  lcall tuliskosong
  mov r3, #230
  mov nada, #39
okedo3
  lcall oke
  mov dptr, #portc
  MOVx A, @dptr
  mov r1, a
  anl a, #00000111b
  cjne a, #0dh, menubal9
  ajmp okedo3

menubal9:  ljmp menux1
           ret

ta_menu_2_donk
  mov r7, #05h
ulul3axx:  mov r6, #0ffh
ulul2axx:  lcall delay3
            djnz r6, ulul2axx
            djnz r7, ulul3axx

            mov a, simpantempo
            cjne a, #01h, lancek0xx
            mov r6, #1
            mov dptr, #tem1
            lcall printstring1
            mov r7, #1
            mov dptr, #tem1a
            lcall printstring2
            mov beat, #223
            ljmp lancek16x
lancek0xx
            cjne a, #02h, lancek1xx
            mov r6, #1
            mov dptr, #tem2
            lcall printstring1
            mov r7, #1
            mov dptr, #tem2a
            lcall printstring2
            mov beat, #188
            ljmp lancek16x
lancek1xx
            cjne a, #03h, lancek2xx
            mov r6, #1
            mov dptr, #tem3
            lcall printstring1
            mov r7, #1
            mov dptr, #tem3a
            lcall printstring2
            mov beat, #169
lancek2xx
ljmp lancek16x
cjne a, #04h, lancek3xx
mov r6, #1
mov dptr, #tem4
lcall printstring1
mov r7, #1
mov dptr, #tem4a
lcall printstring2
mov r#16, #1
mov dptr, #tem5
lcall printstring1
mov r7, #1
mov dptr, #tem5a
lcall printstring2
mov beat, #153
ljmp lancek16x
lancek3xx
cjne a, #05h, lancek4x
mov r6, #1
mov dptr, #tem5
lcall printstring1
mov r7, #1
mov dptr, #tem5a
lcall printstring2
mov beat, #138
ljmp lancek16x
lancek4x
cjne a, #06h, lancek5x
mov r6, #1
mov dptr, #tem6
lcall printstring1
mov r7, #1
mov dptr, #tem6a
lcall printstring2
mov beat, #127
ljmp lancek16x
lancek5x
cjne a, #07h, lancek6x
mov r6, #1
mov dptr, #tem7
lcall printstring1
mov r7, #1
mov dptr, #tem7a
lcall printstring2
mov beat, #110
ljmp lancek16x
lancek6x
cjne a, #08h, lancek7x
mov r6, #1
mov dptr, #tem8
lcall printstring1
mov r7, #1
mov dptr, #tem8a
lcall printstring2
mov beat, #99
ljmp lancek16x
lancek7x
cjne a, #09h, lancek8x
mov r6, #1
mov dptr, #tem9
lcall printstring1
mov r7, #1
mov dptr, #tem9a
lcall printstring2
mov beat, #87
ljmp lancek16x
lancek8x
cjne a, #0ah, lancek9x
mov r6, #1
mov dptr, #tema
lcall printstring1
mov r7, #1
mov dptr, #tema a
lcall printstring2
mov beat, #77
ljmp lancek16x
lancek9x
cjne a, #0bh, lancek1x
mov r6, #1
mov dptr, #temb
lcall printstring1
mov r7, #1
mov dptr, #temb a
lcall printstring2
mov beat, #66
ljmp lancek16x
lancek10x
cjne a, #0ch, lancek11x
mov r6, #1
mov dptr, #temc
lcall printstring1
mov r7, #1
mov dptr, #temc a
lcall printstring2
mov beat, #55
ljmp lancek16x
lancek11x
cjne a, #0dh, lancek12x
mov r6, #1
mov dptr, #temd
lcall printstring1
mov r7, #1
mov dptr, #temd a
lcall printstring2
mov beat, #44
ljmp lancek16x
lancek12x
cjne a, #0eh, lancek13x
mov r6, #1
mov dptr, #teme
lcall printstring1
mov r7, #1
mov dptr, #teme a
lcall printstring2
mov beat, #33
ljmp lancek16x
lancek13x
cjne a, #0fh, lancek14x
mov r6, #1
mov dptr, #temf
lcall printstring1
mov r7, #1
mov dptr, #temf a
lcall printstring2
mov beat, #22
ljmp lancek16x
lancek14x
cjne a, #10h, lancek15x
mov r6, #1
mov dptr, #temf
lcall printstring1
mov r7, #1
mov dptr, #temf a
lcall printstring2
mov beat, #11
ljmp lancek16x
lancek15x
cjne a, #11h, lancek16x
mov r6, #1
mov dptr, #temt
lcall printstring1
mov r7, #1
mov dptr, #temt a
lcall printstring2
mov beat, #00
mov    dptr,#tem10
1call printstring1
mov    r7,#1
mov    dptr,#tem10a
1call printstring2
mov    beat,#75
ajmp lancek16x
lancek9x

cjne a,#0bh,lancek10x
mov    r6,#1
mov    dptr,#tem11
1call printstring1
mov    r7,#1
mov    dptr,#tem11a
1call printstring2
mov    beat,#65
ajmp lancek16x
lancek10x

cjne a,#0ch,lancek11x
mov    r6,#1
mov    dptr,#tem12
1call printstring1
mov    r7,#1
mov    dptr,#tem12a
1call printstring2
mov    beat,#55
ajmp lancek16x
lancek11x

cjne a,#0dh,lancek12x
mov    r6,#1
mov    dptr,#tem13
1call printstring1
mov    r7,#1
mov    dptr,#tem13a
1call printstring2
mov    beat,#49
ajmp lancek16x
lancek12x

cjne a,#0eh,lancek13x
mov    r6,#1
mov    dptr,#tem14
1call printstring1
mov    r7,#1
mov    dptr,#tem14a
1call printstring2
mov    beat,#44
ajmp lancek16x
lancek13x

cjne a,#0fh,lancek14x
mov    r6,#1
mov    dptr,#tem15
1call printstring1
mov    r7,#1
mov    dptr,#tem15a
1call printstring2
mov    beat,#32
ajmp lancek16x
lancek14x

cjne a,#10h,lancek16x
mov    r6,#1
mov    dptr,#tem16
1call printstring1
mov    r7,#1
mov dptr, #tem16a
lcall printstring2
mov beat, #24
lancek16x
ret
mulai_beat
mov nada, #78
lcall okedeh
ret
menu2
lcall iam_menu2
lcall ta_menu_2_donk
mov r7, #05h
ulul3axxx:
mov r6, #0ffh
ulul2axxx:
licall delay3
djnz r6, ulul2axxx
djnz r7, ulul3axxx
ulang2x:
lcall scankeypad
mov r0, tombol
cjne r0, '#b', cmenu1x
inc simpantempo
mov r6, simpantempo
cjne r6, #17, belum14
mov simpantempo, #00h
belum14:
lcall ta_menu_2_donk
ajmp ulang2x
cmenu1x
mov r0, tombol
cjne r0, '#a', cmenu2x
dec simpantempo
mov r0, simpantempo
cjne r0, #0ffh, truss1x
mov simpantempo, #00h
truss1x:
mov r0, simpantempo
cjne r0, #0ffh, truss1x
mov simpantempo, #00h
truss6x:
mov r0, simpantempo
cjne r0, #0ffh, belum00
mov simpantempo, #16
belum00:
lcall ta_menu_2_donk
ajmp ulang2x
cmenu2x
mov r0, tombol
cjne r0, '#c', cmenu3x
ajmp setawal
cmenu3x
mov r0, tombol
cjne r0, '#e', cmenu4x
lcall mulai_beat
ajmp ulang2x
cmenu4x
mov r0, tombol
cjne r0, '#m', cmenu5x
ljmp choosemenu
cmenu5x
ajmp ulang2x
ret

delayku mov r7,#05h
ulul3axxx: mov r6,#0ffh
ulul2axxx: lcall delay3
djnz r6,ulul2axxx
djnz r7,ulul3axxx
ret

menu3
lcall tam_menu3
lcall ta_menu_2_donk
mov r7,#1
mov dptr,#doc
lcall printstring2
acall delayku

ulang3x:
lcall scankeypad
mov r0,tombol
cjne r0,'#b',cmenu1xx
inc simpantempo
mov r0,simpantempo
cjne r0,#17,belum14x
mov simpantempo,#00h

belum14x:
lcall ta_menu_2_donk
ajmp ulang3x

cmenu1xx
mov r0,tombol
cjne r0,'#A',cmenu2xx
dec simpantempo
mov r1,simpantempo
cjne r1,#0ffh,truss11xx
mov simpantempo,#00h

truss11xx:
mov r0,simpantempo
cjne r0,#00h,belum000
mov simpantempo,#16

belum000:
lcall ta_menu_2_donk
ajmp ulang3x

cmenu2xx
mov r0,tombol
cjne r0,'#C',cmenu3xx
ajmp setawal

cmenu3xx
mov r0,tombol
cjne r0,'#E',cmenu4xx

mov r7,#10
bunyi5detik lcall oke
djnz r7,bunyi5detik

lcall okedeh
ajmp ulang3x

cmenu4xx
mov r0,tombol
cjne r0,'#M',cmenu5xx
ljmp choosemenu

cmenu5xx
mov r0,tombol ;standai jika # ditekan
cjne r0,’#’,menulbal1x
mov simpan#,#0AAh
mov r7,#1
lcall posisi2.1
mov a,’#’
lcall dataout
ljmp ulang3x

menulbal1x:
mov r0,tombol
cjne r0,’1’,menulbal2x
mov rl,simpan#
cjne rl,#0AAh,kreslx ;cek kres dipitek
mov r7,#1
mov dptr,#dock
lcall printstring2
mov simpan#,#00h
mov nada,#74
acall delayku
ajmp ulang3x

kreslx:
mov r7,#1 ;nada biasa tanpa kres
mov dptr,#dock
lcall printstring2
mov nada,#78
acall delayku
ajmp ulang3x

menulbal2x:
mov r0,tombol ;idem menulbal
cjne r0,’2’,menulbal3x
mov rl,simpan#
cjne rl,#0AAh,kres2x
mov r7,#1
mov dptr,#dock
lcall printstring2
mov simpan#,#00h
mov nada,#66
acall delayku
ajmp ulang3x

kres2x
mov r7,#1
mov dptr,#dock
lcall printstring2
mov nada,#71
acall delayku
ajmp ulang3x

menulbal3x: mov r0,tombol
cjne r0,’3’,menulbal4x
mov r7,#1
mov dptr,#dod
lcall printstring2
mov nada,#62
acall delayku
ajmp ulang3x

menulbal4x:
mov r0, tombol
cjne r0, #4', menu1bal5x
mov r1, simpan#
cjne r1, #0AAh, kres3x
mov r7, #1
mov dptr, #dofx
lcall printstring2
mov simpan#, #00h
mov nada, #55
acall delayku
ajmp ulang3x

kres3x:

mov r7, #1
mov dptr, #dof
lcall printstring2
mov nada, #59
acall delayku
ajmp ulang3x

menu1bal5x:

mov r0, tombol
cjne r0, #5', menu1bal6x
mov r1, simpan#
cjne r1, #0AAh, kres4x
mov r7, #1
mov dptr, #dogx
lcall printstring2
mov simpan#, #00h
mov nada, #49
acall delayku
ajmp ulang3x

kres4x:

mov r7, #1
mov dptr, #dog
lcall printstring2
mov nada, #52
acall delayku
ajmp ulang3x

+ menu1bal6x:

mov r0, tombol
cjne r0, #6', menu1bal7x
mov r1, simpan#
cjne r1, #0AAh, kres5x
mov r7, #1
mov dptr, #doax
lcall printstring2
mov simpan#, #00h
mov nada, #44
acall delayku
ajmp ulang3x

kres5x:

mov r7, #1
mov dptr, #doa
lcall printstring2
mov nada, #46
acall delayku
Inenulbal7x:
mov r0,tombol
cjne r0,'#7',menulbal8x
mov r7,#1
mov dptr,#dob
lcall printstring2
mov nada,#41
acall delayku
ajmp ulang3x

menulbal8x:
mov r0,tombol
cjne r0,'#8',menulbal9x
mov r7,#1
mov dptr,#doct
lcall printstring2
mov nada,#39
acall delayku

menulbal9x: ajmp ulang3x
ret

--------------------------------------
menu4
;JOYFUL, JOYFUL WE ADORE THEE -beethoven-
;MM = 116
--------------------------------------

mov r6,#1
mov r7,#1
mov dptr,#judul1
lcall printstring1
mov dptr,#judul2
lcall printstring2
mov beat,#75
mov r3,#80
mov nada,#41 ;mi
lcall oke
lcall delaybeat
mov r3,#80
mov nada,#41 ;mi
lcall oke
lcall delaybeat
mov r3,#80
mov nada,#39 ;fa
lcall oke
lcall delaybeat
mov r3,#80
mov nada,#35 ;sol
lcall oke
lcall delaybeat
mov r3,#80
mov nada,#35 ;sol
lcall oke
lcall delaybeat
mov r3,#80
mov nada,#39 ;fa
lcall oke
lcall delaybeat
mov r3, #80
mov nada, #41 ; mi
lcall oke
lcall delaybeat
mov r3, #80
mov nada, #46 ; re
lcall oke
lcall delaybeat
mov r3, #80
mov nada, #52 ; do
lcall oke
lcall delaybeat
mov r3, #80
mov nada, #52 ; do
lcall oke
lcall delaybeat
mov r3, #80
mov nada, #46 ; re
lcall oke
lcall delaybeat
mov r3, #80
mov nada, #41 ; mi
lcall oke
lcall delaybeat
mov r3, #200
mov nada, #41 ; mi 1 1/2
lcall oke
mov r3, #100
mov nada, #41 ; mi 1 1/2
lcall oke
mov beat, #37
lcall delaybeat
mov beat, #75
mov r3, #40
mov nada, #46 ; re 1/2
lcall oke
mov r3, #80
mov nada, #46 ; re
lcall oke
MOV beat, #37
lcall delaybeat
MOV beat, #75
mov r3, #80
mov nada, #46 ; re
lcall oke
lcall delaybeat
lcall delaybeat
mov r3, #80
mov nada, #41 ; mi
lcall oke
lcall delaybeat
mov r3, #80
mov nada, #41 ;mi
lcall oke
lcall delaybeat
mov r3, #80
mov nada, #39 ;fa
lcall oke
lcall delaybeat
mov r3, #80
mov nada, #35 ;sol
lcall oke
lcall delaybeat
mov r3, #80
mov nada, #35 ;sol
lcall oke
lcall delaybeat
mov r3, #80
mov nada, #39 ;fa
lcall oke
lcall delaybeat
mov r3, #80
mov nada, #41 ;mi
lcall oke
lcall delaybeat
mov r3, #80
mov nada, #46 ;re
lcall oke
lcall delaybeat
mov r3, #80
mov nada, #52 ;do
lcall oke
lcall delaybeat
mov r3, #80
mov nada, #52 ;do
lcall oke
lcall delaybeat
mov r3, #80
mov nada, #46 ;re
lcall oke
lcall delaybeat
mov r3, #80
mov nada, #46 ;re
lcall oke
lcall delaybeat
mov r3, #80
mov nada, #52 ;do
lcall oke
lcall delaybeat
mov r3, #80
mov nada, #41 ;mi
lcall oke
lcall delaybeat
mov r3, #200
mov nada, #46 ;re 1 1/2
lcall oke
mov r3, #200
mov nada, #46 ;re 1 1/2
lcall oke
mov beat, #37
lcall delaybeat
mov beat, #75
mov  r3, #40
mov  nada, #52  ;do 1/2
lcall  oke
mov  r3, #80
mov  nada, #52  ;do
lcall  oke
mov  beat, #31
mov  beat, #75

mov  r3, #80
mov  nada, #52  ;do
lcall  oke
lcall  delaybeat
lcall  delaybeat

mov  r3, #80
mov  nada, #46  ;re
lcall  oke
lcall  delaybeat
mov  r3, #80
mov  nada, #46  ;re
lcall  oke
lcall  delaybeat
mov  r3, #40
mov  nada, #41  ;mi 1/2
lcall  oke

MOV  beat, #37
lcall  delaybeat
MOV  beat, #75

mov  r3, #40
mov  nada, #39  ;FA 1/2
lcall  oke

MOV  beat, #37
lcall  delaybeat
MOV  beat, #75

mov  r3, #80
mov  nada, #41  ;mi
lcall oke
lcall delaybeat
mov r3,#80
mov nada,#52 ;do
lcall oke
lcall delaybeat
mov r3,#80
mov nada,#46 ;re
lcall oke
lcall delaybeat
mov r3,#40
mov nada,#41 ;mi 1/2
lcall oke
MOV beat,#37
lcall delaybeat
MOV bcat,#75
mov r3,#30
mov nada,#39 ;FA 1/2
lcall oke
MOV beat,#37
lcall delaybeat
MOV beat,#75
mov r3,#80
mov nada,#41 ;mi
lcall oke
lcall delaybeat
mov r3,#80
mov nada,#46 ;re
lcall oke
lcall delaybeat
mov r3,#80
mov nada,#52 ;do
lcall oke
lcall delaybeat
mov r3,#80
mov nada,#46 ;re
lcall oke
lcall delaybeat
mov r3,#200
mov nada,#71 ;sol r 2x
lcall oke
mov r3,#200
mov nada,#71 ;sol r 2x
lcall oke
lcall delaybeat
mov r3,#80
mov nada,#41 ;mi
; call delaybeat
mov r3, #80
mov nada, #41 ; mi
; call oke
; call delaybeat
mov r3, #80
mov nada, #39 ; FA
; call oke
; call delaybeat
mov r3, #80
mov nada, #35 ; SOL
; call oke
; call delaybeat
mov r3, #80
mov nada, #35 ; SOL
; call oke
; call delaybeat
mov r3, #80
mov nada, #39 ; FA
; call oke
; call delaybeat
mov r3, #80
mov nada, #41 ; mi
; call oke
; call delaybeat
mov r3, #80
mov nada, #46 ; re
; call oke
; call delaybeat
mov r3, #80
mov nada, #52 ; do
; call oke
; call delaybeat
mov r3, #80
mov nada, #52 ; do
; call oke
; call delaybeat
mov r3, #80
mov nada, #46 ; re
; call oke
; call delaybeat
mov r3, #80
mov nada, #46 ; re
; call oke
; call delaybeat
mov r3, #80
mov nada, #41 ; mi
; call oke
; call delaybeat
mov r3, #200
mov nada, #46 ; re 1 1/2
; call oke
; call delaybeat
mov r3, #200
mov nada, #46 ; re 1 1/2
; call oke
mov beat, #37
; call delaybeat
mov beat, #75
mov r3,#40
mov nada,#52 :DO
lcall ok

MOV beat,#37
lcall delaybeat
MOV beat,#75

mov r3,#120
mov nada,#52 :do
lcall ok:
tel.

setawal:
mov simpanmenu,#00h ;data menu yg dipilih
mov simpan tempo,#01h ;xxxx
mov simpan nada,#02h ;xxxx
mov simpan #,#03h ;data tombol kres ditekan
mov ie,#00h
mov sp,#60h ;push-pop max 15X !!! 60-7f
lcall init.lcd
lcall init.ppi
MOV A,#0
MOV DPTR,#portc
MOVX @DPTR,A
mov r6,#1 ;kolom1
mov r7,#1 ;lem
mov dptr,#sil tek
lcall printstring1 ;baris1
mov dptr,#sil
lcall printstring2 ;baris2

ulang1
lcall scankeypad ;move tombol -> R0
cjne r0,'#M',menut1 ;bandingkan isi r0 dengan 'm'
lcall choosemenu ;jika ya panggil choosemenu
ajmp ulang1 ;jika tidak lompat ulang1

menut1:
mov r0,tombol
cjne r0,'#C',ulang1
ajmp setawal
Features
- Compatible with MCS-51™ Products
- 4K Bytes of In-System Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

Description
The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash Programmable and Erasable Read Only Memory (PEROM). The device is manufactured using Atmel’s high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

Pin Configurations (continued)
The AT89C51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

Pin Description

\[\text{Vcc} \quad \text{Supply voltage.} \]

\[\text{GND} \quad \text{Ground.} \]

**Port 0**

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs. Port 0 may also be configured to be the multiplexed lower-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups. Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

**Port 1**

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (\(I_{OH}\)) because of the internal pullups. Port 1 also receives the low-order address bytes during Flash programming and verification.

**Port 2**

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (\(I_{OH}\)) because of the internal pullups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ @PTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

**Port 3**

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (\(I_{OH}\)) because of the pullups. Port 3 also serves the functions of various special features of the AT89C51 as listed below:

<table>
<thead>
<tr>
<th>Port Pin</th>
<th>Alternate Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>P3.0</td>
<td>RXD (serial input port)</td>
</tr>
<tr>
<td>P3.1</td>
<td>TXD (serial output port)</td>
</tr>
<tr>
<td>P3.2</td>
<td>INTO (external interrupt 0)</td>
</tr>
<tr>
<td>P3.3</td>
<td>INTO (external interrupt 1)</td>
</tr>
<tr>
<td>P3.4</td>
<td>TO (timer 0 external input)</td>
</tr>
<tr>
<td>P3.5</td>
<td>T1 (timer 1 external input)</td>
</tr>
<tr>
<td>P3.6</td>
<td>WR (external data memory write strobe)</td>
</tr>
<tr>
<td>P3.7</td>
<td>RD (external data memory read strobe)</td>
</tr>
</tbody>
</table>

Port 3 also receives some control signals for Flash programming and verification.

**RST**

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

**ALE/PROG**

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8Eh. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

**PSEN**

Program Store Enable is the read strobe to external program memory.
When the AT89C51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA/VP
External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset.
EA should be strapped to Vcc for internal program executions.
This pin also receives the 12-volt programming enable voltage (Vpp) during Flash programming, for parts that require 12-volt Vpp.

XTAL1
Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2
Output from the inverting oscillator amplifier.

Oscillator Characteristics
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode
In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Status of External Pins During Idle and Power Down Modes

<table>
<thead>
<tr>
<th>Mode</th>
<th>Program Memory</th>
<th>ALE</th>
<th>PSEN</th>
<th>PORT0</th>
<th>PORT1</th>
<th>PORT2</th>
<th>PORT3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Idle</td>
<td>Internal</td>
<td>1</td>
<td>1</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
<tr>
<td>Idle</td>
<td>External</td>
<td>1</td>
<td>1</td>
<td>Float</td>
<td>Data</td>
<td>Address</td>
<td>Data</td>
</tr>
<tr>
<td>Power Down</td>
<td>Internal</td>
<td>0</td>
<td>0</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
<tr>
<td>Power Down</td>
<td>External</td>
<td>0</td>
<td>0</td>
<td>Float</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
</tbody>
</table>

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections
![Oscillator Connections Diagram]

Note: C1, C2 = 30 pF ± 10 pF for Crystals = 40 pF ± 10 pF for Ceramic Resonators

Figure 2. External Clock Drive Configuration
![External Clock Drive Configuration Diagram]
Power Down Mode

In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before VCC is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Lock Bit Protection Modes

<table>
<thead>
<tr>
<th>Program Lock Bits</th>
<th>Protection Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>LB1</td>
<td>LB2</td>
</tr>
<tr>
<td>1 U</td>
<td>U</td>
</tr>
<tr>
<td>2 P</td>
<td>U</td>
</tr>
<tr>
<td>3 P</td>
<td>P</td>
</tr>
<tr>
<td>4 P</td>
<td>P</td>
</tr>
</tbody>
</table>

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

When lock bit 1 is programmed, the logic level at the EA pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latch level of EA be in agreement with the current logic level at that pin in order for the device to function properly.

Program the Flash

The AT89C51 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage VCC program enable signal. The low-voltage programming mode provides a convenient way to program the AT89C51 inside the user's system, while the high-voltage programming mode is compatible with conventional third-party Flash or EPROM programmers.

The AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

<table>
<thead>
<tr>
<th>Top-Side Mark</th>
<th>Signature</th>
<th>Vpp = 12V</th>
<th>Vpp = 5V</th>
</tr>
</thead>
<tbody>
<tr>
<td>AT89C51 xxxx</td>
<td>(030H)=1EH</td>
<td>AT89C51 xxxx</td>
<td>(030H)=1EH</td>
</tr>
<tr>
<td>yww</td>
<td>(031H)=51H</td>
<td>yww</td>
<td>(031H)=51H</td>
</tr>
<tr>
<td></td>
<td>(032H)=FFH</td>
<td></td>
<td>(032H)=05H</td>
</tr>
</tbody>
</table>

The AT89C51 code memory array is programmed byte-by-byte in either programming mode. To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.

Programming Algorithm: Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figures 3 and 4. To program the AT89C51, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise EA/VPP to 12V for the high-voltage programming mode.
5. Pulse ALE/PROG once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89C51 features Data Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/BSY output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.
Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/PROG low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

- (030H) = 1EH indicates manufactured by Atmel
- (031H) = 51H indicates 89C51
- (032H) = FFH indicates 12V programming
- (032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

<table>
<thead>
<tr>
<th>Mode</th>
<th>RST</th>
<th>PSEN</th>
<th>ALE/PROG</th>
<th>EA/V_{pp}</th>
<th>P2.6</th>
<th>P2.7</th>
<th>P3.6</th>
<th>P3.7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write Code Data</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>Read Code Data</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td></td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>Write Lock</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>Bit - 1</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>Bit - 2</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>Bit - 3</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>Chip Erase</td>
<td>H</td>
<td>L</td>
<td></td>
<td>(1)</td>
<td>H/12V</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>Read Signature Byte</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td></td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
</tbody>
</table>

Note: 1. Chip Erase requires a 10-ms PROG pulse.
AT89C51

**Figure 3. Programming the Flash**

![Diagram of AT89C51 Programming](image)

**Figure 4. Verifying the Flash**

![Diagram of AT89C51 Verification](image)

### Flash Programming and Verification Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{PP}(1)$</td>
<td>Programming Enable Voltage</td>
<td>11.5</td>
<td>12.5</td>
<td>V</td>
</tr>
<tr>
<td>$I_{PE}(1)$</td>
<td>Programming Enable Current</td>
<td>3</td>
<td>1.0</td>
<td>mA</td>
</tr>
<tr>
<td>$f_{OSC}$</td>
<td>Oscillator Frequency</td>
<td>24</td>
<td>48</td>
<td>MHz</td>
</tr>
<tr>
<td>$t_{ASL}$</td>
<td>Address Setup to PROG Low</td>
<td>48</td>
<td>96</td>
<td>CLC/CLCL</td>
</tr>
<tr>
<td>$t_{AH}$</td>
<td>Address Hold After PROG</td>
<td>48</td>
<td>96</td>
<td>CLC/CLCL</td>
</tr>
<tr>
<td>$t_{DSL}$</td>
<td>Data Setup to PROG Low</td>
<td>48</td>
<td>96</td>
<td>CLC/CLCL</td>
</tr>
<tr>
<td>$t_{DH}$</td>
<td>Data Hold After PROG</td>
<td>48</td>
<td>96</td>
<td>CLC/CLCL</td>
</tr>
<tr>
<td>$t_{P27}$</td>
<td>P2.7 (ENABLE) High to $V_{PP}$</td>
<td>48</td>
<td>96</td>
<td>CLC/CLCL</td>
</tr>
<tr>
<td>$t_{PSP}$</td>
<td>$V_{PP}$ Setup to PROG Low</td>
<td>10</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>$t_{PH}$</td>
<td>$V_{PP}$ Hold After PROG</td>
<td>10</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>$t_{PW}$</td>
<td>PROG Width</td>
<td>1</td>
<td>110</td>
<td>μs</td>
</tr>
<tr>
<td>$t_{ADV}$</td>
<td>Address to Data Valid</td>
<td>48</td>
<td>96</td>
<td>CLC/CLCL</td>
</tr>
<tr>
<td>$t_{ELV}$</td>
<td>ENABLE Low to Data Valid</td>
<td>48</td>
<td>96</td>
<td>CLC/CLCL</td>
</tr>
<tr>
<td>$t_{EFZ}$</td>
<td>Data Float After ENABLE</td>
<td>0</td>
<td></td>
<td>CLC/CLCL</td>
</tr>
<tr>
<td>$t_{PBH}$</td>
<td>PROG High to BUSY Low</td>
<td>1.0</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>$t_{BW}$</td>
<td>Byte Write Cycle Time</td>
<td>2.0</td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>

*Note: 1. Only used in 12-volt programming mode.*

---

ATMEL

4-35
Flash Programming and Verification Waveforms - High Voltage Mode ($V_{PP} = 12V$)

- **PORT 0**
  - DATA IN: $t_{AVGL}$, $t_{DVGL}$, $t_{GHDX}$, $t_{GAX}$
  - DATA OUT: $t_{AVOV}$, $t_{DVGL}$, $t_{GHDX}$, $t_{GAX}$

- **ALE/PROG**
  - $t_{SHGL}$, $t_{GLGH}$, $t_{GSHL}$

- **EA/$V_{PP}$**
  - $V_{PP}$, $t_{EHSN}$, $t_{EHQV}$, $t_{EHQz}$

- **P2.7 (ENABLE)**
  - $t_{GSHL}$

- **P3.4 (RDY/BSY)**

---

Flash Programming and Verification Waveforms - Low Voltage Mode ($V_{PP} = 5V$)

- **PORT 0**
  - DATA IN: $t_{AVGL}$, $t_{DVGL}$, $t_{GHDX}$, $t_{GAX}$
  - DATA OUT: $t_{AVOV}$, $t_{DVGL}$, $t_{GHDX}$, $t_{GAX}$

- **ALE/PROG**
  - $t_{SHGL}$, $t_{GLGH}$

- **EA/$V_{PP}$**
  - $V_{PP}$, $t_{EHSN}$, $t_{EHQV}$, $t_{EHQz}$

- **P2.7 (ENABLE)**
  - $t_{GSHL}$

- **P3.4 (RDY/BSY)**

---

4-36  AT89C51
### Absolute Maximum Ratings*

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Temperature</td>
<td>-55°C to +125°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage on Any Pin with Respect to Ground</td>
<td>-1.0V to +7.0V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum Operating Voltage</td>
<td>6.6V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DC Output Current</td>
<td>15.0 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*NOTICE:* Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### DC Characteristics

$T_A = -40°C$ to $85°C$, $V_{CC} = 5.0V ± 20%$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td>(Except EA)</td>
<td>-0.5</td>
<td>$0.2 V_{CC} - 0.1$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL1}$</td>
<td>Input Low Voltage (EA)</td>
<td>(Except XTAL1, RST)</td>
<td>-0.5</td>
<td>$0.2 V_{CC} - 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>(XTAL1, RST)</td>
<td>$0.2 V_{CC} - 0.9$</td>
<td>$V_{CC} - 0.5$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage (Ports 1,2,3)</td>
<td>$I_{OL} = 1.6$ mA</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL1}$</td>
<td>Output Low Voltage (Port 0, ALE, PSEN)</td>
<td>$I_{OL} = 3.2$ mA</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage (Ports 1,2,3, ALE, PSEN)</td>
<td>$I_{OH} = -0.5$ μA, $V_{CC} = 5V ± 10%$</td>
<td>2.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH1}$</td>
<td>Output High Voltage (Port 0 in External Bus Mode)</td>
<td>$I_{OH} = -25$ μA</td>
<td>0.75 $V_{CC}$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{OH}$</td>
<td></td>
<td>$I_{OH} = -10$ μA</td>
<td>0.9 $V_{CC}$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{OL}$</td>
<td></td>
<td>$I_{OL} = -800$ μA, $V_{CC} = 5V ± 10%$</td>
<td>2.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{OL}$</td>
<td></td>
<td>$I_{OH} = -300$ μA</td>
<td>0.75 $V_{CC}$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{OL}$</td>
<td></td>
<td>$I_{OH} = -80$ μA</td>
<td>0.9 $V_{CC}$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Logical 0 Input Current (Ports 1,2,3)</td>
<td>$V_{IN} = 0.45V$</td>
<td>-50</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Logical 1 to 0 Transition Current (Ports 1,2,3)</td>
<td>$V_{IN} = 2V, V_{CC} = 5V ± 10%$</td>
<td>-650</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Leakage Current (Port 0, EA)</td>
<td>$0.45 &lt; V_{IN} &lt; V_{CC}$</td>
<td>±10</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$RRST$</td>
<td>Reset Pulldown Resistor</td>
<td>$V_{IN} = 0.45V$</td>
<td>50</td>
<td>300</td>
<td>KΩ</td>
</tr>
<tr>
<td>$C_{IN}$</td>
<td>Pin Capacitance</td>
<td>Test Freq. = 1 MHz, $T_A = 25°C$</td>
<td>10</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Power Supply Current</td>
<td>Active Mode, 12 MHz</td>
<td>20</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Power Down Mode (2)</td>
<td>Idle Mode, 12 MHz</td>
<td>5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>Power Down</td>
<td>$V_{CC} = 5V$</td>
<td>100</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>Power Down</td>
<td>$V_{CC} = 3V$</td>
<td>40</td>
<td></td>
<td>μA</td>
</tr>
</tbody>
</table>

Notes:
1. Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:
   - Maximum $I_{OL}$ per port pin: 10 mA
   - Maximum $I_{OL}$ per 8-bit port: Port 0: 26 mA
     Port 1, 2, 3: 15 mA
   - Maximum total $I_{OL}$ for all output pins: 71 mA
   - If $I_{OL}$ exceeds the test condition, $V_{OL}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum $V_{CC}$ for Power Down is 2V.
### AC Characteristics
(Under Operating Conditions; Load Capacitance for Port 0, ALE/PROG, and PSEN = 100 pF; Load Capacitance for all other outputs = 80 pF)

### External Program and Data Memory Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>12 MHz Oscillator</th>
<th>16 to 24 MHz Oscillator</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{\text{CCLK}}$</td>
<td>Oscillator Frequency</td>
<td>Min</td>
<td>Max</td>
<td>MHz</td>
</tr>
<tr>
<td>$t_{\text{HLH}}$</td>
<td>ALE Pulse Width</td>
<td>127</td>
<td>$2t_{\text{CCLK}}$-40</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{WL}}$</td>
<td>Address Valid to ALE Low</td>
<td>43</td>
<td>$t_{\text{CCLK}}$-13</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{LAX}}$</td>
<td>Address Hold After ALE Low</td>
<td>48</td>
<td>$t_{\text{CCLK}}$-20</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{LV}}$</td>
<td>ALE Low to Valid Instruction In</td>
<td>233</td>
<td>$4t_{\text{CCLK}}$-65</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{LPL}}$</td>
<td>ALE Low to PSEN Low</td>
<td>43</td>
<td>$t_{\text{CCLK}}$-20</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{PLH}}$</td>
<td>PSEN Pulse Width</td>
<td>205</td>
<td>$3t_{\text{CCLK}}$-20</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{PLV}}$</td>
<td>PSEN Low to Valid Instruction In</td>
<td>145</td>
<td>$3t_{\text{CCLK}}$-45</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{PIX}}$</td>
<td>Input Instruction Hold After PSEN</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{PIXZ}}$</td>
<td>Input Instruction Float After PSEN</td>
<td>59</td>
<td>$t_{\text{CCLK}}$-10</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{XAV}}$</td>
<td>PSEN to Address Valid</td>
<td>75</td>
<td>$t_{\text{CCLK}}$-8</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{XIV}}$</td>
<td>Address to Valid Instruction In</td>
<td>312</td>
<td>$5t_{\text{CCLK}}$-55</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{PLAZ}}$</td>
<td>PSEN Low to Address Float</td>
<td>10</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{RPH}}$</td>
<td>RD Pulse Width</td>
<td>400</td>
<td>$6t_{\text{CCLK}}$-100</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{VLWH}}$</td>
<td>WR Pulse Width</td>
<td>400</td>
<td>$6t_{\text{CCLK}}$-100</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{RLD}}$</td>
<td>RD Low to Valid Data In</td>
<td>252</td>
<td>$5t_{\text{CCLK}}$-90</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{RHD}}$</td>
<td>Data Hold After RD</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{RHDZ}}$</td>
<td>Data Float After RD</td>
<td>97</td>
<td>$2t_{\text{CCLK}}$-28</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{LLD}}$</td>
<td>ALE Low to Valid Data In</td>
<td>517</td>
<td>$8t_{\text{CCLK}}$-150</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{AVD}}$</td>
<td>Address Valid to Data In</td>
<td>585</td>
<td>$9t_{\text{CCLK}}$-165</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{LLW}}$</td>
<td>ALE Low to RD or WR Low</td>
<td>200</td>
<td>$3t_{\text{CCLK}}$-50</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{AVW}}$</td>
<td>Address to RD or WR Low</td>
<td>203</td>
<td>$4t_{\text{CCLK}}$-75</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{DVX}}$</td>
<td>Data Valid to WR Transition</td>
<td>23</td>
<td>$t_{\text{CCLK}}$-20</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{DVWH}}$</td>
<td>Data Valid to WR High</td>
<td>433</td>
<td>$7t_{\text{CCLK}}$-120</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{WHG}}$</td>
<td>Data Hold After WR</td>
<td>33</td>
<td>$t_{\text{CCLK}}$-20</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{RLAZ}}$</td>
<td>RD Low to Address Float</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{WHEL}}$</td>
<td>RD or WR High to ALE High</td>
<td>43</td>
<td>$t_{\text{CCLK}}$-20</td>
<td>ns</td>
</tr>
</tbody>
</table>
External Program Memory Read Cycle

- ALE
- PSEN
- PORT 0
  - A0 - A7
  - INSTR IN
- PORT 2
  - A8 - A15

External Data Memory Read Cycle

- ALE
- PSEN
- RD
- PORT 0
  - A0 - A7 FROM RI OR DPX
  - DATA IN
  - A0 - A7 FROM PCL
- PORT 2
  - P2.0 - P2.7 OR A8 - A15 FROM DPX
  - A8 - A15 FROM PCX
External Data Memory Write Cycle

---

External Clock Drive Waveforms

---

External Clock Drive

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{CLCL}$</td>
<td>Oscillator Frequency</td>
<td>0</td>
<td>24</td>
<td>MHz</td>
</tr>
<tr>
<td>$t_{CLCH}$</td>
<td>Clock Period</td>
<td>41.6</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CHCX}$</td>
<td>High Time</td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CLKX}$</td>
<td>Low Time</td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CLCH}$</td>
<td>Rise Time</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CHCL}$</td>
<td>Fall Time</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>
Serial Port Timing: Shift Register Mode Test Conditions

\((V_{CC} = 5.0 \text{ V} \pm 20\% ; \text{ Load Capacitance} = 80 \text{ pF})\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>12 MHz Osc</th>
<th>Variable Oscillator</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{XLXL})</td>
<td>Serial Port Clock Cycle Time</td>
<td>Min 1.0</td>
<td>Max 12CLCL</td>
<td>µs</td>
</tr>
<tr>
<td>(t_{OVXH})</td>
<td>Output Data Setup to Clock Rising Edge</td>
<td>Min 700</td>
<td>Max 10CLCL-133</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{XHDX})</td>
<td>Output Data Hold After Clock Rising Edge</td>
<td>Min 50</td>
<td>Max 2CLCL-117</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{XHDV})</td>
<td>Input Data Hold After Clock Rising Edge</td>
<td>Min 0</td>
<td>Max 0</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{XHDV})</td>
<td>Clock Rising Edge to Input Data Valid</td>
<td>Min 700</td>
<td>Max 10CLCL-133</td>
<td>ns</td>
</tr>
</tbody>
</table>

Shift Register Mode Timing Waveforms

AC Testing Input/Output Waveforms

\(V_{CC} = 0.5V\)

\(-0.2 V_{CC} + 0.9V\)

TEST POINTS

\(-0.2 V_{CC} - 0.1V\)

Note: 1. AC Inputs during testing are driven at \(V_{CC} = 0.5V\) for a logic 1 and \(0.45V\) for a logic 0. Timing measurements are made at \(V_{TH}\) min. for a logic 1 and \(V_{IL}\) max. for a logic 0.

Float Waveforms

\(V_{LOAD} = 0.1V\)

\(V_{CL} = 0.1V\)

Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded \(V_{OH}/V_{OL}\) level occurs.
## Ordering Information

<table>
<thead>
<tr>
<th>Speed (MHz)</th>
<th>Power Supply</th>
<th>Ordering Code</th>
<th>Package</th>
<th>Operation Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>5V ± 20%</td>
<td>AT89C51-12AC</td>
<td>44A</td>
<td>Commercial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12JC</td>
<td>44J</td>
<td>(0°C to 70°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12PC</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12QC</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12AI</td>
<td>44A</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12JI</td>
<td>44J</td>
<td>(-40°C to 85°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12PI</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12QI</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12AA</td>
<td>44A</td>
<td>Automotive</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12JA</td>
<td>44J</td>
<td>(-40°C to 105°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12FA</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12QA</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>5V ± 20%</td>
<td>AT89C51-16AC</td>
<td>44A</td>
<td>Commercial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16JC</td>
<td>44J</td>
<td>(0°C to 70°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16PC</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16QC</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16AI</td>
<td>44A</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16JI</td>
<td>44J</td>
<td>(-40°C to 85°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16PI</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16QI</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16AA</td>
<td>44A</td>
<td>Automotive</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16JA</td>
<td>44J</td>
<td>(-40°C to 105°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16FA</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16QA</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>5V ± 20%</td>
<td>AT89C51-20AC</td>
<td>44A</td>
<td>Commercial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20JC</td>
<td>44J</td>
<td>(0°C to 70°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20PC</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20QC</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20AI</td>
<td>44A</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20JI</td>
<td>44J</td>
<td>(-40°C to 85°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20PI</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20QI</td>
<td>44Q</td>
<td></td>
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</table>
## Ordering Information

<table>
<thead>
<tr>
<th>Speed (MHz)</th>
<th>Power Supply</th>
<th>Ordering Code</th>
<th>Package</th>
<th>Operation Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>5V ± 20%</td>
<td>AT89C51-24AC</td>
<td>44A</td>
<td>Commercial (0°C to 70°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24JC</td>
<td>44J</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24PC</td>
<td>44P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24QC</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24AI</td>
<td>44A</td>
<td>Industrial (-40°C to 85°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24JI</td>
<td>44J</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24PI</td>
<td>44P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24QI</td>
<td>44Q</td>
<td></td>
</tr>
</tbody>
</table>

### Package Type

<table>
<thead>
<tr>
<th>Package Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>44A</td>
<td>44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)</td>
</tr>
<tr>
<td>44J</td>
<td>44 Lead, Plastic J-Leaded Chip Carrier (PLCC)</td>
</tr>
<tr>
<td>40P6</td>
<td>40 Lead, 0.600&quot; Wide, Plastic Dual Inline Package (PDIP)</td>
</tr>
<tr>
<td>44Q</td>
<td>44 Lead, Plastic Gull Wing Quad Flatpack (PQFP)</td>
</tr>
</tbody>
</table>
82C55A
CHMOS PROGRAMMABLE PERIPHERAL INTERFACE

- Compatible with all Intel and Most Other Microprocessors
- High Speed, "Zero Wait State" Operation with 8 MHz 8086/88 and 80186/188
- 24 Programmable I/O Pins
- Low Power CHMOS
- Completely TTL Compatible

The Intel 82C55A is a high-performance, CHMOS version of the industry standard 8255A general purpose programmable I/O device which is designed for use with all Intel and most other microprocessors. It provides 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The 82C55A is pin compatible with the NMOS 8255A and 8255A-5.

In MODE 0, each group of 12 I/O pins may be programmed in sets of 4 and 8 to be inputs or outputs. In MODE 1, each group may be programmed to have 8 lines of input or output. 3 of the remaining 4 pins are used for handshaking and interrupt control signals. MODE 2 is a strobed bi-directional bus configuration.

The 82C55A is fabricated on Intel's advanced CHMOS III technology which provides low power consumption with performance equal to or greater than the equivalent NMOS product. The 82C55A is available in 40-pin DIP and 44-pin plastic leaded chip carrier (PLCC) packages.

Figure 1. 82C55A Block Diagram
Figure 2. 82C55A Pinout
Diagrams are for pin reference only. Package sizes are not to scale.
## Table 1. Pin Description

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Pin Number Dip</th>
<th>Pin Number PLCC</th>
<th>Type</th>
<th>Name and Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>PA&lt;sub&gt;3&lt;/sub&gt;-&lt;sub&gt;0&lt;/sub&gt;</td>
<td>1–4</td>
<td>2–5</td>
<td>I/O</td>
<td>PORT A, PINS 0–3: Lower nibble of an 8-bit data output latch/buffer and an 8-bit data input latch.</td>
</tr>
<tr>
<td>RD</td>
<td>5</td>
<td>6</td>
<td>I</td>
<td>READ CONTROL: This input is low during CPU read operations.</td>
</tr>
<tr>
<td>CS</td>
<td>6</td>
<td>7</td>
<td>I</td>
<td>CHIP SELECT: A low on this input enables the 82C55A to respond to RD and WR signals. RD and WR are ignored otherwise.</td>
</tr>
<tr>
<td>GND</td>
<td>7</td>
<td>8</td>
<td>I</td>
<td>System Ground</td>
</tr>
<tr>
<td>A&lt;sub&gt;1&lt;/sub&gt;-&lt;sub&gt;0&lt;/sub&gt;</td>
<td>8–9</td>
<td>9–10</td>
<td>I</td>
<td>ADDRESS: These input signals, in conjunction RD and WR, control the selection of one of the three ports or the control word registers.</td>
</tr>
</tbody>
</table>

### Input Operation (Read)

<table>
<thead>
<tr>
<th>A&lt;sub&gt;1&lt;/sub&gt;</th>
<th>A&lt;sub&gt;0&lt;/sub&gt;</th>
<th>RD</th>
<th>WR</th>
<th>CS</th>
<th>Data Bus - Port A</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Port A - Data Bus</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Port B - Data Bus</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Port C - Data Bus</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Control Word - Data Bus</td>
</tr>
</tbody>
</table>

### Output Operation (Write)

<table>
<thead>
<tr>
<th>X</th>
<th>X</th>
<th>X</th>
<th>X</th>
<th>1</th>
<th>Data Bus - 3 - State</th>
</tr>
</thead>
</table>

### Disable Function

| X | X | 1 | 0 | Data Bus - 3 - State |


| PC<sub>0</sub>-<sub>3</sub> | 14–17 | 16–19 | I/O | PORT C, PINS 0–3: Lower nibble of Port C. |

| PB<sub>0</sub>-<sub>7</sub> | 18–25 | 20–22, 24–28 | I/O | PORT B, PINS 0–7: An 8-bit data output latch/buffer and an 8-bit data input buffer. |

| V<sub>CC</sub> | 26 | 20 | I/O | SYSTEM POWER: +5V Power Supply |

| D<sub>7</sub>-<sub>0</sub> | 27–34 | 30–33, 35–38 | I/O | DATA BUS: Bi-directional, tri-state data bus lines, connected to system data bus. |

| RESET | 35 | 39 | I | RESET: A high on this input clears the control register and all ports are set to the input mode. |

| WR | 36 | 40 | I | WRITE CONTROL: This input is low during CPU write operations. |


| NC | 1, 12, 23, 34 | | | No Connect |
82C55A FUNCTIONAL DESCRIPTION

General

The 82C55A is a programmable peripheral interface device designed for use in Intel microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 82C55A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

Group A and Group B Controls

The functional configuration of each port is programmed by the system software. In essence, the CPU "outputs" a control word to the 82C55A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 82C55A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper (C7–C4)
Control Group B - Port B and Port C lower (C3–C0)

The control word register can be both written and read as shown in the address decode table in the pin descriptions. Figure 6 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic "1", as this implies control word mode information.

Ports A, B, and C

The 82C55A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 82C55A.

Port A. One 8-bit data output latch/buffer and one 8-bit input latch buffer. Both "pull-up" and "pull-down" bus hold devices are present on Port A.

Port B. One 8-bit data input/output latch/buffer. Only "pull-up" bus hold devices are present on Port B.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. Only "pull-up" bus hold devices are present on Port C.

See Figure 4 for the bus-hold circuit configuration for Port A, B, and C.
Figure 3. 82C55A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions

*NOTE:*
Port pins loaded with more than 20 pF capacitance may not have their logic level guaranteed following a hardware reset.
82C55A OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 — Basic input/output
Mode 1 — Strobed Input/output
Mode 2 — Bi-directional Bus

When the reset input goes “high” all ports will be set to the input mode with all 24 port lines held at a logic “one” level by the internal bus hold devices (see Figure 4 Note). After the reset is removed the 82C55A can remain in the input mode with no additional initialization required. This eliminates the need for pullup or pulldown devices in “all CMOS” designs. During the execution of the system program, any of the other modes may be selected by using a single output instruction. This allows a single 82C55A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be “tailored” to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTPUT instruction. This feature reduces software requirements in Control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.
Interrupt Control Functions

When the 82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

- (BIT-SET) — INTE is SET — Interrupt enable
- (BIT-RESET) — INTE is RESET — Interrupt disable

Note:
All Mask flip-flops are automatically reset during mode selection and device Reset.
Operating Modes

Mode 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No “handshaking” is required, data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:
- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.
### MODE 0 Port Definition

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>GROUP A</th>
<th>GROUP B</th>
</tr>
</thead>
<tbody>
<tr>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
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</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
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<td>1</td>
<td>0</td>
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<td>1</td>
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<td>1</td>
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<td>1</td>
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</tr>
<tr>
<td>1</td>
<td>0</td>
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</tr>
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<td>1</td>
<td>0</td>
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<td>1</td>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

### MODE 0 Configurations

- **CONTROL WORD #1**
- **CONTROL WORD #2**
- **CONTROL WORD #3**

![Diagram](image-url)
Operating Modes

**MODE 1 (Strobed Input/Output).** This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic functional Definitions:
- Two Groups (Group A and Group B).
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output.
- Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.
Input Control Signal Definition

STB (Strobe Input). A “low” on this input loads data into the input latch.

IBF (Input Buffer Full F/F)
A “high” on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

INTR (Interrupt Request)
A “high” on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the STB is a “one”, IBF is a “one” and INTE is a “one”. It is reset by the falling edge of RD. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A
Controlled by bit set/reset of PC4.

INTE B
Controlled by bit set/reset of PC2.

Figure 8. MODE 1 Input

Figure 9. MODE 1 (Strobed Input)
82C55A

Output Control Signal Definition

**OBF (Output Buffer Full F/F)**. The OBF output will go "low" to indicate that the CPU has written data out to the specified port. The OBF F/F will be set by the rising edge of the WR input and reset by ACK input being low.

**ACK (Acknowledge Input)**. A "low" on this input informs the 82C55A that the data from Port A or Port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

**INTR (Interrupt Request)**. A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when ACK is a "one", OBF is a "one" and INTE is a "one". It is reset by the falling edge of WR.

**INTE A**
Controlled by bit set/reset of PC6.

**INTE B**
Controlled by bit set/reset of PC2.

---

**Figure 10. MODE 1 Output**

**Figure 11. MODE 1 (Strobed Output)**
Combinations of MODE 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

Figure 12. Combinations of MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O). This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus port (Port A) and a 5-bit control port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for input or output operations.

Output Operations

ØBF (Output Buffer Full). The ØBF output will go "low" to indicate that the CPU has written data out to port A.

ACK (Acknowledge). A "low" on this input enables the tri-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high impedance state.


Input Operations

STB (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

Figure 13. MODE Control Word

Figure 14. MODE 2

Figure 15. MODE 2 (Bidirectional)

NOTE:
Any sequence where WR occurs before ACK, and STB occurs before RD is permissible. (INTR = IBF + MASK + STB + RD + OBF + MASK + ACK + WR)
Figure 16. MODE 1/4 Combinations
## Mode Definition Summary

<table>
<thead>
<tr>
<th>MODE 0</th>
<th>MODE 1</th>
<th>MODE 2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PA0</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PA1</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PA2</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PA3</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PA4</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PA5</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PA6</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PA7</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PB0</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PB1</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PB2</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PB3</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PB4</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PB5</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PB6</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PB7</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PC0</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PC1</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PC2</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PC3</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PC4</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PC5</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PC6</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>PC7</td>
<td>IN</td>
<td>OUT</td>
</tr>
</tbody>
</table>

### Special Mode Combination Considerations

There are several combinations of modes possible. For any combination, some or all of the Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.

During a read of Port C, the state of all the Port C lines, except the ACK and STB lines, will be placed on the data bus. In place of the ACK and STB line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 18.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C" command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port C Bit" command, any Port C line programmed as an output (including INTR, IBF, and OBF) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including ACK and STB lines, associated with Port C are not affected by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the ACK and STB lines with the "Set/Reset Port C Bit" command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 18.

### Current Drive Capability

Any output on Port A, B or C can sink or source 2.5 mA. This feature allows the 82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.
Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts “hand-shaking” signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the “status” of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

**Figure 17a. MODE 1 Status Word Format**

<table>
<thead>
<tr>
<th>Interrupt Enable Flag</th>
<th>Position</th>
<th>Alternate Port C Pin Signal (Mode)</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTE B</td>
<td>PC2</td>
<td>ACKA (Output Mode 1) or STB (Input Mode 1)</td>
</tr>
<tr>
<td>INTE A2</td>
<td>PC4</td>
<td>STB (Input Mode 1 or Mode 2)</td>
</tr>
<tr>
<td>INTE A1</td>
<td>PC6</td>
<td>ACKA (Output Mode 1 or Mode 2)</td>
</tr>
</tbody>
</table>

Figure 18. Interrupt Enable Flags in Modes 1 and 2
### ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ........... -40°C to + 70°C  
Storage Temperature ...................... -65°C to +150°C  
Supply Voltage .......................... -0.5V to +8.0V  
Operating Voltage ....................... +4V to +7V  
Voltage on any Input ...................... GND - 2V to +6.5V  
Voltage on any Output ..................... GND - 0.5V to VCC + 0.5V  
Power Dissipation ....................... 1 Watt

 NOTICE: This is a production data sheet. The specifications are subject to change without notice.

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

### D.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = +5V$ ± 10%, GND = 0V ($T_A = -40°C$ to + 85°C for Extended Temperature)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td>-0.5</td>
<td>0.8</td>
<td>V</td>
<td>$V_{IN} = V_{CC}$ to 0V (Note 1)</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>2.0</td>
<td>$V_{CC}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage</td>
<td>0.4</td>
<td>V</td>
<td>$I_{OL} = 2.5mA$</td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage</td>
<td>3.0</td>
<td>$V_{CC} - 0.4$</td>
<td>V</td>
<td>$I_{OH} = -2.5mA$, $I_{OH} = -100 \mu A$</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Leakage Current</td>
<td>± 1</td>
<td>$\mu A$</td>
<td>$V_{IN} = V_{CC}$ to 0V (Note 1)</td>
<td></td>
</tr>
<tr>
<td>$I_{OFL}$</td>
<td>Output Float Leakage Current</td>
<td>10</td>
<td>$\mu A$</td>
<td>$V_{IN} = V_{CC}$ to 0V (Note 2)</td>
<td></td>
</tr>
<tr>
<td>$I_{OAR}$</td>
<td>Darlington Drive Current</td>
<td>± 2.5</td>
<td>(Note 4)</td>
<td>mA</td>
<td>Ports A, B, C $R_{ext} = 500\Omega$, $V_{ext} = 1.7V$</td>
</tr>
<tr>
<td>$I_{PHL}$</td>
<td>Port Hold Low Leakage Current</td>
<td>+50</td>
<td>+300</td>
<td>$\mu A$</td>
<td>$V_{OUT} = 1.0V$ Port A only</td>
</tr>
<tr>
<td>$I_{PHH}$</td>
<td>Port Hold High Leakage Current</td>
<td>-50</td>
<td>-300</td>
<td>$\mu A$</td>
<td>$V_{OUT} = 3.0V$ Ports A, B, C</td>
</tr>
<tr>
<td>$I_{PLO}$</td>
<td>Port Hold Low Overdrive Current</td>
<td>-350</td>
<td>$\mu A$</td>
<td>$V_{OUT} = 0.8V$</td>
<td></td>
</tr>
<tr>
<td>$I_{PHO}$</td>
<td>Port Hold High Overdrive Current</td>
<td>+350</td>
<td>$\mu A$</td>
<td>$V_{OUT} = 3.0V$</td>
<td></td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>$V_{CC}$ Supply Current</td>
<td>10</td>
<td>mA</td>
<td>(Note 3)</td>
<td></td>
</tr>
<tr>
<td>$I_{CCSB}$</td>
<td>$V_{CC}$ Supply Current-Standby</td>
<td>10</td>
<td>$\mu A$</td>
<td>$V_{CC} = 5.5V$ $V_{IN} = V_{CC}$ or GND Port Conditions If I/P = Open/High $O/P = $ Open Only With Data Bus = High/Low $CS = $ High Reset = Low Pure Inputs = Low/High</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. Pins $A_1$, $A_0$, $CS$, $WR$, $RD$, Reset.  
2. Data Bus, Ports B, C.  
3. Outputs open.  
4. Limit output current to 4.0 mA.
CAPACITANCE
$T_A = 25^\circ C, V_{CC} = GND = 0V$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_IN</td>
<td>Input Capacitance</td>
<td>10</td>
<td></td>
<td>pF</td>
<td>Unmeasured pins returned to GND $f_c = 1 \text{ MHz}(5)$</td>
</tr>
<tr>
<td>C_I/O</td>
<td>I/O Capacitance</td>
<td>20</td>
<td></td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>

NOTE:
5. Sampled not 100% tested.

A.C. CHARACTERISTICS
$T_A = 0^\circ \text{C to } 70^\circ \text{C}, V_{CC} = +5V \pm 10\%, GND = 0V$
$T_A = -40^\circ \text{C to } 185^\circ \text{C for Extended Temperature}$

BUS PARAMETERS

READ CYCLE

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>$82C55A-2$</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td></td>
</tr>
<tr>
<td>$t_{AR}$</td>
<td>Address Stable Before RD $\downarrow$</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{RA}$</td>
<td>Address Hold Time After RD $\uparrow$</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{RR}$</td>
<td>RD Pulse Width</td>
<td>150</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{RD}$</td>
<td>Data Delay from RD $\downarrow$</td>
<td></td>
<td>120</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{DF}$</td>
<td>RD $\uparrow$ to Data Floating</td>
<td>10</td>
<td>75</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{RV}$</td>
<td>Recovery Time between RD/WR</td>
<td>200</td>
<td></td>
<td></td>
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</tbody>
</table>

WRITE CYCLE

<table>
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<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>$82C55A-2$</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td></td>
</tr>
<tr>
<td>$t_{AW}$</td>
<td>Address Stable Before WR $\downarrow$</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{WA}$</td>
<td>Address Hold Time After WR $\uparrow$</td>
<td>20</td>
<td></td>
<td>ns (Ports A &amp; B)</td>
</tr>
<tr>
<td>$t_{WW}$</td>
<td>WR Pulse Width</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{DW}$</td>
<td>Data Setup Time Before WR $\uparrow$</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{WD}$</td>
<td>Data Hold Time After WR $\uparrow$</td>
<td>30</td>
<td></td>
<td>ns (Ports A &amp; B)</td>
</tr>
</tbody>
</table>

19
### OTHER TIMINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>lWB</td>
<td>WR = 1 to Output</td>
<td>82C55A-2</td>
</tr>
<tr>
<td>tHR</td>
<td>Peripheral Data Before RD</td>
<td>ns</td>
</tr>
<tr>
<td>tHR</td>
<td>Peripheral Data After RD</td>
<td>ns</td>
</tr>
<tr>
<td>tAK</td>
<td>ACK Pulse Width</td>
<td>ns</td>
</tr>
<tr>
<td>tST</td>
<td>STB Pulse Width</td>
<td>ns</td>
</tr>
<tr>
<td>tAS</td>
<td>Per. Data Before STB High</td>
<td>ns</td>
</tr>
<tr>
<td>tPH</td>
<td>Per. Data After STB High</td>
<td>ns</td>
</tr>
<tr>
<td>tAD</td>
<td>ACK = 0 to Output</td>
<td>ns</td>
</tr>
<tr>
<td>tKD</td>
<td>ACK = 1 to Output Float</td>
<td>ns</td>
</tr>
<tr>
<td>tWOB</td>
<td>WR = 1 to OBF = 0</td>
<td>ns</td>
</tr>
<tr>
<td>tAOB</td>
<td>ACK = 0 to OBF = 1</td>
<td>ns</td>
</tr>
<tr>
<td>tSIB</td>
<td>STB = 0 to IBF = 1</td>
<td>ns</td>
</tr>
<tr>
<td>tSB</td>
<td>RD = 1 to IBF = 0</td>
<td>ns</td>
</tr>
<tr>
<td>tRIT</td>
<td>RD = 0 to INTR = 0</td>
<td>ns</td>
</tr>
<tr>
<td>tSIT</td>
<td>STB = 1 to INTR = 1</td>
<td>ns</td>
</tr>
<tr>
<td>tAIT</td>
<td>ACK = 0 to INTR = 1</td>
<td>ns</td>
</tr>
<tr>
<td>tWIT</td>
<td>WR = 0 to INTR = 0</td>
<td>ns</td>
</tr>
<tr>
<td>tRES</td>
<td>Reset Pulse Width</td>
<td>ns</td>
</tr>
</tbody>
</table>

**NOTE:**
1. INTR ↑ may occur as early as WR ↓.
2. Pulse width of initial Reset pulse after power on must be at least 50 μSec. Subsequent Reset pulses may be 500 ns minimum. The output Ports A, B, or C may glitch low during the reset pulse but all port pins will be held at a logic "one" level after the reset pulse.
WAVEFORMS (Continued)

MODE 1 (STROBED INPUT)

MODE 1 (STROBED OUTPUT)
**WAVEFORMS (Continued)**

**MODE 2 (BIDIRECTIONAL)**

Note:
Any sequence where WR occurs before ACK AND STB occurs before RD is permissible.
(INTR = IBF • MASK • STB • RD + OBF • MASK • ACK • WR)

**WRITE TIMING**

**READ TIMING**

**A.C. TESTING INPUT, OUTPUT WAVEFORM**

**DEVICE LOAD CIRCUIT**

A.C. Testing Inputs Are Driven At 2.4V For A Logic 1 And 0.45V For A Logic 0. Timing Measurements Are Made At 2.0V For A Logic 1 And 0.8 For A Logic 0.

*VEXT is Set At Various Voltages During Testing To Guarantee The Specification. CL Includes Jig Capacitance.*

---

(A digital logic diagram with timing notations and waveforms, followed by text explanations for each section.)
74LV573
Octal D-type transparent latch (3-State)

Product specification
Supersedes data of 1997 Jun 06
IC24 Data Handbook

1998 Jun 10
Octal D-type transparent latch (3-State) 74LV573

**FEATURES**
- Wide operating voltage: 1.0 to 5.5V
- Optimized for low voltage applications: 1.0V to 3.6V
- Absolute input voltage: VCC = 2.7V and VIL = 0.8V
- Typical IOCL (output ground bounce) < 0.8V at VCC = 3.3V, t<sub>min</sub> = 25°C
- Typical VOLH (output VOH undershoot) > 2V at VCC = 3.3V, t<sub>max</sub> = 25°C
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Use as input or output port for microprocessors/microcomputer
- Common 3-State output enable input
- Output capability: bus driver
- VCC category: MSI

**DESCRIPTION**
The 74LV573 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT573.

The 74LV573 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus controlled applications. A latch enable (LE) input and an output enable (OE) input are common to all internal latches.

The 573 consists of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the D inputs enter the latches. In this condition the latches are transparent, i.e., a latch output will change at the same time as its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a setup time preceding the HIGH-to-LOW transition of LE. When OE is LOW, the contents of the eight latches are available at the outputs. When OE is HIGH, the outputs go to the high impedance OFF state. Operation of the OE input does not affect the state of the latches.

The 573 is functionally identical to the '563 and '373, but the '563 has inverted outputs and the '373 has a different pin arrangement.

**QUICK REFERENCE DATA**
GND = 0V, T<sub>AMB</sub> = 25°C, t<sub>L</sub> = t<sub>H</sub> ≤ 2.5 ns

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>TYPICAL</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>P&lt;sub&gt;DL&lt;/sub&gt;</td>
<td>Propagation delay</td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 15pF, V&lt;sub&gt;CC&lt;/sub&gt; = 3.3V</td>
<td>12</td>
<td>ns</td>
</tr>
<tr>
<td>C&lt;sub&gt;L&lt;/sub&gt;</td>
<td>Input capacitance</td>
<td></td>
<td>13</td>
<td></td>
</tr>
<tr>
<td>C&lt;sub&gt;PD&lt;/sub&gt;</td>
<td>Power dissipation capacitance per latch</td>
<td>Notes 1, 2</td>
<td>3.5</td>
<td>pF</td>
</tr>
<tr>
<td>C&lt;sub&gt;PD&lt;/sub&gt;</td>
<td>Power dissipation capacitance per latch</td>
<td>Notes 1, 2</td>
<td>20</td>
<td>pF</td>
</tr>
</tbody>
</table>

**NOTES:**
1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in mW): P<sub>D</sub> = C<sub>PD</sub> x f<sub>I</sub> x V<sup>2</sup><sub>CC</sub> + f<sub>O</sub> x (C<sub>L</sub> + V<sup>2</sup><sub>CC</sub>) + f<sub>I</sub> x V<sup>2</sup><sub>CC</sub>)
2. The condition is V<sub>L</sub> = GND to V<sub>CC</sub>.

**ORDERING AND PACKAGE INFORMATION**

<table>
<thead>
<tr>
<th>PACKAGES</th>
<th>TEMPERATURE RANGE</th>
<th>OUTSIDE NORTH AMERICA</th>
<th>NORTH AMERICA</th>
<th>PKG. DWG. #</th>
</tr>
</thead>
<tbody>
<tr>
<td>20-Pin Plastic DIL</td>
<td>-40°C to +125°C</td>
<td>74LV573 N</td>
<td>74LV573 N</td>
<td>SOT146-1</td>
</tr>
<tr>
<td>20-Pin Plastic SO</td>
<td>-40°C to +125°C</td>
<td>74LV573 D</td>
<td>74LV573 D</td>
<td>SOT163-1</td>
</tr>
<tr>
<td>25-Pin Plastic SSOP Type II</td>
<td>-40°C to +125°C</td>
<td>74LV573 DB</td>
<td>74LV573 DB</td>
<td>SOT133-1</td>
</tr>
<tr>
<td>20-Pin Plastic SSOP Type III</td>
<td>-40°C to +125°C</td>
<td>74LV573 FW</td>
<td>74LV573 FW UH</td>
<td>SOT130-1</td>
</tr>
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</table>

**PIN DESCRIPTION**

<table>
<thead>
<tr>
<th>PIN NUMBER</th>
<th>SYMBOL</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OE</td>
<td>Output enable input (active LOW)</td>
</tr>
<tr>
<td>2, 3, 4, 5, 6, 7, 8, 9</td>
<td>D0-D7</td>
<td>Data inputs</td>
</tr>
<tr>
<td>16, 17, 18, 19, 15, 14, 13, 12</td>
<td>Q0-Q7</td>
<td>Data outputs</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>Ground (0V)</td>
</tr>
<tr>
<td>11</td>
<td>LE</td>
<td>Latch enable input (active HIGH)</td>
</tr>
<tr>
<td>20</td>
<td>VCC</td>
<td>Positive supply voltage</td>
</tr>
</tbody>
</table>

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**FUNCTION TABLE**

<table>
<thead>
<tr>
<th>OPERATING MODES</th>
<th>INPUTS</th>
<th>INTERNAL LATCHES</th>
<th>OUTPUTS Q0 to Q7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Latch and read register (transient mode)</td>
<td>L</td>
<td>H, L</td>
<td>L</td>
</tr>
<tr>
<td></td>
<td>L</td>
<td>H, H</td>
<td>L</td>
</tr>
<tr>
<td>Latch and read register</td>
<td>L</td>
<td>H, L</td>
<td>L</td>
</tr>
<tr>
<td></td>
<td>L</td>
<td>H, H</td>
<td>L</td>
</tr>
<tr>
<td>Latch register and disable outputs</td>
<td>H</td>
<td>L, L</td>
<td>L, Z</td>
</tr>
<tr>
<td></td>
<td>H</td>
<td>L, H</td>
<td>L, Z</td>
</tr>
</tbody>
</table>

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LC transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LC transition
Z = High impedance OFF-state

**PIN CONFIGURATION**

**LOGIC SYMBOL**
**ABSOLUTE MAXIMUM RATINGS**¹,²

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>RATING</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(DD)</td>
<td>DC supply voltage</td>
<td>-0.5 to +7.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I IDK</td>
<td>DC input diode current</td>
<td>V I ≤ 0.5 or V I &gt; VCC + 0.5V</td>
<td>20</td>
<td>mA</td>
</tr>
<tr>
<td>I ODK</td>
<td>DC output diode current</td>
<td>V O ≤ -0.5 or V O &gt; VCC + 0.5V</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td>I IM</td>
<td>DC output source or sink current</td>
<td>-0.5V &lt; VO &lt; VCC + 0.5V</td>
<td>35</td>
<td>mA</td>
</tr>
<tr>
<td>I (CC)</td>
<td>DC VCC or GND current for types with open-collector or open-drain outputs</td>
<td>-0.5V &lt; VO &lt; VCC + 0.5V</td>
<td>70</td>
<td>mA</td>
</tr>
<tr>
<td>T SS</td>
<td>Storage temperature range</td>
<td>-65 to +150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>P TOT</td>
<td>Power dissipation per package</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-plastic DIL</td>
<td>for temperature range: -40 to +125°C</td>
<td>750</td>
<td>W</td>
<td></td>
</tr>
<tr>
<td>-plastic mini-pack (SO)</td>
<td>above +70°C derate linearly with 12mW/K</td>
<td>500</td>
<td>mW/K</td>
<td></td>
</tr>
<tr>
<td>-plastic shrink mini-pack (SSOP and TSSOP)</td>
<td>above +60°C derate linearly with 5.5 mW/K</td>
<td>400</td>
<td>mW/K</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

**RECOMMENDED OPERATING CONDITIONS**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP.</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(DD)</td>
<td>DC supply voltage</td>
<td>See Note 1</td>
<td>1.0</td>
<td>3.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>V I</td>
<td>Input voltage</td>
<td>0</td>
<td>-</td>
<td>VCC</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V O</td>
<td>Output voltage</td>
<td>0</td>
<td>-</td>
<td>VCC</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>T amin</td>
<td>Operating ambient temperature range in free air</td>
<td>See DC and AC characteristics</td>
<td>-40</td>
<td>-40</td>
<td>+85</td>
<td>°C</td>
</tr>
<tr>
<td>t £</td>
<td>Input rise and fall times</td>
<td>VCC = 1.0V to 2.0V</td>
<td>-</td>
<td>-</td>
<td>500</td>
<td>ns/V</td>
</tr>
<tr>
<td>t £</td>
<td></td>
<td>VCC = 2.0V to 2.7V</td>
<td>-</td>
<td>-</td>
<td>200</td>
<td>ns/V</td>
</tr>
<tr>
<td>t £</td>
<td></td>
<td>VCC = 2.7V to 3.6V</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>ns/V</td>
</tr>
<tr>
<td>t £</td>
<td></td>
<td>VCC = 3.6V to 5.5V</td>
<td>-</td>
<td>-</td>
<td>50</td>
<td>ns/V</td>
</tr>
</tbody>
</table>

**NOTE:**
1. The LV is guaranteed to function down to VCC = 1.0V (input levels GND or VCC). DC characteristics are guaranteed from VCC = 1.2V to VCC = 5.5V.
DC CHARACTERISTICS FOR THE LV FAMILY
Over recommended operating conditions voltages are referenced to GND (ground = 0V)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>LIMITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{IH}</td>
<td>HIGH level Input voltage</td>
<td>V_{CC} = 1.2V</td>
<td>0.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 2.0V</td>
<td>MIN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 2.7 to 3.6V</td>
<td>1.4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 4.5 to 5.5V</td>
<td>MAX</td>
</tr>
<tr>
<td>V_{IL}</td>
<td>LOW level Input voltage</td>
<td>V_{CC} = 1.2V</td>
<td>0.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 2.0V</td>
<td>MIN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 2.7 to 3.6V</td>
<td>0.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 4.5 to 5.5V</td>
<td>MAX</td>
</tr>
<tr>
<td>V_{TH}</td>
<td>HIGH level output voltage; all outputs</td>
<td>V_{CC} = 1.2V; V_{IH} = V_{HLM} or V_{ILH}; V_{OC} = 100\mu A</td>
<td>0.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 2.0V; V_{IH} = V_{HLM} or V_{ILH}; V_{OC} = 100\mu A</td>
<td>MIN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 2.7V; V_{IH} = V_{HLM} or V_{ILH}; V_{OC} = 100\mu A</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 3.0V; V_{IH} = V_{HLM} or V_{ILH}; V_{OC} = 100\mu A</td>
<td>2.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 4.5V; V_{IH} = V_{HLM} or V_{ILH}; V_{OC} = 100\mu A</td>
<td>4.3</td>
</tr>
<tr>
<td>V_{OH}</td>
<td>HIGH level output voltage; BUS driver outputs</td>
<td>V_{CC} = 3.0V; V_{IH} = V_{HLM} or V_{ILH}; V_{OC} = 8mA</td>
<td>2.4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 4.5V; V_{IH} = V_{HLM} or V_{ILH}; V_{OC} = 16mA</td>
<td>3.6</td>
</tr>
<tr>
<td>V_{OL}</td>
<td>LOW level output voltage; all outputs</td>
<td>V_{CC} = 1.2V; V_{IL} = V_{HLM} or V_{ILH}; V_{OC} = 100\mu A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 2.0V; V_{IL} = V_{HLM} or V_{ILH}; V_{OC} = 100\mu A</td>
<td>MIN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 2.7V; V_{IL} = V_{HLM} or V_{ILH}; V_{OC} = 100\mu A</td>
<td>0.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 3.0V; V_{IL} = V_{HLM} or V_{ILH}; V_{OC} = 100\mu A</td>
<td>0.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 4.5V; V_{IL} = V_{HLM} or V_{ILH}; V_{OC} = 100\mu A</td>
<td>0.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 3.0V; V_{IL} = V_{HLM} or V_{ILH}; V_{OC} = 8mA</td>
<td>0.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 4.5V; V_{IL} = V_{HLM} or V_{ILH}; V_{OC} = 16mA</td>
<td>0.35</td>
</tr>
<tr>
<td>I_{L}</td>
<td>Input leakage current</td>
<td>V_{CC} = 5.5V; V_{IH} = V_{CC} or GND</td>
<td>1</td>
</tr>
<tr>
<td>I_{OZ}</td>
<td>3-State output OFF-state current</td>
<td>V_{CC} = 5.5V; V_{IH} = V_{ILH}; V_{0} = V_{CC} or GND</td>
<td>5</td>
</tr>
<tr>
<td>I_{CC}</td>
<td>Quiescent supply current</td>
<td>V_{CC} = 5.5V; V_{IH} = V_{CC} or GND; V_{OC} = 0</td>
<td>20</td>
</tr>
<tr>
<td>I_{CC}</td>
<td>Additional quiescent supply current per input</td>
<td>V_{CC} = 2.7V to 3.6V; V_{IH} = V_{CC} or -0.6V</td>
<td>500</td>
</tr>
</tbody>
</table>

**NOTE:**
- All typical values are measured at T_{amb} = 25°C.
### AC CHARACTERISTICS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>WAVEFORM</th>
<th>CONDITION</th>
<th>LIMITS -40 to +85 °C</th>
<th>LIMITS -40 to +125 °C</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>t(_{PH,APLH})</td>
<td>Propagation delay Dn to On</td>
<td>Figures 1, 5</td>
<td>V(_{CC})(V)</td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
</tr>
<tr>
<td>t(_{PL,APLH})</td>
<td>Propagation delay LE to On</td>
<td>Figures 2, 5</td>
<td>1.2</td>
<td>-</td>
<td>75</td>
<td>-</td>
</tr>
<tr>
<td>t(_{PH,APZL})</td>
<td>3-State output enable time OE to On</td>
<td>Figures 3, 5</td>
<td>2.0</td>
<td>-</td>
<td>27</td>
<td>-</td>
</tr>
<tr>
<td>t(_{PH,APZL})</td>
<td>3-State output disable time OE to On</td>
<td>Figures 3, 5</td>
<td>3.0</td>
<td>-</td>
<td>152</td>
<td>-</td>
</tr>
<tr>
<td>t(_{PH,APZL})</td>
<td>3-State output disable time OE to On</td>
<td>Figures 3, 5</td>
<td>4.5</td>
<td>-</td>
<td>21</td>
<td>-</td>
</tr>
<tr>
<td>(t(_{PWH}))</td>
<td>LE pulse width HIGH</td>
<td>Figure 2</td>
<td>2.0</td>
<td>-</td>
<td>34</td>
<td>-</td>
</tr>
<tr>
<td>(t(_{PH}))</td>
<td>Setup time Dn to LE</td>
<td>Figure 4</td>
<td>3.0</td>
<td>-</td>
<td>20</td>
<td>-</td>
</tr>
<tr>
<td>(t(_{H}))</td>
<td>Hold time Dn to LE</td>
<td>Figure 4</td>
<td>4.5</td>
<td>-</td>
<td>20</td>
<td>-</td>
</tr>
</tbody>
</table>

**NOTES:**

All typical values are measured at \(T_{Amb} = 25^\circ C\)

1. Typical values are measured at \(V_{CC} = 3.3\) V

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AC WAVEFORMS

$V_{IH} = 1.5V$ at $V_{CC} \geq 2.7V$ and $\leq 3.6V$

$V_{IL} = 0.5^*V_{CC}$ at $V_{CC} < 2.7V$ and $\geq 4.5V$

$V_{OH}$ and $V_{OL}$ are the typical output voltage drop that occur with the output load.

$V_{X} = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$ and $\leq 3.6V$

$V_{X} = V_{OL} + 0.1V_{CC}$ at $V_{CC} < 2.7V$ and $\geq 4.5V$

$V_{X} = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$ and $\leq 3.6V$

$V_{X} = V_{OH} - 0.1V_{CC}$ at $V_{CC} < 2.7V$ and $\geq 4.5V$

**NOTE:**

The shaded areas indicate when the input is permitted to change for predictable output performance.

**DEFINITIONS**

- $V_{OH} = V_{CC}$
- $V_{OL} = 0$ or $GND$
- $C_{L}$ = Load capacitance
- $R_{L}$ = Load resistance
- $R_{D}$ = Output resistor
- $V_{IH} = 1.5V$
- $V_{IL} = 0.5V$
- $V_{CC} = 5V$
- $V_{IN} = 0V$
- $V_{OUT} = 1V$

**TEST CIRCUIT**

**SWITCH POSITION**

<table>
<thead>
<tr>
<th>TEST</th>
<th>$R_{L}$ (kΩ)</th>
<th>$R_{D}$ (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1)</td>
<td>$50k$</td>
<td>$50k$</td>
</tr>
<tr>
<td>2)</td>
<td>$2.7V$</td>
<td>$V_{CC}$</td>
</tr>
<tr>
<td>3)</td>
<td>$2.7V$</td>
<td>$V_{CC}$</td>
</tr>
<tr>
<td>4)</td>
<td>$4.5V$</td>
<td>$V_{CC}$</td>
</tr>
</tbody>
</table>

**Figure 1.** Data input ($D_{o}$) to output ($Q_{o}$) propagation delays and the output transition times.

**Figure 2.** Latch enable input (LE) pulse width, the latch enable input to output ($Q_{o}$) propagation delays and the output transition times.

**Figure 3.** 3-State enable and disable times.

**Figure 4.** Data setup and hold times for the $D_{o}$ input to the LE input.

**Figure 5.** Load circuitry for switching times.
Octal D-type transparent latch (3-State)

DIP20: plastic dual-in-line package; 20 leads (300 mil)

SOT146-1

**Dimensions (inch dimensions are derived from the original mm dimensions):**

<table>
<thead>
<tr>
<th>UNIT</th>
<th>A max.</th>
<th>A1 min.</th>
<th>A2 max.</th>
<th>b</th>
<th>b1</th>
<th>c</th>
<th>d(1)</th>
<th>e</th>
<th>e1</th>
<th>L</th>
<th>M0</th>
<th>M1</th>
<th>w</th>
<th>Z(1) max.</th>
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<tbody>
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<td>4.2</td>
<td>0.51</td>
<td>3.2</td>
<td>1.73</td>
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<td>0.021</td>
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<td>0.30</td>
<td>0.14</td>
<td>0.32</td>
<td>0.38</td>
<td>0.01</td>
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</table>

Note:
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

**Outline Version**

<table>
<thead>
<tr>
<th>IEC</th>
<th>JEDEC</th>
<th>EIAJ</th>
</tr>
</thead>
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<tr>
<td>SOT146-1</td>
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</tbody>
</table>

**European Projection**

98-14-47
95-05-24

1998 Jun 10
**Octal D-type transparent latch (3-State)**

**74LV573**

**SO20:** plastic small outline package; 20 leads; body width 7.5 mm

**SOT163-1**

### Dimensions (inch dimensions are derived from the original mm dimensions)

<table>
<thead>
<tr>
<th>UNIT</th>
<th>A</th>
<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>bP</th>
<th>C</th>
<th>D(1)</th>
<th>E(1)</th>
<th>nE</th>
<th>L</th>
<th>Lp</th>
<th>Q</th>
<th>V</th>
<th>W</th>
<th>y</th>
<th>z(1)</th>
<th>z(2)</th>
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</thead>
<tbody>
<tr>
<td>mm</td>
<td>2.65</td>
<td>0.30</td>
<td>0.15</td>
<td>2.65</td>
<td>0.30</td>
<td>0.15</td>
<td>0.32</td>
<td>13.0</td>
<td>7.0</td>
<td>1.27</td>
<td>10.65</td>
<td>1.1</td>
<td>1.1</td>
<td>1.1</td>
<td>0.25</td>
<td>0.25</td>
<td>0.1</td>
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<tr>
<td>in.</td>
<td>0.10</td>
<td>0.10</td>
<td>0.10</td>
<td>0.10</td>
<td>0.10</td>
<td>0.10</td>
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<td>0.10</td>
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Note:
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

### OUTLINE VERSION

**IEC** | **JEDEC** | **EIAJ** | **EUROPEAN** | **ISSUE DATE**

| SOT163-1 | 072604 | MS-013AC | | 92-11-18 | 25-01-24 |

1998 Jun 10
Octal D-type transparent latch (3-State) 74LV573

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

DIMENSIONS (mm are the original dimensions)

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<th>UNIT</th>
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<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>bP</th>
<th>c</th>
<th>D(1)</th>
<th>E(1)</th>
<th>H6</th>
<th>L</th>
<th>Lp</th>
<th>O</th>
<th>V</th>
<th>v</th>
<th>y</th>
<th>z(1)</th>
<th>u</th>
</tr>
</thead>
<tbody>
<tr>
<td>mm</td>
<td>2.0</td>
<td>0.21</td>
<td>1.80</td>
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<td>0.38</td>
<td>0.20</td>
<td>7.4</td>
<td>3.4</td>
<td>0.05</td>
<td>7.9</td>
<td>1.25</td>
<td>1.03</td>
<td>0.9</td>
<td>0.2</td>
<td>0.13</td>
<td>0.1</td>
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<tr>
<td></td>
<td>0.05</td>
<td>1.65</td>
<td>0.25</td>
<td>0.56</td>
<td>0.25</td>
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<td>3.4</td>
<td>0.05</td>
<td>7.9</td>
<td>1.25</td>
<td>1.03</td>
<td>0.9</td>
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<td>0.13</td>
<td>0.1</td>
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</table>

Note:
1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION | IEC | JEDEC | EIAJ | EUROPEAN PROJECTION | ISSUE DATE
SOT339-1        | IEC | JEDEC | EIAJ |                        | 00-08-98 |

1993 Jun 10
Octal D-type transparent latch (3-State)  

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm  

SOT360-1

**DIMENSIONS (mm are the original dimensions)**

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<thead>
<tr>
<th>UNIT</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
<th>H</th>
<th>L</th>
<th>M</th>
<th>N</th>
<th>O</th>
<th>P</th>
<th>Q</th>
<th>R</th>
<th>S</th>
</tr>
</thead>
<tbody>
<tr>
<td>mm</td>
<td>2.0</td>
<td>2.0</td>
<td>1.5</td>
<td>1.0</td>
<td>0.8</td>
<td>0.4</td>
<td>0.4</td>
<td>0.3</td>
<td>0.6</td>
<td>0.6</td>
<td>0.5</td>
<td>0.3</td>
<td>0.2</td>
<td>0.2</td>
<td>0.1</td>
<td>0.05</td>
</tr>
</tbody>
</table>
| Notes  | 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.  
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.  

<table>
<thead>
<tr>
<th>OUTLINE VERSION</th>
<th>IEC</th>
<th>JEDEC</th>
<th>EIAJ</th>
<th>EUROPEAN PROJECTION</th>
<th>ISSUE DATE</th>
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<td>MO-153AC</td>
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<td>95-04-16, 95-02-04</td>
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</table>
# Octal D-type transparent latch (3-State)

**74LV573**

## DEFINITIONS

<table>
<thead>
<tr>
<th>Data Sheet Identification</th>
<th>Product Status</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Objective Specification</td>
<td>Formative or in Design</td>
<td>This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.</td>
</tr>
<tr>
<td>Preliminary Specification</td>
<td>Preproduction Product</td>
<td></td>
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<tr>
<td>Product Specification</td>
<td>Full Production</td>
<td></td>
</tr>
</tbody>
</table>

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Let’s make things better.
74HC/HCT138
3-to-8 line decoder/demultiplexer; inverting

Product specification
File under Integrated Circuits, IC06

September 1993
3-to-8 line decoder/demultiplexer; inverting

**FEATURES**
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- Output capability: standard
- \( f_{CC} \) category: MSI

**GENERAL DESCRIPTION**

The 74HC/HCT138 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

**QUICK REFERENCE DATA**

GND = 0 V; \( T_{amb} = 25 \ ^\circ \text{C} \); \( t_{f} = 6 \ \text{ns} \)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>TYPICAL</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>( C_L = 15 \ \text{pF} ); ( V_{CC} = 5 \ \text{V} )</td>
<td>HC</td>
<td>HCT</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 12 )</td>
<td>( 17 )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 14 )</td>
<td>( 19 )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 3.5 )</td>
<td>( 3.5 )</td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>notes 1 and 2</td>
<td>67</td>
<td>67</td>
</tr>
</tbody>
</table>

Notes
1. \( C_{PD} \) is used to determine the dynamic power dissipation \( (P_D \text{ in } \mu \text{W}) \):

\[
P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)
\]

\( f_i \) = input frequency in MHz

\( f_o \) = output frequency in MHz

\( \sum (C_L \times V_{CC}^2 \times f_o) \) = sum of outputs

\( C_L \) = output load capacitance in pF

\( V_{CC} \) = supply voltage in V

2. For HC the condition is \( V_I = GND \) to \( V_{CC} \)

For HCT the condition is \( V_I = GND \) to \( V_{CC} - 1.5 \ \text{V} \)

**ORDERING INFORMATION**

See "74HC/HCT/HCU/HCMOS Logic Package Information".

September 1993
3-to-8 line decoder/demultiplexer; inverting

74HC/HCT138

PIN DESCRIPTION

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>SYMBOL</th>
<th>NAME AND FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 2, 3</td>
<td>A₀ to A₂</td>
<td>address inputs</td>
</tr>
<tr>
<td>4, 5</td>
<td>E₁, E₂</td>
<td>enable inputs (active LOW)</td>
</tr>
<tr>
<td>6</td>
<td>E₃</td>
<td>enable input (active HIGH)</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>ground (0 V)</td>
</tr>
<tr>
<td>15, 14, 13, 12, 11, 10, 9, 7</td>
<td>V₀ to V₇</td>
<td>outputs (active LOW)</td>
</tr>
<tr>
<td>16</td>
<td>VCC</td>
<td>positive supply voltage</td>
</tr>
</tbody>
</table>

Fig. 1 Pin configuration.

Fig. 2 Logic symbol.

Fig. 3 IEC logic symbol.

Fig. 4 Functional diagram.

September 1993
### FUNCTION TABLE

<table>
<thead>
<tr>
<th>$\bar{E}_1$</th>
<th>$\bar{E}_2$</th>
<th>$E_3$</th>
<th>$A_0$</th>
<th>$A_1$</th>
<th>$A_2$</th>
<th>$\bar{Y}_0$</th>
<th>$\bar{Y}_1$</th>
<th>$\bar{Y}_2$</th>
<th>$\bar{Y}_3$</th>
<th>$\bar{Y}_4$</th>
<th>$\bar{Y}_5$</th>
<th>$\bar{Y}_6$</th>
<th>$\bar{Y}_7$</th>
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<td>X</td>
<td>X</td>
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<td>X</td>
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<td>H</td>
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<tr>
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<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
</tbody>
</table>

### Notes
1. H = HIGH voltage level
2. L = LOW voltage level
3. X = don’t care

### Diagram

Fig. 5 Logic diagram.

---

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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

Icc category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; \( t_i = t_f = 6 \) ns; \( C_L = 50 \) pF

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>( T_{amb} ) (°C)</th>
<th>UNIT</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
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<tr>
<td></td>
<td></td>
<td>( V_{cc} ) (V)</td>
<td>WAVEFORMS</td>
<td></td>
</tr>
<tr>
<td>( \text{typ.} )</td>
<td>( \text{min.} )</td>
<td>( \text{max.} )</td>
<td>( \text{min.} )</td>
<td>( \text{max.} )</td>
</tr>
<tr>
<td>( \text{min.} )</td>
<td>( \text{max.} )</td>
<td>( \text{min.} )</td>
<td>( \text{max.} )</td>
<td>( \text{max.} )</td>
</tr>
<tr>
<td>( t_{pHL}/ t_{pLH} ) propagation delay</td>
<td>( A_n ) to ( Y_n )</td>
<td>( +25 )</td>
<td>( -40 ) to ( +85 )</td>
<td>( -40 ) to ( +125 )</td>
</tr>
<tr>
<td>( 41 )</td>
<td>( 150 )</td>
<td>( 190 )</td>
<td>( 225 )</td>
<td>ns</td>
</tr>
<tr>
<td>( 15 )</td>
<td>( 30 )</td>
<td>( 38 )</td>
<td>( 45 )</td>
<td>( 38 )</td>
</tr>
<tr>
<td>( 12 )</td>
<td>( 26 )</td>
<td>( 33 )</td>
<td>6.0</td>
<td>Fig.6</td>
</tr>
<tr>
<td>( t_{pHL}/ t_{pLH} ) propagation delay</td>
<td>( E_3 ) to ( Y_n )</td>
<td>( +25 )</td>
<td>( -40 ) to ( +85 )</td>
<td>( -40 ) to ( +125 )</td>
</tr>
<tr>
<td>( 47 )</td>
<td>( 150 )</td>
<td>( 190 )</td>
<td>( 225 )</td>
<td>ns</td>
</tr>
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<td>( 17 )</td>
<td>( 30 )</td>
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<td>( 45 )</td>
<td>( 38 )</td>
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<tr>
<td>( 14 )</td>
<td>( 26 )</td>
<td>( 33 )</td>
<td>6.0</td>
<td>Fig.6</td>
</tr>
<tr>
<td>( t_{pHL}/ t_{pLH} ) propagation delay</td>
<td>( E_n ) to ( Y_n )</td>
<td>( +25 )</td>
<td>( -40 ) to ( +85 )</td>
<td>( -40 ) to ( +125 )</td>
</tr>
<tr>
<td>( 47 )</td>
<td>( 150 )</td>
<td>( 190 )</td>
<td>( 225 )</td>
<td>ns</td>
</tr>
<tr>
<td>( 17 )</td>
<td>( 30 )</td>
<td>( 38 )</td>
<td>( 45 )</td>
<td>( 38 )</td>
</tr>
<tr>
<td>( 14 )</td>
<td>( 26 )</td>
<td>( 33 )</td>
<td>6.0</td>
<td>Fig.7</td>
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<tr>
<td>( t_{THL}/ t_{TLH} ) output transition time</td>
<td></td>
<td>( +25 )</td>
<td>( -40 ) to ( +85 )</td>
<td>( -40 ) to ( +125 )</td>
</tr>
<tr>
<td>( 19 )</td>
<td>( 75 )</td>
<td>( 95 )</td>
<td>( 110 )</td>
<td>ns</td>
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<td>( 7 )</td>
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<td>( 19 )</td>
<td>( 22 )</td>
<td>( 19 )</td>
</tr>
<tr>
<td>( 6 )</td>
<td>( 13 )</td>
<td>( 16 )</td>
<td>4.5</td>
<td>Figs 6 and 7</td>
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</table>

September 1993
3-to-8 line decoder/demultiplexer; inverting 74HC/HCT138

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

iCC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔiCC) for a unit load of 1 is given in the family specifications. To determine ΔiCC per input, multiply this value by the unit load coefficient shown in the table below.

<table>
<thead>
<tr>
<th>INPUT</th>
<th>UNIT LOAD COEFFICIENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>A3</td>
<td>1.50</td>
</tr>
<tr>
<td>E3</td>
<td>1.25</td>
</tr>
<tr>
<td>E5</td>
<td>1.00</td>
</tr>
</tbody>
</table>

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; tP = tP = 6 ns; CL = 50 pF

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>TAMB (°C)</th>
<th>74HCT</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>+25</td>
<td>-40 to +85</td>
<td>-40 to +125</td>
</tr>
<tr>
<td></td>
<td></td>
<td>min.</td>
<td>typ.</td>
<td>max.</td>
</tr>
<tr>
<td>tPHL/ tPLH</td>
<td>propagation delay A3 to Yn</td>
<td>20</td>
<td>35</td>
<td>44</td>
</tr>
<tr>
<td>tPHL/ tPLH</td>
<td>propagation delay E3 to Yn</td>
<td>18</td>
<td>40</td>
<td>50</td>
</tr>
<tr>
<td>tPHL/ tPLH</td>
<td>propagation delay E3 to Yn</td>
<td>19</td>
<td>40</td>
<td>50</td>
</tr>
<tr>
<td>tTHL/ tTLH</td>
<td>output transition time</td>
<td>7</td>
<td>15</td>
<td>19</td>
</tr>
</tbody>
</table>
3-to-8 line decoder/demultiplexer; inverting 74HC/HCT138

AC WAVEFORMS

Fig 6  Waveforms showing the address input \((A_n)\) and enable input \((E_n)\) to output \((\overline{Y}_n)\) propagation delays and the output transition times.

Fig 7  Waveforms showing the enable input \((\overline{E}_n)\) to output \((\overline{Y}_n)\) propagation delays and the output transition times.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".
Features
- Fast Read Access Time - 150 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64 Bytes
- Fast Write Cycle Times
  - Page Write Cycle Time: 10 ms Maximum
  - 1 to 64-byte Page Write Operation
- Low Power Dissipation
  - 40 mA Active Current
  - 100 μA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling and Toggle Bit for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 100,000 Cycles
  - Data Retention: 10 Years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-wide Pinout
- Commercial and Industrial Temperature Ranges

Description
The AT28C64B is a high-performance electrically-erasable and programmable read only memory (EEPROM). Its 64K of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 220 mW. When the device is deselected, the CMOS standby current is less than 100 μA.

Pin Configurations

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0 - A12</td>
<td>Addresses</td>
</tr>
<tr>
<td>CE</td>
<td>Chip Enable</td>
</tr>
<tr>
<td>OE</td>
<td>Output Enable</td>
</tr>
<tr>
<td>WE</td>
<td>Write Enable</td>
</tr>
<tr>
<td>I/O0 - I/O7</td>
<td>Data Inputs/Outputs</td>
</tr>
<tr>
<td>NC</td>
<td>No Connect</td>
</tr>
<tr>
<td>DC</td>
<td>Don't Connect</td>
</tr>
</tbody>
</table>

Note: PLCC package pins 1 and 17 are DON'T CONNECT.
The AT28C64B is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA POLLING of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

Atmel’s AT28C64B has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.

**Block Diagram**

```
<table>
<thead>
<tr>
<th>ADDRESS INPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
</tr>
<tr>
<td>GND</td>
</tr>
<tr>
<td>OE</td>
</tr>
<tr>
<td>WE</td>
</tr>
<tr>
<td>CE</td>
</tr>
<tr>
<td>OE, WE and WE LOGIC</td>
</tr>
<tr>
<td>Y DECODER</td>
</tr>
<tr>
<td>X DECODER</td>
</tr>
<tr>
<td>DATA LATCH</td>
</tr>
<tr>
<td>DATA INPUTS/OUTPUTS</td>
</tr>
<tr>
<td>I/O0 - I/O7</td>
</tr>
</tbody>
</table>
```

<table>
<thead>
<tr>
<th>Absolute Maximum Ratings*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Under Bias</td>
</tr>
<tr>
<td>Storage Temperature</td>
</tr>
<tr>
<td>All Input Voltages (including NC Pins) with Respect to Ground</td>
</tr>
<tr>
<td>All Output Voltages with Respect to Ground</td>
</tr>
<tr>
<td>Voltage on OE and A9 with Respect to Ground</td>
</tr>
</tbody>
</table>

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Device Operation

READ: The AT28C64B is accessed like a Static RAM. When CE and OE are low and WE is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high-impedance state when either CE or OE is high. This dual line control gives designers flexibility in preventing bus contention in their systems.

BYTE WRITE: A low pulse on the WE or CE input with CE or WE low (respectively) and OE high initiates a write cycle. The address is latched on the falling edge of CE or WE, whichever occurs last. The data is latched by the first rising edge of CE or WE. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of \( t_{WP} \) a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28C64B allows 1 to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; after the first byte is written, it can then be followed by 1 to 63 additional bytes. Each successive byte must be loaded within 150 \( \mu \)s (t\( _{WLC} \)) of the previous byte. If the t\( _{WLC} \) limit is exceeded, the AT28C64B will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 to A12 inputs. For each WE high to low transition during the page write operation, A6 to A12 must be the same.

The A0 to A5 inputs specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

DATA POLLING: The AT28C64B features DATA Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O\( _{E} \). Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. DATA Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to DATA Polling, the AT28C64B provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O\( _{E} \) toggling between one and zero. Once the write has completed, I/O\( _{E} \) will stop toggling, and valid data will be read. Toggle bit reading may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28C64B in the following ways: (a) V\( _{CC} \) sense—if V\( _{CC} \) is below 3.8V (typical), the function is inhibited; (b) V\( _{CC} \) power-on delay—once V\( _{CC} \) has reached 3.8V, the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit—holding any one of OE low, CE high, or WE high inhibits write cycles; and (d) noise filter— pulses of less than 15 ns (typical) on the WE or OE inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C64B. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C64B is shipped from Atmel with SDP disabled.

SDP is enabled by the user issuing a series of three write commands in which three specific bytes of data are written to three specific addresses (refer to the Software Data Protection Algorithm diagram in this data sheet). After writing the 3-byte command sequence and waiting \( t_{WP} \), the entire AT28C64B will be protected against inadvertent writes. It should be noted that even after SDP is enabled, the user may still perform a byte or page write to the AT28C64B by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP remains active unless the disable command sequence is issued. Power transitions do not disable SDP, and SDP protects the AT28C64B during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not actually written into the device; their addresses may still be written with user data in either a byte or page write operation. After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device. However, for the duration of \( t_{WP} \), read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V \( \pm 0.5V \) and using address locations 1FCH to 1FFH, the additional bytes may be written to or read from in the same manner as the regular memory array.
DC and AC Operating Range

<table>
<thead>
<tr>
<th>Operating Temperature (Case)</th>
<th>AT28C64B-15</th>
<th>AT28C64B-20</th>
<th>AT28C64B-25</th>
</tr>
</thead>
<tbody>
<tr>
<td>Com.</td>
<td>0°C - 70°C</td>
<td>0°C - 70°C</td>
<td>0°C - 70°C</td>
</tr>
<tr>
<td>Ind.</td>
<td>-40°C - 85°C</td>
<td>-40°C - 85°C</td>
<td>-40°C - 85°C</td>
</tr>
<tr>
<td>V_CC Power Supply</td>
<td>5V ± 10%</td>
<td>5V ± 10%</td>
<td>5V ± 10%</td>
</tr>
</tbody>
</table>

Operating Modes

<table>
<thead>
<tr>
<th>Mode</th>
<th>CE</th>
<th>OE</th>
<th>WE</th>
<th>IO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read</td>
<td>V_IL</td>
<td>V_IL</td>
<td>V_H</td>
<td>D_OUT</td>
</tr>
<tr>
<td>Write[^2]</td>
<td>V_IL</td>
<td>V_H</td>
<td>V_H</td>
<td>D_IN</td>
</tr>
<tr>
<td>Standby/Write Inhibit</td>
<td>V_H</td>
<td>X[^1]</td>
<td>X</td>
<td>High Z</td>
</tr>
<tr>
<td>Write Inhibit</td>
<td>X</td>
<td>X</td>
<td>V_H</td>
<td>High Z</td>
</tr>
<tr>
<td>Write Inhibit</td>
<td>X</td>
<td>V_IL</td>
<td>X</td>
<td>High Z</td>
</tr>
<tr>
<td>Output Disable</td>
<td>X</td>
<td>V_H</td>
<td>X</td>
<td>High Z</td>
</tr>
<tr>
<td>Chip Erase</td>
<td>V_IL</td>
<td>V_H[^3]</td>
<td>V_IL</td>
<td>High Z</td>
</tr>
</tbody>
</table>

Notes:
1. X can be V_IL or V_H.
2. Refer to the AC Write Waveforms diagrams in this data sheet.
3. V_H = 12.0V ± 0.5V.

DC Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_L</td>
<td>Input Load Current</td>
<td>V_IN = 0V to V_CC + 1V</td>
<td>10</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>I_O</td>
<td>Output Leakage Current</td>
<td>V_IO = 0V to V_CC</td>
<td>10</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>I_SB1</td>
<td>V_CC Standby Current CMOS</td>
<td>CE = V_CC - 0.3V to V_CC + 1V</td>
<td>100</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>I_SB2</td>
<td>V_CC Standby Current TTL</td>
<td>CE = 2.0V to V_CC + 1V</td>
<td>2</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I_CC</td>
<td>V_CC Active Current</td>
<td>f = 5 MHz; I_OUT = 0 mA</td>
<td>40</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I_VH</td>
<td>Input High Voltage</td>
<td></td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I_OH</td>
<td>Output Low Voltage</td>
<td>I_OH = 2.1 mA</td>
<td>0.40</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I_CH</td>
<td>Output High Voltage</td>
<td>I_CH = -400 μA</td>
<td>2.4</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

AT28C64B
AC Read Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>AT28C64B-15</th>
<th>AT28C64B-20</th>
<th>AT28C64B-25</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACC</td>
<td>Address to Output Delay</td>
<td>Min 150</td>
<td>Min 200</td>
<td>Min 250</td>
</tr>
<tr>
<td>CE</td>
<td>CE to Output Delay</td>
<td>Max 150</td>
<td>Max 200</td>
<td>Max 250</td>
</tr>
<tr>
<td>OE(1)</td>
<td>OE to Output Delay</td>
<td>0</td>
<td>70</td>
<td>0</td>
</tr>
<tr>
<td>CE(1)</td>
<td>CE or OE to Output Float</td>
<td>0</td>
<td>50</td>
<td>0</td>
</tr>
<tr>
<td>ICH(1)(4)</td>
<td>Output Hold from OE, CE or Address, whichever occurred first</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

AC Read Waveforms(1)(2)(3)(4)

Notes:
1. CE may be delayed up to tACC - tCE after the address transition without impact on tACC.
2. OE may be delayed up to tCE - tOE after the falling edge of CE without impact on tCE or by tACC - tOE after an address change without impact on tACC.
3. tOE is specified from OE or CE whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Output Test Waveforms and Measurement Level

Input Capacitance

1 MHz, T = 25°C(1)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>CIN</td>
<td>4</td>
<td>6</td>
<td>pF</td>
<td>V_IN = 0V</td>
</tr>
<tr>
<td>COUT</td>
<td>8</td>
<td>12</td>
<td>pF</td>
<td>V_OUT = 0V</td>
</tr>
</tbody>
</table>

Note: 1. This parameter is characterized and is not 100% tested.
AC Write Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{AS}, t_{OES}</td>
<td>Address, OE Set-up Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{AH}</td>
<td>Address Hold Time</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{CS}</td>
<td>Chip Select Set-up Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{CH}</td>
<td>Chip Select Hold Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{WP}</td>
<td>Write Pulse Width (WE or CE)</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{DS}</td>
<td>Data Set-up Time</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{DH}, t_{OEH}</td>
<td>Data, OE Hold Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

AC Write Waveforms

WE Controlled

E Controlled

AT28C64B
### Page Mode Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tWC</td>
<td>Write Cycle Time</td>
<td>10</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>tWC</td>
<td>Write Cycle Time (28C64B SL184)</td>
<td>0</td>
<td>2</td>
<td>ms</td>
</tr>
<tr>
<td>tAS</td>
<td>Address Set-up Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tAH</td>
<td>Address Hold Time</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tDS</td>
<td>Data Set-up Time</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tDH</td>
<td>Data Hold Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tWP</td>
<td>Write Pulse Width</td>
<td>100</td>
<td>150</td>
<td>ns</td>
</tr>
</tbody>
</table>

### Page Mode Write Waveforms

#### Notes:
1. A6 through A12 must specify the same page address during each high to low transition of WEA (or CE).
2. OE must be high only when WE and CE are both low.

### Chip Erase Waveforms

- CE
- VIL
- VH
- OE
- VIH
- IS
- IH
- WE
- VIL

<table>
<thead>
<tr>
<th>tWC = tWP = 1 μsec (min.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>t = 10 msec (min.)</td>
</tr>
<tr>
<td>VIL = 12.0 ± 0.5V</td>
</tr>
</tbody>
</table>
Software Data Protection

Enable Algorithm\(^{(1)}\)

\[
\begin{align*}
\text{LOAD DATA AA} & \quad \text{TO ADDRESS 1555} \\
\text{LOAD DATA 55} & \quad \text{TO ADDRESS 0AAA} \\
\text{LOAD DATA A0} & \quad \text{TO ADDRESS 1555} \\
\text{LOAD DATA XX} & \quad \text{TO ANY ADDRESS}\(^{(2)}\) \\
\text{LOAD LAST BYTE} & \quad \text{TO LAST ADDRESS} \\
\end{align*}
\]

\(^{(2)}\): \text{Writtes Enabled}\(^{(2)}\)

Software Protected Write Cycle Waveforms\(^{(1)(2)}\)

\[\begin{array}{cccc}
\text{OE} & \text{CE} & \text{WE} & \text{DATA}
\end{array}\]

\[\begin{array}{cccc}
\text{IWP} & \text{IWP}\text{H} & \text{IBLC} & \text{IWP}\text{H}
\end{array}\]

\[\begin{array}{cccc}
\text{IWP} & \text{IWP}\text{H} & \text{IBLC} & \text{IWP}\text{H}
\end{array}\]

\[\begin{array}{cccc}
\text{IWP} & \text{IWP}\text{H} & \text{IBLC} & \text{IWP}\text{H}
\end{array}\]

Notes:
1. A6 through A12 must specify the same page address during each high to low transition of WE (or CE) after the software code has been entered.
2. OE must be high only when WE and CE are both low.
Data Polling Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tDH</td>
<td>Data Hold Time</td>
<td></td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tOEH</td>
<td>OE Hold Time</td>
<td></td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tOE</td>
<td>OE to Output Delay</td>
<td></td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tWR</td>
<td>Write Recovery Time</td>
<td></td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Notes:
1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

Data Polling Waveforms

Toggle Bit Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tDH</td>
<td>Data Hold Time</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tOEH</td>
<td>OE Hold Time</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tOE</td>
<td>OE to Output Delay</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tOEHP</td>
<td>OE High Pulse</td>
<td>150</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tWR</td>
<td>Write Recovery Time</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Notes:
1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

Toggle Bit Waveforms

Notes:
1. Toggling either OE or CE or both OE and CE will operate toggle bit.
2. Beginning and ending state of I/O6 may vary.
3. Any address location may be used but the address should not vary.
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE

NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY

AT28C64B
Ordering Information (1)

<table>
<thead>
<tr>
<th>( I_{cc} ) (mA) ( I_{cc} )</th>
<th>( I_{cc} ) (mA)</th>
<th>Ordering Code</th>
<th>Package</th>
<th>Operation Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>150</td>
<td>40</td>
<td>0.1</td>
<td>AT28C64B-15JC</td>
<td>32J</td>
</tr>
<tr>
<td>200</td>
<td>40</td>
<td>0.1</td>
<td>AT28C64B-20JC</td>
<td>32J</td>
</tr>
<tr>
<td>250</td>
<td>40</td>
<td>0.1</td>
<td>AT28C64B-25JC</td>
<td>32J</td>
</tr>
</tbody>
</table>

Note: 1. See Valid Part Numbers table below.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

<table>
<thead>
<tr>
<th>Device Numbers</th>
<th>Speed</th>
<th>Package and Temperature Combinations</th>
</tr>
</thead>
<tbody>
<tr>
<td>AT28C64B</td>
<td>15</td>
<td>JC, JI, PC, PI, SC, SI, TC, TI</td>
</tr>
<tr>
<td>AT28C64B</td>
<td>20</td>
<td>JC, JI, PC, PI, SC, SI, TC, TI</td>
</tr>
<tr>
<td>AT28C64B</td>
<td>25</td>
<td>JC, JI, PC, PI, SC, SI, TC, TI</td>
</tr>
<tr>
<td>AT28C64B</td>
<td>-</td>
<td>W</td>
</tr>
</tbody>
</table>

Die Products

Reference Section: Parallel EEPROM Die Products

Package Type

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>32J</td>
<td>32-lead, Plastic J-leaded Chip Carrier (PLCC)</td>
</tr>
<tr>
<td>28P6</td>
<td>28-lead, 0.600&quot; Wide, Plastic Dual Inline Package (PDIP)</td>
</tr>
<tr>
<td>28S</td>
<td>28-lead, 0.300&quot; Wide, Plastic Gull Wing Small Outline (SOIC)</td>
</tr>
<tr>
<td>28T</td>
<td>28-lead, Plastic Thin Small Outline Package (TSOP)</td>
</tr>
<tr>
<td>W</td>
<td>Die</td>
</tr>
</tbody>
</table>
Packaging Information

32J, 32-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-016 AE

28P6, 28-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AB

28S, 28-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)

28T, 28-lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*

AT28C648
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