LAMPIRAN
LAMPIRAN A

Gambar Alat
#include<stdio.h>
#include<regx51.h>

sbit DQ = P0_4;
sfr lda = 0x90;
sbit rs = P3_0;
sbit en = P3_1;
unsigned int suhu;
char a;
int b,c,d,e,f;

void delay(int useconds)
{
    int s;
    for (s=0; s<useconds; s++)
{
    unsigned char ow_reset (void)
    { unsigned char presence;
        DQ = 0; //pull DQ line low
        delay(29); // leave it low for 4801s
        DQ = 1; // allow line to return high
        delay(3); // wait for presence
        presence = DQ; // get presence signal
        delay(25); // wait for end of timeslot
        return(presence); // presence signal returned
    } // 0=presence, 1 = no part
    unsigned char read_bit(void)
    { unsigned char i;
        DQ = 0; // pull DQ low to start timeslot
        DQ = 1; // then return high
        for (i=0; i<3; i++) // delay 151s from start of timeslot
        { delay(5); // return value of DQ line
        }
    }
    void write_bit(char bitval)
    {
        DQ = 0; // pull DQ low to start timeslot
        if(bitval==1) DQ =1; // return DQ high if write 1
        delay(5); // hold value for remainder of timeslot
        DQ = 1;
    }
    unsigned char read_byte(void)
    { unsigned char i;
        unsigned char value = 0;
        for (i=0; i<8; i++)
        { if(read_bit()) value|=0x01<<i; // reads byte in, one bit at a time and then
          // shifts it left
          delay(6); // wait for rest of timeslot
        return(value);
        }
    }
    void write_byte(char val)
    { unsigned char i;
        unsigned char temp;
        for (i=0; i<8; i++) // writes byte, one bit at a time
        { temp = val>>i; // shifts val right 'i' spaces
            temp &= 0x01; // copy that bit to temp
            write_bit(temp); // write bit in temp into
        }
delay(5);
void MSDelay(unsigned int itime)
{
    unsigned int i, j;
    for(i=0;i<itime;i++)
        for(j=0;j<1275;j++);
}
void lcddata(unsigned char value)
{ldata = value;
    rs = 1;
    en = 1;
    MSDelay(20);
    en = 0;
    return;
}
void tampilkan_ke_lcd(char *tulisan)
{
    char hitung_tulisan;
    while (hitung_tulisan=*tulisan++)
    {
        lcddata(hitung_tulisan);
    }
}
unsigned char Read_Current (void)
{
    int lsb, msb, temp, nilai;
    float Current; //This value may be declared globally
    if(ow_reset()==0) //If a presence is detected, continue to read
    {
        write_byte(0xCC); // Skip Net Address Command
        write_byte(0x69); // Read Registers Command
        msb = read_byte(); // Read msb
        write_byte(0x0E); // Read Current Register Address
        msb = read_byte() & 0xF8; // Read msb
        lsb = read_byte() & 0xFB; // Read lsb and mask off lower 3 bits
        suhu = 256*msb + lsb;
        suhu = suhu/4;
        nilai = suhu*(-0.2215)+3698.8;
        if (nilai >100 & nilai < 200)
            nilai=nilai-20;
        if (nilai < 100)
            nilai=nilai-40;
        lcddata(nilai/100 %10 + 0x30);
        lcddata(nilai/10 %10 + 0x30);
        lcddata(nilai %10 + 0x30);
        lcddata(0xDF);
        lcddata('C');
    }
    return(O); //Return 0 if no error
} return(1); //Return 1 if no presence detected
void motor_putar()
{P3_7 = 1;
}
void motor_aduk()
{P2_4 = 1;
P2_5 = 1;
}
void motor_wajan()
{P2_2 = 1; // on
P2_3 = 1; // back
}
void pemanas()
{P2_6 = 1;
void pemanas2()
{
P2_6 = 0;
P2_7 = 0;
}

void posisi()
{
    satu:
    if (P0_5 == 0)
        P2_4 = 0;
    else
goto satu;
    dua:
    MSDe1ay(1000);
    if (P0_6 == 0)
        P2_5 = 0;
    else
goto dua;
}

void lcdcmd(unsigned char value)
{
    ldata = value;
    rs = 0;
    en = 1;
    MSDelay(20);
    en = 0;
    return;
}

void wajan_naik()
{
lcdcmd(0x01);
tampilkan_ke_lcd("penirisan");
MSDelay(1000);
P2_1 = 1;        //motor atas
MSDelay(1000);
P2_1 = 0;
MSDelay(200);
P2_1 = 1;
MSDelay(1000);
P2_1 = 0;
MSDelay(1000);
        //motor wajan
P2_3 = 1;
while(P0_3 != 0);
P2_2 = 1;
MSDelay(50);
P2 = 0x00;
}

void wajan_turun()
{
P2 = 0x00;
MSDelay(1000);
P2 = 0x00;
MSDelay(2000);        //motor wajan
P2_1 = 1;
P2_0 = 1;
MSDelay(1000);
P2 = 0x00;
MSDelay(1000);
P2 = 0x03;
MSDelay(2000);        //motor atas
P2 = 0x00;
}

void init_lcd()
{
lcdcmd(0x38);
MSDelay(20);
lcdcmd(0x01);
MSDelay(20);
lcdcmd(0x06);
MSDelay(20);
lcdcmd(0x01);
}
void mulai()
{
  pemanas1();
a = 0;
  while(P0_3 != 0) {
    if (P0_3 !=0)
      MSDelay(500);
P3_2 = 1;
    if (P0_3 !=0)
      MSDelay(500);
a++;
    if (a>10)
      break;
  }

  if (a>=10)
    {P3_2 = 0;
     while (P0_3 != 0)
     {
      if (P0_3 !=0)
        MSDelay(1000);
      if (suhu < 15597)
        pemanas2();
      else
        pemanas1();
    }
  }
lcdcmd(0x01);
pemanas1();
P3_2 = 1;
lcdcmd(0x01);
tampilkan_ke_lcd("tunggu suhu");
lcdcmd(0xC4);
read_current();
while(suhu > 14687)
  {lcdcmd(0xC4);
   read_current();
   MSDelay(1000);
  }
}
void daging()
{
  lcdcmd(0x01);
tampilkan_ke_lcd("masukkan");
lcdcmd(0xC0);
tampilkan_ke_lcd("daging + bumbu");
a = 0;
  while(P0_3 != 0) {
    if (P0_3 !=0)
      MSDelay(500);
P3_2 = 1;
    if (P0_3 !=0)
      MSDelay(1000);
a++;
    if (a>10)
      break;
  }

  if (a>=10)
    {P3_2 = 0;
     while (P0_3 != 0); 
    }
P3_2 = 1;
lcdcmd(0x01);
}
void daging_bumbu() 
{
lcdcmd(0x01);
tampilkan_ke_lcd("masukkan");
lcdcmd(0x0C0);
tampilkan_ke_lcd("daging berbumbu");
MSDelay(1000);
a = 0;
while(P0_3 != 0)
{
P3_2 = 0;
if (P0_3 != 0)
MSDelay(500);
P3_2 = 1;
if (P0_3 != 0)
MSDelay(1000);
++a;
if (a>10)
break;
}
if (a>=10)
{
P3_2 = 0;
while (P0_3 != 0);
}
P3_2 = 1;
lcdcmd(0x01);
}
void waktu()
{
c = 0;
tampilkan_ke_lcd("sisa");
if (b != f)
motor_aduk();
while (b != 0)
{
if (b == d)
posisi();
if (b == e)
motor_aduk();
lcdcmd(0x85);
lcddata(b/10 %10 + 0x30);
lcddata(b %10 + 0x30);
tampilkan_ke_lcd(" menit");
c = 0;
while (c <= 173)
{
lcdcmd(0xc4);
read_current();
MSDelay(10);
++c;
}
b--;
}
void waktu_kering()
{
c = 0;
while (b != 0)
{
c = 0;
while (c <= 233)
{
MSDelay(100);
++c;
}
b--;
}
}
void main(void)
{
P3 = 0x04;
P1 = 0x00;
P2 = 0x00;
P0 = 0xff;
init_lcd();
lcdcmd(0x01);
lcdcmd(0x84);
tampilkan_ke_lcd("wibisono");
lcdcmd(0xC3);
tampilkan_ke_lcd("Sl03003007");
while(PO_3 != 0);
lcdcmd(0x01);
tampilkan_ke_lcd("tombol 1 = 100g");
lcdcmd(0x00);
tampilkan_ke_lcd("tombol 2 = 250g");
while(1)
{
  if (PO_0 == 0)
  (lcdcmd(0x01);
tampilkan_ke_lcd("masukkan minyak");
lcdcmd(0x00);
tampilkan_ke_lcd("2 sendok makan");
mulai();
daging();
b=10;
d=5;
e=25;
f=25;
waktu();
pemanas2();
wajan_naiik();
MSDelay(500);
wajan_turun();
motor_putar();
b=3;
waktu_kering();
P3_7 = 0;//goreng
pemanas1();
lcdcmd(0x01);
tampilkan_ke_lcd("masukkan minyak");
lcdcmd(0x00);
tampilkan_ke_lcd("200 ml");
mulai();
daging_bumbu();
b=20;
d=5;
e=15;
f=20;
waktu();
pemanas2();
wajan_naiik();
MSDelay(500);
wajan_turun();
motor_putar();
b=3;
waktu_kering();
P3_7 = 0;
lcdcmd(0x01);
tampilkan_ke_lcd("selesai!!!!!");
while(P0_3 != 0)
{
P3_2 = 0;
if (P0_3 !=0)
MSDelay(500);
P3_2 = 1;
if (P0_3 !=0)
MSDelay(1000);
}
lcdcmd(0x01);
lcdcmd(0x00);
tampilkan_ke_lcd("tombol 1 = 100g");
lcdcmd(0x00);
tampilkan_ke_lcd("tombol 2 = 250g");
}
else
if (PO_1 == 0)
(lcdcmd(0x01);
tampilkan_ke_lcd("masukkan minyak");
lcdcmd(0x00);
tampilkan_ke_lcd("2 sendok makan");
mulai();
daging();
b=10;
d=5;
e=25;
f=15;
waktu();
pemanas2();
wajan_naik();
MSDelay(500);
wajan_turun();
motor_putar();
b=3;
waktu_kering();
P3_7 = 0;//goreng
pemanas1();
lccmd(0x01);
tampilkan_ke_lcd("masukkan minyak");
lccmd(0xc0);
tampilkan_ke_lcd("300 ml");
mulai();
daging_bumbu();
b=30;
d=10;
e=20;
f=30;
waktu();
pemanas2();
MSDelay(500);
wajan_turun();
motor_putar();
b=3;
waktu_kering();
P3_7 = 0;
lccmd(0x01);
tampilkan_ke_lcd("selesai!!!!");
while(P0_3 != 0)
{
P3_2 = 0;
if (P0_3 !=0)
MSDelay(500);
P3_2 = 1;
if (P0_3 !=0)
MSDelay(1000);
}
lccmd(0x01);
lccmd(0x80);
tampilkan_ke_lcd("tombol 1 = 100g");
lccmd(0xc0);
tampilkan_ke_lcd("tombol 2 = 250g");
//motor_aduk();
}
LAMPIRAN D

DATA PENGAMBILAN SAMPEL

Tabel Sampel

<table>
<thead>
<tr>
<th>DS2760</th>
<th>Multimeter UNI-T Type UT720B</th>
<th>Hasil dari persamaan Y</th>
<th>Selisih</th>
</tr>
</thead>
<tbody>
<tr>
<td>16365</td>
<td>30</td>
<td>71,9525</td>
<td>41,9525</td>
</tr>
<tr>
<td>16347</td>
<td>40</td>
<td>75,9395</td>
<td>35,9395</td>
</tr>
<tr>
<td>16331</td>
<td>50</td>
<td>79,4835</td>
<td>29,4835</td>
</tr>
<tr>
<td>16313</td>
<td>60</td>
<td>83,4705</td>
<td>23,4705</td>
</tr>
<tr>
<td>16295</td>
<td>70</td>
<td>87,4575</td>
<td>17,4575</td>
</tr>
<tr>
<td>16273</td>
<td>80</td>
<td>92,3305</td>
<td>12,3305</td>
</tr>
<tr>
<td>16249</td>
<td>90</td>
<td>97,6465</td>
<td>7,6465</td>
</tr>
<tr>
<td>16225</td>
<td>100</td>
<td>102,9625</td>
<td>2,9625</td>
</tr>
<tr>
<td>16195</td>
<td>110</td>
<td>109,6075</td>
<td>0,9625</td>
</tr>
<tr>
<td>16159</td>
<td>120</td>
<td>117,5815</td>
<td>-2,4185</td>
</tr>
<tr>
<td>16129</td>
<td>130</td>
<td>124,2265</td>
<td>-5,7735</td>
</tr>
<tr>
<td>16091</td>
<td>140</td>
<td>132,6435</td>
<td>-7,3565</td>
</tr>
<tr>
<td>16051</td>
<td>150</td>
<td>141,5035</td>
<td>-8,4965</td>
</tr>
<tr>
<td>16013</td>
<td>160</td>
<td>149,9205</td>
<td>-10,0795</td>
</tr>
<tr>
<td>15979</td>
<td>170</td>
<td>157,4515</td>
<td>-12,5485</td>
</tr>
<tr>
<td>15933</td>
<td>180</td>
<td>167,6405</td>
<td>-12,3595</td>
</tr>
<tr>
<td>15891</td>
<td>190</td>
<td>176,9435</td>
<td>-13,0565</td>
</tr>
<tr>
<td>15849</td>
<td>200</td>
<td>186,2465</td>
<td>-13,7535</td>
</tr>
<tr>
<td>15803</td>
<td>210</td>
<td>196,4355</td>
<td>-13,5645</td>
</tr>
<tr>
<td>15775</td>
<td>220</td>
<td>202,6375</td>
<td>-17,3625</td>
</tr>
<tr>
<td>15715</td>
<td>230</td>
<td>215,9275</td>
<td>-14,0725</td>
</tr>
<tr>
<td>15667</td>
<td>240</td>
<td>226,5595</td>
<td>-13,4405</td>
</tr>
<tr>
<td>15613</td>
<td>250</td>
<td>238,5205</td>
<td>-11,4795</td>
</tr>
<tr>
<td>15567</td>
<td>260</td>
<td>248,7095</td>
<td>-11,2905</td>
</tr>
<tr>
<td>15523</td>
<td>270</td>
<td>258,4555</td>
<td>-11,5445</td>
</tr>
<tr>
<td>15475</td>
<td>280</td>
<td>269,0875</td>
<td>-10,9125</td>
</tr>
<tr>
<td>15423</td>
<td>290</td>
<td>280,6055</td>
<td>-9,3945</td>
</tr>
<tr>
<td>15377</td>
<td>300</td>
<td>290,7945</td>
<td>-9,2055</td>
</tr>
<tr>
<td>15327</td>
<td>310</td>
<td>301,8695</td>
<td>-8,1305</td>
</tr>
<tr>
<td>15265</td>
<td>320</td>
<td>315,6025</td>
<td>-4,3975</td>
</tr>
<tr>
<td>15225</td>
<td>330</td>
<td>324,4625</td>
<td>-5,5375</td>
</tr>
<tr>
<td>15181</td>
<td>340</td>
<td>334,2085</td>
<td>-5,7915</td>
</tr>
<tr>
<td>15129</td>
<td>350</td>
<td>345,7265</td>
<td>-4,2735</td>
</tr>
<tr>
<td>15091</td>
<td>360</td>
<td>354,1435</td>
<td>-5,8565</td>
</tr>
<tr>
<td>15065</td>
<td>370</td>
<td>359,9025</td>
<td>-10,0975</td>
</tr>
<tr>
<td>14981</td>
<td>380</td>
<td>378,5085</td>
<td>-1,4915</td>
</tr>
<tr>
<td>14901</td>
<td>390</td>
<td>396,2285</td>
<td>6,2285</td>
</tr>
<tr>
<td>14861</td>
<td>400</td>
<td>405,0885</td>
<td>5,0885</td>
</tr>
<tr>
<td>14811</td>
<td>410</td>
<td>416,1635</td>
<td>6,1635</td>
</tr>
<tr>
<td>14761</td>
<td>420</td>
<td>427,2385</td>
<td>7,2385</td>
</tr>
</tbody>
</table>
### Tabel Sampel (lanjutan)

<table>
<thead>
<tr>
<th>DS2760</th>
<th>Multimeter UNI-T Type UT720B</th>
<th>Hasil dari persamaan ( Y )</th>
<th>Selisih</th>
</tr>
</thead>
<tbody>
<tr>
<td>14711</td>
<td>430</td>
<td>438,3135</td>
<td>8,3135</td>
</tr>
<tr>
<td>14657</td>
<td>440</td>
<td>450,2745</td>
<td>10,2745</td>
</tr>
<tr>
<td>14597</td>
<td>450</td>
<td>463,5645</td>
<td>13,5645</td>
</tr>
<tr>
<td>14561</td>
<td>460</td>
<td>471,5385</td>
<td>11,5385</td>
</tr>
<tr>
<td>14509</td>
<td>470</td>
<td>483,0565</td>
<td>13,0565</td>
</tr>
<tr>
<td>14481</td>
<td>480</td>
<td>493,6885</td>
<td>13,6885</td>
</tr>
<tr>
<td>14403</td>
<td>490</td>
<td>506,5255</td>
<td>16,5255</td>
</tr>
</tbody>
</table>

### Grafik dari pengambilan sampel

\[
y = -0.2215x + 3696.8 \\
R^2 = 0.9895
\]
Nama : Wibisono
NRP : 5103003007
Tempat/ Tgl. Lahir : Surabaya / 1 April 1982
Agama : Katholik
Alamat Rumah : Jl. Tarmidi 52

Samarinda – Kalimantan Timur

Riwayat Pendidikan :

• Tahun 1988, Lulus TK Kristus Radja Surabaya.

• Tahun 1996, Lulus SD Swasta Megawati Surabaya.

• Tahun 1999, Lulus SLTP Katholik Santa Agnes Surabaya.

• Tahun 2003, Lulus SMK Katholik St. Louis Surabaya.

• Tahun 2003 hingga buku ini ditulis, tercatat sebagai mahasiswa di Jurusan Teknik Elektro, Fakultas Teknik, Universitas Katolik Widya Mandala, Surabaya.
TURES
+ safety circuit
Overvoltage protection
Overcurrent/short circuit protection
Undervoltage protection
≥ Volt Battery Recovery Charge
available in two configurations:
Internal 25mΩ sense resistor
External user-selectable sense resistor
Current measurement
12-bit bidirectional measurement
Internal sense resistor configuration: 0.625mA LSB and ±1.9A dynamic range
External sense resistor configuration: 15.625μV LSB and ±64mV dynamic range
Current accumulation
Internal sense resistor: 0.25mAhr LSB
External sense resistor: 6.25μVhr LSB
Voltage measurement with 4.88mV resolution
Temperature measurement using integrated
sensor with 0.125°C resolution
System power management and control feature
2 bytes of lockable EEPROM
6 bytes of general purpose SRAM
texas 1-Wire® interface with unique 64-bit device address
Low power consumption:
Active current: 90μA max
Sleep current: 2μA max

PIN ASSIGNMENT

<table>
<thead>
<tr>
<th>PIN DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>CC - Charge control output</td>
</tr>
<tr>
<td>DC - Discharge control output</td>
</tr>
<tr>
<td>DQ - Data input/output</td>
</tr>
<tr>
<td>PIO - Programmable I/O pin</td>
</tr>
<tr>
<td>PLS - Battery pack positive terminal input</td>
</tr>
<tr>
<td>PS - Power switch sense input</td>
</tr>
<tr>
<td>VIN - Voltage sense input</td>
</tr>
<tr>
<td>VDD - Power supply input (2.5V to 5.5V)</td>
</tr>
<tr>
<td>VSS - Device ground</td>
</tr>
<tr>
<td>SNS - Sense resistor connection</td>
</tr>
<tr>
<td>IS1 - Current sense input</td>
</tr>
<tr>
<td>IS2 - Current sense input</td>
</tr>
<tr>
<td>SNS Probe - Do not connect</td>
</tr>
<tr>
<td>VSS Probe - Do not connect</td>
</tr>
</tbody>
</table>

is a registered trademark of Dallas Semiconductor.
SERING INFORMATION

<table>
<thead>
<tr>
<th>Part</th>
<th>Marking</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>50AE+</td>
<td>DS2760A</td>
<td>TSSOP, External Sense Resistor, 4.275V Vov, Lead-Free</td>
</tr>
<tr>
<td>50BE+</td>
<td>DS2760B</td>
<td>TSSOP, External Sense Resistor, 4.35V Vov, Lead-Free</td>
</tr>
<tr>
<td>50AE+T&amp;R</td>
<td>DS2760A</td>
<td>DS2760AE+ on Tape &amp; Reel, Lead-Free</td>
</tr>
<tr>
<td>50BE+T&amp;R</td>
<td>DS2760B</td>
<td>DS2760BE+ on Tape &amp; Reel, Lead-Free</td>
</tr>
<tr>
<td>60AE+025</td>
<td>2760A25</td>
<td>TSSOP, 25mΩ Sense Resistor, 4.275V Vov, Lead-Free</td>
</tr>
<tr>
<td>60BE+025</td>
<td>2760B25</td>
<td>TSSOP, 25mΩ Sense Resistor, 4.35V Vov, Lead-Free</td>
</tr>
<tr>
<td>60AE+025/T&amp;R</td>
<td>2760A25</td>
<td>DS2760AE+025 in Tape &amp; Reel, Lead-Free</td>
</tr>
<tr>
<td>60BE+025/T&amp;R</td>
<td>2760B25</td>
<td>DS2760BE+025 in Tape &amp; Reel, Lead-Free</td>
</tr>
<tr>
<td>60AX</td>
<td>DS2760A</td>
<td>Flipchip, External Sense Resistor, Tape &amp; Reel, 4.275V Vov</td>
</tr>
<tr>
<td>60BX</td>
<td>DS2760B</td>
<td>Flipchip, External Sense Resistor, Tape &amp; Reel, 4.35V Vov</td>
</tr>
<tr>
<td>60AX-025</td>
<td>DS2760AR</td>
<td>Flipchip, 25mΩ Sense Resistor, Tape &amp; Reel, 4.35V Vov</td>
</tr>
<tr>
<td>60BX-025</td>
<td>DS2760BR</td>
<td>Flipchip, 25mΩ Sense Resistor, Tape &amp; Reel, 4.35V Vov</td>
</tr>
<tr>
<td>60AE</td>
<td>DS2760A</td>
<td>TSSOP, External Sense Resistor, 4.275V Vov</td>
</tr>
<tr>
<td>60BE</td>
<td>DS2760B</td>
<td>TSSOP, External Sense Resistor, 4.35V Vov</td>
</tr>
<tr>
<td>60AE/T&amp;R</td>
<td>DS2760A</td>
<td>DS2760AE on Tape &amp; Reel</td>
</tr>
<tr>
<td>60BE/T&amp;R</td>
<td>DS2760B</td>
<td>DS2760BE on Tape &amp; Reel</td>
</tr>
<tr>
<td>60AE-025</td>
<td>2760A25</td>
<td>TSSOP, 25mΩ Sense Resistor, 4.275V Vov</td>
</tr>
<tr>
<td>60BE-025</td>
<td>2760B25</td>
<td>TSSOP, 25mΩ Sense Resistor, 4.35V Vov</td>
</tr>
<tr>
<td>60AE-025/T&amp;R</td>
<td>2760A25</td>
<td>DS2760AE-025 in Tape &amp; Reel</td>
</tr>
<tr>
<td>60BE-025/T&amp;R</td>
<td>2760B25</td>
<td>DS2760BE-025 in Tape &amp; Reel</td>
</tr>
</tbody>
</table>

DESCRIPTION

DS2760 High-Precision Li+ Battery Monitor is a data acquisition, information storage, and safety device tailored for cost-sensitive battery pack applications. This low-power device integrates temperature, voltage, and current measurement, nonvolatile data storage, and Li+ protection into a small footprint of either a TSSOP package or flip chip. The DS2760 is a key component in applications including remaining capacity estimation, safety monitoring, and battery-specific data storage.

Its 1-Wire interface, the DS2760 gives the host system read/write access to status and control registers, instrumentation registers, and general purpose data storage. Each device has a unique factory-rammed 64-bit net address which allows it to be individually addressed by the host system, permitting multi-battery operation.

DS2760 is capable of performing temperature, voltage and current measurement to a resolution sufficient to support process monitoring applications such as battery charge control, remaining capacity estimation, and safety monitoring. Temperature is measured using an on-chip sensor, eliminating the need for an external thermistor. Bidirectional current measurement and accumulation are accomplished using an internal 25mΩ sense resistor or an external device. The DS2760 also features a programmable I²C bus that allows the host system to sense and control other electronics in the pack, including switches, motors, speakers and LEDs.

Types of memory are provided on the DS2760 for battery information storage: EEPROM, lockable ROM and SRAM. EEPROM memory saves important battery data in true nonvolatile memory that is unaffected by severe battery depletion, accidental shorts or ESD events. Lockable EEPROM becomes locked when locked to provide additional security for unchanging battery data. SRAM provides temporary storage for temporary data.
Figure 1

1-WIRE INTERFACE AND ADDRESS

THERMAL SENSE

VOLTAGE REFERENCE

MUX

ADC

REGISTERS AND USER MEMORY

LOCKABLE EEPROM

SRAM

TEMPERATURE

VOLTAGE

CURRENT

ACCUM. CURRENT

STATUS / CONTROL

LI+ PROTECTION

TIMEBASE

PIO

CC

DC

internal sense resistor configuration only

SNS

25mΩ

IS2

IS1

chip ground

VSS
### Table 1

<table>
<thead>
<tr>
<th>PIN</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td><strong>Charge Protection Control Output.</strong> Controls an external p-channel high-side charge protection FET.</td>
</tr>
<tr>
<td>C2</td>
<td><strong>Discharge Protection Control Output.</strong> Controls an external p-channel high-side discharge protection FET.</td>
</tr>
<tr>
<td>B4</td>
<td><strong>Data Input/Out.</strong> 1-Wire data line. Open-drain output driver. Connect this pin to the DATA terminal of the battery pack. Pin has an internal 1μA pull-down for sensing disconnection.</td>
</tr>
<tr>
<td>E2</td>
<td><strong>Programmable I/O Pin.</strong> Used to control and monitor user-defined external circuitry. Open drain to VSS.</td>
</tr>
<tr>
<td>B1</td>
<td><strong>Battery Pack Positive Terminal Input.</strong> The device monitors the state of the battery pack’s positive terminal through this pin in order to detect events such as the attachment of a charger or the removal of a short circuit. Additionally, a charge path to recover a deeply depleted cell is provided from PLS to VDD.</td>
</tr>
<tr>
<td>E4</td>
<td><strong>Power Switch Sense Input.</strong> The device wakes up from Sleep Mode when it senses the closure of a switch to VSS on this pin. Pin has an internal 1μA pull-up to VDD.</td>
</tr>
<tr>
<td>D1</td>
<td><strong>Voltage Sense Input.</strong> The voltage of the Li+ cell is monitored via this input pin. This pin has a weak pullup to VDD.</td>
</tr>
<tr>
<td>E1</td>
<td><strong>Power Supply Input.</strong> Connect to the positive terminal of the Li+ cell through a decoupling network.</td>
</tr>
<tr>
<td>F3</td>
<td><strong>Device Ground.</strong> Connect directly to the negative terminal of the Li+ cell. For the external sense resistor configuration, connect the sense resistor between VSS and SNS.</td>
</tr>
<tr>
<td>A3</td>
<td><strong>Sense Resistor Connection.</strong> Connect to the negative terminal of the battery pack. In the internal sense resistor configuration, the sense resistor is connected between VSS and SNS.</td>
</tr>
<tr>
<td>D4</td>
<td><strong>Current Sense Input.</strong> This pin is internally connected to VSS through a 4.7kΩ resistor. Connect a 0.1μF capacitor between IS1 and IS2 to complete a low-pass input filter.</td>
</tr>
<tr>
<td>C4</td>
<td><strong>Current Sense Input.</strong> This pin is internally connected to SNS through a 4.7kΩ resistor.</td>
</tr>
<tr>
<td>A2</td>
<td>Do Not Connect.</td>
</tr>
<tr>
<td>C2</td>
<td>Do Not Connect.</td>
</tr>
</tbody>
</table>

![Mechanical drawing for the 16-pin TSSOP and DS2760 flip-chip package can be found at:](/pdfserv.maxim-ic.com/arpdf/Packages/16tssop.pdf)

![Mechanical drawing for the 16-pin TSSOP and DS2760 flip-chip package can be found at:](/pdfserv.maxim-ic.com/arpdf/Packages/chips/2760x.pdf)
SENS is present for external sense resistor configurations only
SENSINT is present for internal sense resistor configurations only
ER MODES

S2760 has two power modes: Active and Sleep. While in Active Mode, the DS2760 continually measures current, voltage and temperature to provide data to the host system and to support current regulation and Li+ safety monitoring. In Sleep Mode, the DS2760 ceases these activities. The device enters Sleep Mode when any of the following conditions occur:

- PMOD bit in the Status Register has been set to 1 and the DQ line is low for longer than 1 second (pack disconnection)
- Voltage on VIN drops below undervoltage threshold \( V_{UV} \) for \( t_{UVD} \) (cell depletion)
- Pack is disabled through the issuance of a SWAP command (SWEN bit = 1)

S2760 returns to Active Mode when any of the following occurs:

- PMOD bit has been set to 1 and the SWEN bit is set to 0 and the DQ line is pulled high (pack connection)
- PS pin is pulled low (power switch)
- Voltage on PLS becomes greater than the voltage on VIN (charger connection) with the SWEN bit = 0
- Pack is enabled through the issuance of a SWAP command (SWEN bit = 1)

S2760 defaults to Sleep Mode when power is first applied.

PROTECTION CIRCUITRY

In Active Mode, the DS2760 constantly monitors cell voltage and current to protect the battery from large overvoltage, overdischarge (undervoltage) and excessive charge and discharge currents (short circuit). Conditions and DS2760 responses are described in the sections below and summarized in Table 2 and Figure 3.

PROTECTION CONDITIONS AND DS2760 RESPONSES

<table>
<thead>
<tr>
<th>Condition</th>
<th>Activation</th>
<th>Release</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage</td>
<td>VIN &gt; ( V_{OV} )</td>
<td>( t_{OVD} )</td>
</tr>
<tr>
<td>Overvoltage</td>
<td>VIN &lt; ( V_{UV} )</td>
<td>( t_{UVD} )</td>
</tr>
<tr>
<td>Current, Charge</td>
<td>( V_{IS} &gt; V_{OC} )</td>
<td>( t_{OCD} )</td>
</tr>
<tr>
<td>Current, Discharge</td>
<td>( V_{IS} &lt; -V_{OC} )</td>
<td>( t_{OCD} )</td>
</tr>
<tr>
<td>Circuit Current</td>
<td>( V_{SNS} &gt; V_{SC} )</td>
<td>( t_{SCD} )</td>
</tr>
</tbody>
</table>

\( V_{IS1} - V_{IS2} \). Logic high = \( V_{PLS} \) for \( CC \) and \( V_{DD} \) for \( DC \). All voltages are with respect to VSS. \( I_{SNS} \) is the current delivered from pin SNS.

\( V_{DD} < 2.2 \) V, release is delayed until the recovery charge current \( (I_{RC}) \) passed from PLS to \( V_{DD} \) charges the battery and allows \( V_{DD} \) to exceed 2.2 V.

For the internal sense resistor configuration, the overcurrent thresholds are expressed in terms of current: \( I_{SNS} > I_{OC} \) for charge direction and \( I_{SNS} < -I_{OC} \) for discharge direction.

With test current \( I_{ST1} \) current flowing from PLS to VSS (pull-down on PLS)

With test current \( I_{ST2} \) current flowing from \( V_{DD} \) to PLS (pull-up on PLS)

\( V_{DD} \) voltage. If the voltage of the cell exceeds overvoltage threshold \( V_{OV} \) for a period longer than voltage delay \( t_{OVD} \), the DS2760 shuts off the external charge FET and sets the OV flag in the section Register. When the cell voltage falls below charge enable threshold \( V_{CE} \), the DS2760 turns the
FET back on (unless another protection condition prevents it). Discharging remains enabled overvoltage.

**voltage.** If the voltage of the cell drops below undervoltage threshold $V_{UV}$ for a period longer than voltage delay $t_{UVD}$, the DS2760 shuts off the charge and discharge FETs, sets the UV flag in the protection register, and enters Sleep Mode. The DS2760 provides a current-limited (IRC) recovery path from PLS to VDD to gently charge severely depleted cells. The recovery path is enabled if $0 \leq VDD < 3\text{V}(\text{typ})$. Once VDD reaches $3\text{V}(\text{typ})$, the DS2760 will return to normal operation, connecting of a charger to turn on the charge FET and pull out of Sleep Mode.

**current, Charge Direction.** The voltage difference between the IS1 pin and the IS2 pin ($V_{IS} = V_{IS1}$) is the filtered voltage drop across the current sense resistor. If $V_{IS}$ exceeds overcurrent threshold $r$ a period longer than overcurrent delay $t_{OCD}$, the DS2760 shuts off both external FETs and sets the flag in the Protection Register. The charge current path is not re-established until the voltage on the in drops below $V_{DD} - V_{TP}$. The DS2760 provides a test current of value $I_{TST}$ from PLS to VDD to LS down in order to detect the removal of the offending charge current source.

**current, Discharge Direction.** If $V_{IS}$ is less than $-V_{OC}$ for a period longer than $t_{OCD}$, the DS2760 shuts off the external discharge FET and sets the DOC flag in the Protection Register. The discharge current path is not re-established until the voltage on PLS rises above $V_{DD} - V_{TP}$. The DS2760 provides a test current of value $I_{TST}$ from VDD to PLS to pull PLS up in order to detect the removal of the offending impedance load.

**Circuit.** If the voltage on the SNS pin with respect to VSS exceeds short circuit threshold $V_{SC}$ for a period longer than short circuit delay $t_{SCD}$, the DS2760 shuts off the external discharge FET and sets the flag in the Protection Register. The discharge current path is not re-established until the voltage on PLS rises above $V_{DD} - V_{TP}$. The DS2760 provides a test current of value $I_{TST}$ from VDD to PLS to pull PLS up in order to detect the removal of the short circuit.

**IIUM-ION PROTECTION CIRCUITRY EXAMPLE WAVEFORMS** Figure 3

(1) To allow the device to react quickly to short circuits, detection is actually done on the SNS pin rather than on the filtered IS1 and IS2 pins. The actual short circuit detect condition is $V_{SNS} > V_{SC}$. 

7
All of the protection conditions described above are OR’ed together to affect the \( \overline{DC} \) and \( \overline{CC} \) s.

\[
\overline{DC} = \text{(Undervoltage) or (Overcurrent, EITHER Direction) or (Short Circuit) or (Protection Register bit DE = 0) or (Sleep Mode)}
\]

\[
\overline{CC} = \text{(Overvoltage) or (Undervoltage) or (Overcurrent, Charge Direction) or (Protection Register bit CE = 0) or (Sleep Mode)}
\]

**RENT MEASUREMENT**

Active Mode of operation, the DS2760 continually measures the current flow into and out of the \( y \) by measuring the voltage drop across a current sense resistor. The DS2760 is available in two configurations: (1) internal 25m\( \Omega \) current sense resistor, and (2) external user-selectable sense resistor. In configuration, the DS2760 considers the voltage difference between pins IS1 and IS2 \( (V_{IS} = V_{IS1} - V_{IS2}) \) to be the filtered voltage drop across the sense resistor. A positive \( V_{IS} \) value indicates current is flowing into the battery (charging), while a negative \( V_{IS} \) value indicates current is flowing out of the battery (discharging).

measured with a signed resolution of 12-bits. The current register is updated in two’s complement every 88ms \((128/f_{sample})\) with an average of 128 readings. Currents outside the range are reported at the limit of the range. The format of the Current Register is shown in Figure 4.

In the internal sense resistor configuration, the DS2760 maintains the Current Register in units of Amps, a resolution of 0.625mA and full scale range of no less than ±1.9A (see Note 7 on \( I_{PS} \) spec for more details). The DS2760 automatically compensates for internal sense resistor process variations and temperature effects when reporting current.

In the external sense resistor configuration, the DS2760 writes the measured \( V_{IS} \) voltage to the Current Register, with a resolution of 15.625\( \mu \)V and a full scale range of ±64mV.

**RENT REGISTER FORMAT** Figure 4

<table>
<thead>
<tr>
<th>MSB—Address 0E</th>
<th>LSb—Address 0F</th>
</tr>
</thead>
<tbody>
<tr>
<td>2^11 2^10 2^9 2^8 2^7 2^6 2^5</td>
<td>2^4 2^3 2^2 2^1 2^0 X X X</td>
</tr>
</tbody>
</table>

**RENT ACCUMULATOR**

Current Accumulator facilitates remaining capacity estimation by tracking the net current flow into and out of the battery. Current flow into the battery increments the Current Accumulator while current out of the battery decrements it. Data is maintained in the Current Accumulator in two’s-complement format. The format of the Current Accumulator is shown in Figure 5.

In the internal sense resistor is used, the DS2760 maintains the Current Accumulator in units of Amps, with a resolution of 0.25mAhrs and full scale range of ±8.2Ahrs. When using an external sense
The DS2760 maintains the Current Accumulator in units of Volt-hours, with a resolution of \( V\text{hrs} \) and a full scale range of \( \pm 205 \text{ mVhrs} \).

The Current Accumulator is a read/write register that can be altered by the host system as needed.

**RENT ACCUMULATOR FORMAT** Figure 5

<table>
<thead>
<tr>
<th>MSB — Address 10</th>
<th>LSb — Address 11</th>
</tr>
</thead>
<tbody>
<tr>
<td>S 2^14 2^13 2^12 2^11 2^10 2^9 2^8</td>
<td>2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0</td>
</tr>
<tr>
<td>MSb</td>
<td>LSb</td>
</tr>
</tbody>
</table>

**RENT OFFSET COMPENSATION**

Measurement and the current accumulation are both internally compensated for offset on a per basis minimizing error resulting from variations in device temperature and voltage. Typically a constant bias may be utilized to alter any other sources of offset. This bias resides in the address 33h in two's-complement format and is subtracted from each current measurement. The default for the current offset compensation is a value of 0.

**RENT OFFSET BIAS** Figure 6

<table>
<thead>
<tr>
<th>Address 33</th>
</tr>
</thead>
<tbody>
<tr>
<td>S 2^6 2^5 2^4 2^3 2^2 2^1 2^0</td>
</tr>
<tr>
<td>MSb</td>
</tr>
</tbody>
</table>

**VAGE MEASUREMENT**

DS2760 continually measures the voltage between pins VIN and VSS over a range of 0 to 4.75V. The resulting data is placed in the Voltage Register in two's-complement format with a resolution of \( nV \). Voltages above the maximum register value are reported as the maximum value. The Voltage Register format is shown in Figure 7.

**VAGE REGISTER FORMAT** Figure 7

<table>
<thead>
<tr>
<th>MSB — Address 0C</th>
<th>LSb — Address 0D</th>
</tr>
</thead>
<tbody>
<tr>
<td>S 2^9 2^8 2^7 2^6 2^5 2^4 2^3</td>
<td>2^2 2^1 2^0 X X X X X</td>
</tr>
<tr>
<td>MSb</td>
<td>LSb</td>
</tr>
</tbody>
</table>

Units: 4.88 mV
**Temperature Measurement**

DS2760 uses an integrated temperature sensor to continually measure battery temperature. Temperature measurements are placed in the Temperature Register in two's-complement format with a resolution of 0.125°C over a range of ±127°C. The Temperature Register format is shown in Figure 8.

**Temperature Register Format** Figure 8

<table>
<thead>
<tr>
<th>MSB—Address 18</th>
<th>LSB—Address 19</th>
</tr>
</thead>
<tbody>
<tr>
<td>S 29 28 27 26 25 24 23</td>
<td>22 21 20 X X X X</td>
</tr>
</tbody>
</table>

MSb LSb MSb LSb

Units: 0.125°C

**Grammable I/O**

When the PIO pin as an output, write the desired output value to the PIO bit in the Special Feature Register. Writing a 0 to the PIO bit enables the PIO output driver, pulling the PIO pin to VSS. Writing a 1 to the PIO bit disables the output driver, allowing the PIO pin to be pulled high or used as an input. To read the value on the PIO pin, read the PIO bit. The DS2760 turns off the PIO output driver and sets the PIO pin high when it enters Sleep Mode or when DQ is low for more than 2 seconds, regardless of the state of the PMOD bit.

**Switch Input**

DS2760 provides a power control function that uses the discharge protection FET to gate battery power to the system. The PS pin, internally pulled to VDD through a 1μA current source, is continuously monitored for a low-impedance connection to VSS. If the DS2760 is in Sleep Mode, the detection of a low PS causes the device to transition into Active Mode, turning on the discharge FET. If the DS2760 is already in Active Mode, activity on PS has no effect other than the mirroring of its logic level in the PS bit in the Special Feature Register. The reading of a 0 in the PS bit should be immediately followed by setting a 1 to the PS bit to ensure proper operation.

**Memory**

DS2760 has a 256-byte linear address space with registers for instrumentation, status and control in power 32 bytes, with lockable EEPROM and SRAM memory occupying portions of the remaining address space. All EEPROM and SRAM memory is general-purpose except addresses 30h, 31h, and 33h, which should be written with the default values for the Protection Register, Status Register, and Current Register, respectively. When the MSB of any 2-byte register is read, both the MSB and LSB are read and held for the duration of the Read Data command to prevent updates during the read and to synchronize between the two register bytes. For consistent results, always read the MSB and LSB of a two-byte register during the same Read Data command sequence.

ROM memory is shadowed by RAM to eliminate programming delays between writes and to allow data to be verified by the host system before being copied to EEPROM. All reads and writes to/from ROM memory actually access the shadow RAM. In unlocked EEPROM blocks, the Write Data command updates shadow RAM. In locked EEPROM blocks, the Write Data command is ignored. The Write Data command copies the contents of shadow RAM to EEPROM in an unlocked block of ROM but has no effect on locked blocks. The Recall Data command copies the contents of a block of ROM to shadow RAM regardless of whether the block is locked or not.
<table>
<thead>
<tr>
<th>Address (Hex)</th>
<th>Description</th>
<th>Read/Write</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Protection Register</td>
<td>R/W</td>
</tr>
<tr>
<td>01</td>
<td>Status Register</td>
<td>R</td>
</tr>
<tr>
<td>02-06</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>07</td>
<td>EEPROM Register</td>
<td>R/W</td>
</tr>
<tr>
<td>08</td>
<td>Special Feature Register</td>
<td>R/W</td>
</tr>
<tr>
<td>09-0B</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>0C</td>
<td>Voltage Register MSb</td>
<td>R</td>
</tr>
<tr>
<td>0D</td>
<td>Voltage Register LSb</td>
<td>R</td>
</tr>
<tr>
<td>0E</td>
<td>Current Register MSB</td>
<td>R</td>
</tr>
<tr>
<td>0F</td>
<td>Current Register LSb</td>
<td>R</td>
</tr>
<tr>
<td>10</td>
<td>Accumulated Current Register MSB</td>
<td>R/W</td>
</tr>
<tr>
<td>11</td>
<td>Accumulated Current Register LSb</td>
<td>R/W</td>
</tr>
<tr>
<td>12-17</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>Temperature Register MSB</td>
<td>R</td>
</tr>
<tr>
<td>19</td>
<td>Temperature Register LSb</td>
<td>R</td>
</tr>
<tr>
<td>1A-1F</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>20-2F</td>
<td>EEPROM, block 0</td>
<td>R/W*</td>
</tr>
<tr>
<td>30-3F</td>
<td>EEPROM, block 1</td>
<td>R/W*</td>
</tr>
<tr>
<td>40-7F</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>80-8F</td>
<td>SRAM</td>
<td>R/W</td>
</tr>
<tr>
<td>90-FF</td>
<td>Reserved</td>
<td></td>
</tr>
</tbody>
</table>

EEPROM block is read/write until locked by the LOCK command, after which it is read-only.

**Protection Register**

Protection Register consists of flags that indicate protection circuit status and switches that give functional control over the charging and discharging paths. Bits OV, UV, COC and DOC are set when corresponding protection conditions occur and remain set until cleared by the host system. The default values of the CE and DE bits of the Protection Register are stored in lockable EEPROM in the corresponding bits in address 30h. A Recall Data command for EEPROM block 1 recalls the default values of 1 into CE and DE. The format of the Protection Register is shown in Figure 9. The function of each bit is described in detail in the following paragraphs.

**Protection Register Format Figure 9**

Address 00

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>OV</td>
<td>UV</td>
<td>COC</td>
<td>DOC</td>
<td>GC</td>
<td>DC</td>
<td>CE</td>
<td>DE</td>
</tr>
</tbody>
</table>

- Overvoltage Flag. When set to 1, this bit indicates the battery pack has experienced an overvoltage condition. This bit must be reset by the host system.

- Undervoltage Flag. When set to 1, this bit indicates the battery pack has experienced an undervoltage condition. This bit must be reset by the host system.
- Charge Overcurrent Flag. When set to 1, this bit indicates the battery pack has experienced a direction overcurrent condition. This bit must be reset by the host system.

- Discharge Overcurrent Flag. When set to 1, this bit indicates the battery pack has experienced a direction overcurrent condition. This bit must be reset by the host system.

\( \overline{CC} \) Pin Mirror. This read-only bit mirrors the state of the \( \overline{CC} \) output pin.

\( \overline{DC} \) Pin Mirror. This read-only bit mirrors the state of the \( \overline{DC} \) output pin.

Charge Enable. Writing a 0 to this bit disables charging (\( \overline{CC} \) output high, external charge FET off) unless of cell or pack conditions. Writing a 1 to this bit enables charging, subject to override by the presence of any protection conditions. The DS2760 automatically sets this bit to 1 when it transitions from Sleep Mode to Active Mode.

Discharge Enable. Writing a 0 to this bit disables discharging (\( \overline{DC} \) output high, external discharge FET off) regardless of cell or pack conditions. Writing a 1 to this bit enables discharging, subject to override by the presence of any protection conditions. The DS2760 automatically sets this bit to 1 when it transitions from Sleep Mode to Active Mode.

**STATUS REGISTER**

Default values for the Status Register bits are stored in lockable EEPROM in the corresponding bits address 31h. A Recall Data command for EEPROM block 1 recalls the default values into the Status Register. The format of the Status Register is shown in Figure 10. The function of each bit is described in detail in the following paragraphs.

**STATUS REGISTER FORMAT** Figure 10

<table>
<thead>
<tr>
<th>Address 01</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
</tr>
<tr>
<td>X</td>
</tr>
</tbody>
</table>

- **PMOD** – Sleep Mode Enable. A value of 1 in this bit enables the DS2760 to enter Sleep Mode when the line goes low for greater than 2 seconds and leave Sleep Mode when the DQ line goes high. A value of 0 disables DQ-related transitions into and out of Sleep Mode. This bit is read-only. The desired default value should be set in bit 5 of address 31h. The factory default is 0.

- **RNAOP** – Read Net Address Opcode. A value of 0 in this bit sets the opcode for the Read Net Address command to 33h, while a 1 sets the opcode to 39h. This bit is read-only. The desired default value should be set in bit 4 of address 31h. The factory default is 0.

- **SWEN** - SWAP Command Enable. A value of 1 in this bit location enables the recognition of a SWAP command. If set to 0, SWAP commands are ignored. The desired default value should be set in bit 3 of address 31h. This bit is read-only. The factory default is 0.

Reserved bits.
ROM REGISTER

Format of the EEPROM Register is shown in Figure 11. The function of each bit is described in the following paragraphs.

ROM REGISTER FORMAT Figure 11

<table>
<thead>
<tr>
<th>Address 07</th>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEC LOCK</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>BL1</td>
<td>BL0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- EEPROM Copy Flag. A 1 in this read-only bit indicates that a Copy Data command is in progress. While this bit is high, writes to EEPROM addresses are ignored. A 0 in this bit indicates that data may be written to unlocked EEPROM blocks.

- EEPROM Lock Enable. When this bit is 0, the Lock command is ignored. Writing a 1 to this enables the Lock command. After the Lock command is executed, the LOCK bit is reset to 0. The default is 0.

- EEPROM Block 1 Lock Flag. A 1 in this read-only bit indicates that EEPROM Block 1 (addresses 30-3F) is locked (read-only) while a 0 indicates Block 1 is unlocked (read/write).

- EEPROM Block 0 Lock Flag. A 1 in this read-only bit indicates that EEPROM Block 0 (addresses 20-2F) is locked (read-only) while a 0 indicates Block 0 is unlocked (read/write).

Reserved bits.

SPECIAL FEATURE REGISTER

Format of the Special Feature Register is shown in Figure 12. The function of each bit is described in the following paragraphs.

SPECIAL FEATURE REGISTER FORMAT Figure 12

<table>
<thead>
<tr>
<th>Address 08</th>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PS PIO MSTR</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- PS Pin Mirror. This read-only bit mirrors the state of the PS pin. The reading of a 0 in this bit should be immediately followed by writing a 1 to this location to insure proper operation.

- PIO Pin Sense and Control. See the Programmable I/O section for details on this read/write bit.

- SWAP Master Status Bit. This bit indicates whether a device has been selected through the AP command. Selection of this device through the SWAP command and the appropriate Net Address result in setting this bit, indicating that this device is the master. A 0 signifies that this device is not master.

Reserved bits.
**RE BUS SYSTEM**

Wire bus is a system which has a single bus master and one or more slaves. A multidrop bus is a bus with multiple slaves. A single-drop bus has only one slave device. In all instances, the slave is a slave device. The bus master is typically a microprocessor in the host system. The specification of this bus system consists of four topics: 64-Bit Net Address, Hardware Configuration, Action Sequence, and 1-Wire Signaling.

**IT NET ADDRESS**

DS2760 has a unique, factory-programmed 1-Wire net address which is 64 bits in length. The first are the 1-Wire family code (30h for DS2760). The next 48 bits are a unique serial number. The bits are a CRC of the first 56 bits (see Figure 13). The 64-bit net address and the 1-Wire I/O try built into the device enable the DS2760 to communicate via the 1-Wire protocol detailed in the *Bus System* section of this data sheet.

**1-WIRE NET ADDRESS FORMAT** Figure 13

<table>
<thead>
<tr>
<th>8-bit CRC</th>
<th>48-bit Serial Number</th>
<th>8-Bit Family Code 30h)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSb</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>48-bit Serial Number</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>8-Bit Family Code</td>
</tr>
<tr>
<td></td>
<td></td>
<td>30h)</td>
</tr>
<tr>
<td>LSb</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**GENERATION**

DS2760 has an 8-bit CRC stored in the most significant byte of its 1-Wire net address. To ensure reliable transmission of the address, the host system can compute a CRC value from the first 56 bits of the address and compare it to the CRC from the DS2760. The host system is responsible for verifying the value and taking action as a result. The DS2760 does not compare CRC values and does not prevent a command sequence from proceeding as a result of a CRC mismatch. Proper use of the CRC results in a communication channel with a very high level of integrity.

The CRC can be generated by the host using a circuit consisting of a shift register and XOR gates as shown in Figure 10, or it can be generated in software. Additional information about the Dallas 1-Wire IC Redundancy Check is available in Application Note 27 entitled "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products". (This application note can be found on the Maxim/Dallas Semiconductor website at www.maxim-ic.com).

In the circuit in Figure 14, the shift register bits are initialized to 0. Then, starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value.
Because the 1-Wire bus has only a single line, it is important that each device on the bus be able to drive the appropriate time. To facilitate this, each device attached to the 1-Wire bus must connect to the bus with open-drain or tri-state output drivers. The DS2760 used an open-drain output driver as part of directional interface circuitry shown in Figure 15. If a bidirectional pin is not available on the bus, separate output and input pins can be tied together.

1-Wire bus must have a pull-up resistor at the bus-master end of the bus. For short line lengths, the value of this resistor should be approximately 5kΩ. The idle state for the 1-Wire bus is high. If, for any reason, a bus transaction must be suspended, the bus MUST be left in the idle state in order to properly resume the transaction later. If the bus is left low for more than 120μs, slave devices on the bus begin to reset the low period as a Reset Pulse, effectively terminating the transaction.

**IRE BUS INTERFACE CIRCUITRY Figure 15**

**ANSACTION SEQUENCE**

Protocol for accessing the DS2760 via the 1-Wire port is as follows:

- Initialization
- Net Address Command
- Function Command
- Transaction/Data

Sections that follow describe each of these steps in detail.
Actions of the 1-Wire bus begin with an initialization sequence consisting of a Reset Pulse initiated by the bus master followed by a presence pulse simultaneously transmitted by the DS2760 and other slaves on the bus. The presence pulse tells the bus master that one or more devices are on and ready to operate. For more details, see the 1-Wire Signaling section.

ADDRESS COMMANDS

The bus master has detected the presence of one or more slaves, it can issue one of the Net Address commands described in the following paragraphs. The name of each ROM Command is followed by the opcode for that command in square brackets. Figure 16 presents a transaction flowchart of the Net Address Commands.

Net Address [33h or 39h]. This command allows the bus master to read the DS2760's 1-Wire net address. This command can only be used if there is a single slave on the bus. If more than one slave is on, a data collision occurs when all slaves try to transmit at the same time (open-drain produces a -AND result). The RNAOP bit in the Status Register selects the opcode for this command, with OP=0 indicating 33h and RNAOP=1 indicating 39h.

b Net Address [55h]. This command allows the bus master to specifically address one DS2760 on the 1-Wire bus. Only the addressed DS2760 responds to any subsequent Function Command. All other devices ignore the Function Command and wait for a reset pulse. This command can be used with more slave devices on the bus.

Net Address [CCh]. This command saves time when there is only one DS2760 on the bus by allowing the bus master to issue a Function Command without specifying the address of the slave. If more than one slave device is present on the bus, a subsequent Function Command can cause a data collision when all slaves transmit data at the same time.

Net Address [FOh]. This command allows the bus master to use a process of elimination to identify the 1-Wire net addresses of all slave devices on the bus. The search process involves the iteration of a simple three-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple three-step routine on each bit location of the net address. After one complete pass through all 64 bits, the bus master knows the address of one device. Remaining devices can then be identified on additional iterations of the process. See Chapter 5 of the DS19xx iButton® Standards for a comprehensive discussion of a net address search, including an example. (This publication can be found on the Maxim/Dallas Semiconductor website at maxim-ic.com).

AP [AAh]. SWAP is a Net Address level command specifically intended to aid in distributed multiplexing applications and is described specifically with regards to power control using the 27xx series products. The term power control refers to the ability of the DS2760 to control the flow of power into the battery pack using control pins DC and CC. The SWAP command is issued followed by the Address. The effect is to cause the addressed device to enable power to or from the system while simultaneously (break-before-make) deselecting and powering down (SLEEP) all other packs. This changing sequence is controlled by a timing pulse issued on the DQ line following the net address. The rising edge of the pulse is used to disable power with the rising edge enabling power flow by the selected device. The DS2760 will recognize a SWAP command, device address, and timing pulse if and only if SWEN bit is set.

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FUNCTION COMMANDS

Successfully completing one of the Net Address Commands, the bus master can access the features of the DS2760 with any of the Function Commands described in the following paragraphs. The name of each function is followed by the 8-bit opcode for that command in square brackets.

Data [69h, XX]. This command reads data from the DS2760 starting at memory address XX. The first data in address XX is available to be read immediately after the MSb of the address has been received. Because the address is automatically incremented after the MSb of each byte is received, the first data at address XX+1 is available to be read immediately after the MSb of the data at address XX. If the bus master continues to read beyond address FFh, the DS2760 outputs logic 1 until a Reset occurs. Addresses labeled “Reserved” in the Memory Map contain undefined data. The Read Data command may be terminated by the bus master with a Reset Pulse at any bit boundary.

Data [6 Ch, XX]. This command writes data to the DS2760 starting at memory address XX. The first data to be stored at address XX can be written immediately after the MSb of address has been received. Because the address is automatically incremented after the MSb of each byte is written, the LSB stored at address XX+1 can be written immediately after the MSb to be stored at address XX. If the bus master continues to write beyond address FFh, the DS2760 ignores the data. Writes to read-only memory, reserved addresses and locked EEPROM blocks are ignored. Incomplete bytes are not written. Writes to unlocked EEPROM blocks are to shadow RAM rather than EEPROM. See the Memory section for more details.

Data [48h, XX]. This command copies the contents of shadow RAM to EEPROM for the 16-byte $OM block containing address XX. Copy Data commands that address locked blocks are ignored. While the Copy Data command is executing, the EEC bit in the EEPROM Register is set to 1 and writes to EEPROM addresses are ignored. Reads and writes to non-EEPROM addresses can still occur while a copy is in progress. The Copy Data command takes $t_{EEC}$ time to execute, starting on the next falling edge of the address.

Write Data [B8h, XX]. This command recalls the contents of the 16-byte EEPROM block containing address XX to shadow RAM.

Lock [6 Ah, XX]. This command locks (write-protects) the 16-byte block of EEPROM memory starting at memory address XX. The LOCK bit in the EEPROM Register must be set to 1 before the command is executed. If the LOCK bit is 0, the Lock command has no effect. The Lock command remains permanent; a locked block can never be written again.
<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
<th>Command Protocol</th>
<th>Bus State After Command Protocol</th>
<th>Bus Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>rd Data</td>
<td>Reads data from memory starting at address XX</td>
<td>69h, XX</td>
<td>Master Rx</td>
<td>up to 256 bytes of data</td>
</tr>
<tr>
<td>ite Data</td>
<td>Writes data to memory starting at address XX</td>
<td>6Ch, XX</td>
<td>Master Tx</td>
<td>up to 256 bytes of data</td>
</tr>
<tr>
<td>py Data</td>
<td>Copies shadow RAM data to EEPROM block containing address XX</td>
<td>48h, XX</td>
<td>Bus Idle</td>
<td>none</td>
</tr>
<tr>
<td>:all Data</td>
<td>Recalls EEPROM block containing address XX to shadow RAM</td>
<td>B8h, XX</td>
<td>Bus Idle</td>
<td>none</td>
</tr>
<tr>
<td>:k</td>
<td>Permanently locks the block of EEPROM containing address XX</td>
<td>6Ah, XX</td>
<td>Bus Idle</td>
<td>none</td>
</tr>
</tbody>
</table>
SIGNALING

1-Wire bus requires strict signaling protocols to insure data integrity. The four protocols used by the DS2760 are: the initialization sequence (Reset Pulse followed by Presence Pulse), Write 0, Write 1, and Data. All of these types of signaling except the Presence Pulse are initiated by the bus master.

The initialization sequence required to begin any communication with the DS2760 is shown in Figure 17. Presence Pulse following a Reset Pulse indicates the DS2760 is ready to accept a Net Address and. The bus master transmits (Tx) a Reset Pulse for \( t_{RST_L} \). The bus master then releases the lines into receive mode (Rx). The 1-Wire bus lines are then pulled high by the pull-up resistor. After the rising edge on the DQ pin, the DS2760 waits for \( t_{DH} \) and then transmits the Presence Pulse \( L \).

**1-WIRE INITIALIZATION SEQUENCE** Figure 17

![Diagram of initialization sequence](image)

**LINE TYPE LEGEND:**
- Bus master active low
- Both bus master and DS2760 active low
- DS2760 active low
- Resistor pullup

**WRITE TIME SLOTS**

A write time slot is initiated when the bus master pulls the 1-Wire bus from a logic high (inactive) level to a low level. There are two types of write time slots: Write 1 and Write 0. All write time slots must be \( t_{SLOT} \) (60\( \mu \)S to 120\( \mu \)S) in duration with a 1\( \mu \)S minimum recovery time, \( t_{REC} \), between cycles. The DS2760 samples the 1-Wire bus line between 15\( \mu \)S and 60\( \mu \)S after the line falls. If the line is high when led, a Write 1 occurs. If the line is low when sampled, a Write 0 occurs (see Figure 18). For the bus master to generate a Write 1 time slot, the bus line must be pulled low and then released, allowing the line pulled high within 15\( \mu \)S after the start of the write time slot. For the host to generate a Write 0 time slot the bus line must be pulled low and held low for the duration of the write time slot.

**READ TIME SLOTS**

A read time slot is initiated when the bus master pulls the 1-Wire bus line from a logic high level to a low level. The bus master must keep the bus line low for at least 1\( \mu \)S and then release it to allow the DS2760 to present valid data. The bus master can then sample the data \( t_{RDV} \) (15\( \mu \)S) from the start of the time slot. By the end of the read time slot, the DS2760 releases the bus line and allows it to be pulled high by the external pull-up resistor. All read time slots must be \( t_{SLOT} \) (60\( \mu \)S to 120\( \mu \)S) in duration a 1\( \mu \)S minimum recovery time, \( t_{REC} \), between cycles. See Figure 18 for more information.
RE WRITE AND READ TIME SLOTS Figure 18

WRITE 0 SLOT
\[ t_{SLOT} \prec t_{LOW0} \prec t_{REC} \]
WRITE 1 SLOT
\[ t_{SLOT} \prec t_{LOW1} \prec t_{REC} \]

PACK+

PACK–

DS2760 Sample Window
\[
\begin{array}{ccc}
\text{MIN} & \text{TYP} & \text{MAX} \\
15\mu s & 15\mu s & 30\mu s \\
\end{array}
\]

DS2760 Sample Window
\[
\begin{array}{ccc}
\text{MIN} & \text{TYP} & \text{MAX} \\
15\mu s & 15\mu s & 30\mu s \\
\end{array}
\]

READ 0 SLOT
\[ t_{SLOT} \prec t_{REC} \]
READ 1 SLOT
\[ t_{SLOT} \prec t_{REC} \]

PACK+

PACK–

Master Sample Window
\[ t_{RDV} \]

Master Sample Window
\[ t_{RDV} \]

LINE TYPE LEGEND:
- Bus master active low
- Both bus master and DS2760 active low
- DS2760 active low
- Resistor pullup

AP COMMAND TIMING Figure 19

DQ
\[ t_{SWL} \]
\[ t_{SWOFF} \]

\[ t_{SWON} \]

CC, DC
OLUTE MAXIMUM RATINGS*

-0.3V to +18V
-0.3V to +12V
-0.3V to VDD + 0.3
-0.3V to +6V
±2.5A
±50A for <100μs/sec, <1000 pulses
-40°C to +85°C
-55°C to +125°C
See IPC/JEDEC J-STD-020A Specification

Internal Sense Resistor Current

-40°C to +85°C
-55°C to +125°C

Typing Temperature Range

-20°C to +70°C; 2.5V ≤ VDD ≤ 5.5V

<table>
<thead>
<tr>
<th>AMETER</th>
<th>SYMBOL</th>
<th>CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jly Voltage</td>
<td>VDD</td>
<td></td>
<td>2.5</td>
<td>5.5</td>
<td></td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Pin</td>
<td>DQ</td>
<td></td>
<td>-0.3</td>
<td>5.5</td>
<td></td>
<td>V</td>
<td>1</td>
</tr>
</tbody>
</table>

ELECTRICAL CHARACTERISTICS

-20°C to +70°C; 2.5V ≤ VDD ≤ 5.5V

<table>
<thead>
<tr>
<th>AMETER</th>
<th>SYMBOL</th>
<th>CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jve Current</td>
<td>IACTIVE</td>
<td>DQ = VDD, norm. operation</td>
<td>60</td>
<td>90</td>
<td></td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Jp Mode Current</td>
<td>ISLEEP</td>
<td>DQ = 0V, no activity, PS floating</td>
<td>1</td>
<td>2</td>
<td></td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>t Logic High: PIO</td>
<td>VIL</td>
<td></td>
<td>1.5</td>
<td></td>
<td>V</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>t Logic High: PS</td>
<td>VIH</td>
<td>VDD - 0.2V</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>t Logic Low: PIO</td>
<td>VIH</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>t Logic Low: PS</td>
<td>VIH</td>
<td>VDD - 0.4V</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>out Logic High: CC</td>
<td>VOH</td>
<td>IOH = -0.1mA</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>out Logic High: DC</td>
<td>VOH</td>
<td>IOH = -0.1mA</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>out Logic Low: DC</td>
<td>VOL</td>
<td>IOH = 0.1mA</td>
<td>0.4</td>
<td></td>
<td>V</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>out Logic Low: PIO</td>
<td>VOL</td>
<td>IOL = 4mA</td>
<td>0.4</td>
<td></td>
<td>V</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Pulldown Current</td>
<td>IPD</td>
<td></td>
<td>1</td>
<td></td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Jt Resistance: VIN</td>
<td>RIN</td>
<td></td>
<td>5</td>
<td></td>
<td>MΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>nnal Current Sense istor</td>
<td>RSNS</td>
<td>+25°C</td>
<td>20</td>
<td>25</td>
<td>30</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>Low to Sleep time</td>
<td>tSLEEP</td>
<td></td>
<td>2.1</td>
<td></td>
<td>sec</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**ELECTRICAL CHARACTERISTICS:**

**DTECTION CIRCUITRY**  
(0°C to +50°C; 2.5V ≤ \(V_{DD}\) ≤ 5.5V)

<table>
<thead>
<tr>
<th>AMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>voltage Detect</td>
<td>(V_{OV})</td>
<td>4.325</td>
<td>4.350</td>
<td>4.375</td>
<td>V</td>
<td>1, 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.250</td>
<td>4.275</td>
<td>4.300</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ge Enable</td>
<td>(V_{CE})</td>
<td>4.10</td>
<td>4.15</td>
<td>4.20</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>voltage Detect</td>
<td>(V_{UV})</td>
<td>2.5</td>
<td>2.6</td>
<td>2.7</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>current Detect</td>
<td>(I_{OC})</td>
<td>1.8</td>
<td>1.9</td>
<td>2.0</td>
<td>A</td>
<td>3</td>
</tr>
<tr>
<td>current Detect</td>
<td>(V_{OC})</td>
<td>45</td>
<td>47.5</td>
<td>50</td>
<td>mV</td>
<td>1, 4</td>
</tr>
<tr>
<td>t Circuit Detect</td>
<td>(I_{SC})</td>
<td>5.0</td>
<td>8.0</td>
<td>11</td>
<td>A</td>
<td>3</td>
</tr>
<tr>
<td>t Circuit Detect</td>
<td>(V_{SC})</td>
<td>150</td>
<td>200</td>
<td>250</td>
<td>mV</td>
<td>1</td>
</tr>
<tr>
<td>voltage Delay</td>
<td>(t_{OVD})</td>
<td>0.8</td>
<td>1</td>
<td>1.2</td>
<td>sec</td>
<td></td>
</tr>
<tr>
<td>voltage Delay</td>
<td>(t_{UVD})</td>
<td>90</td>
<td>100</td>
<td>110</td>
<td>ms</td>
<td>1</td>
</tr>
<tr>
<td>current Delay</td>
<td>(t_{OCD})</td>
<td>5</td>
<td>10</td>
<td>20</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>t Circuit Delay</td>
<td>(t_{SCD})</td>
<td>80</td>
<td>100</td>
<td>120</td>
<td>(\mu s)</td>
<td>3</td>
</tr>
<tr>
<td>Threshold</td>
<td>(V_{TP})</td>
<td>0.5</td>
<td>1.0</td>
<td>1.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Current</td>
<td>(I_{TST})</td>
<td>10</td>
<td>20</td>
<td>40</td>
<td>(\mu A)</td>
<td></td>
</tr>
<tr>
<td>Very Charge Current</td>
<td>(I_{RC})</td>
<td>0.5</td>
<td>1</td>
<td>2</td>
<td>mA</td>
<td>13</td>
</tr>
</tbody>
</table>
**TRICAL CHARACTERISTICS:**
**TEMPERATURE, VOLTAGE, CURRENT**

(0°C to +50°C; 2.5V ≤ V<sub>DD</sub> ≤ 5.5V)

<table>
<thead>
<tr>
<th>AMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Resolution</td>
<td>T&lt;sub&gt;LSB&lt;/sub&gt;</td>
<td>0.125</td>
<td></td>
<td></td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Temperature Full Scale Resolution</td>
<td>T&lt;sub&gt;FS&lt;/sub&gt;</td>
<td>127</td>
<td></td>
<td></td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Temperature Error</td>
<td>T&lt;sub&gt;ERR&lt;/sub&gt;</td>
<td>±3</td>
<td></td>
<td></td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Voltage Resolution</td>
<td>V&lt;sub&gt;LSB&lt;/sub&gt;</td>
<td>4.88</td>
<td></td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Voltage Full Scale Resolution</td>
<td>V&lt;sub&gt;FS&lt;/sub&gt;</td>
<td>4.75</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Voltage Offset Error</td>
<td>V&lt;sub&gt;OE&lt;/sub&gt;</td>
<td>1</td>
<td>LSB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage Gain Error</td>
<td>V&lt;sub&gt;GE&lt;/sub&gt;</td>
<td>5</td>
<td>%V</td>
<td>reading</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Resolution</td>
<td>I&lt;sub&gt;LSB&lt;/sub&gt;</td>
<td>0.625</td>
<td></td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Current Full Scale Resolution</td>
<td>I&lt;sub&gt;FS&lt;/sub&gt;</td>
<td>1.9</td>
<td>2.56</td>
<td>64</td>
<td>A</td>
<td>3, 7</td>
</tr>
<tr>
<td>Current Offset Error</td>
<td>I&lt;sub&gt;O&lt;/sub&gt;</td>
<td>1</td>
<td>LSB</td>
<td>1</td>
<td>mV</td>
<td>4</td>
</tr>
<tr>
<td>Current Gain Error</td>
<td>I&lt;sub&gt;G&lt;/sub&gt;</td>
<td>3</td>
<td>%I</td>
<td>reading</td>
<td>3, 9, 14</td>
<td>4</td>
</tr>
<tr>
<td>Cumulated Current Resolution</td>
<td>q&lt;sub&gt;CA&lt;/sub&gt;</td>
<td>0.25</td>
<td></td>
<td></td>
<td>mAh</td>
<td>3</td>
</tr>
<tr>
<td>Cumulated Current Resolution</td>
<td>6.25</td>
<td></td>
<td></td>
<td></td>
<td>μVh</td>
<td>4</td>
</tr>
<tr>
<td>Cumulated Sampling Frequency</td>
<td>f&lt;sub&gt;SAMP&lt;/sub&gt;</td>
<td>1456</td>
<td></td>
<td></td>
<td>Hz</td>
<td></td>
</tr>
<tr>
<td>Cumulated Timebase Accuracy</td>
<td>t&lt;sub&gt;ERR&lt;/sub&gt;</td>
<td>±1</td>
<td>±3</td>
<td></td>
<td>%</td>
<td>10</td>
</tr>
</tbody>
</table>
TRICAL CHARACTERISTICS:

RE INTERFACE

(-20°C to +70°C; 2.5V ≤ V_{DD} ≤ 5.5V)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slot tSLOTT</td>
<td>60</td>
<td>120</td>
<td>µs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Every Time tREC</td>
<td>1</td>
<td></td>
<td>µs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 Low Time tLOW0</td>
<td>60</td>
<td>120</td>
<td>µs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 Low Time tLOW1</td>
<td>1</td>
<td>15</td>
<td>µs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data Valid tRDV</td>
<td></td>
<td>15</td>
<td>µs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Time High tRSTH</td>
<td>480</td>
<td></td>
<td>µs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Time Low tRSTL</td>
<td>480</td>
<td>960</td>
<td>µs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sense Detect High tPDH</td>
<td>15</td>
<td>60</td>
<td>µs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sense Detect Low tPDL</td>
<td>60</td>
<td>240</td>
<td>µs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AP timing pulse width tSWL</td>
<td>0.2</td>
<td>120</td>
<td>µs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AP timing pulse rising to DC release tSWOFF</td>
<td>0</td>
<td>1</td>
<td>µs</td>
<td>12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AP timing pulse rising to DC engage tSWON</td>
<td>0</td>
<td>1</td>
<td>µs</td>
<td>12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitance CDQ</td>
<td></td>
<td>60</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

ROM RELIABILITY SPECIFICATION

(-20°C to +70°C; 2.5V ≤ V_{DD} ≤ 5.5V)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>y to EEPROM Time t_EEC</td>
<td>2</td>
<td>10</td>
<td>ms</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROM Copy Endurance N_EEC</td>
<td>25000</td>
<td></td>
<td>cycles</td>
<td>11</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

TEES

1. Voltages are referenced to VSS.
2. "Ordering Information" section of datasheet to determine corresponding part number for each V_{OV} value.
3. Internal current sense resistor configuration.
4. Self heating due to output pin loading and sense resistor power dissipation can alter the reading from ambient conditions.
5. Voltage offset measurement is with respect to V_{OV} at +25°C.
6. Current register supports measurement magnitudes up to 2.56A using the internal sense resistor option and 64mV with external external resistor option. Compensation of the internal sense resistor value for process and temperature variation can reduce the maximum reportable magnitude to 1.9A.
7. Offset error null to ±1LSB typically requires 3.5s in-system calibration by user.
8. Current gain error specification applies to gain error in converting the voltage difference at IS1 and IS2, and excludes any error remaining after the DS2760 compensates for the internal sense resistor's temperature coefficient of 3700ppm/°C to an accuracy of ±500ppm/°C. The DS2760 does not compensate for external sense resistor characteristics, and any error arising from the use of an external sense resistor should be taken into account when calculating total current measurement error.
9. Typical value for t_{ESR} is at 3.6V and +25°C.
10. -year data retention at +70°C.
11. Typical load capacitance on DC and CC is 1000pF.
12. Test conditions are PLS = 4.1V, V_{DD} = 2.5V. Maximum current for conditions of PLS = 15V, V_{DD} = 0V is 10mA.
13. Error at time of shipment from Dallas Semiconductor is 3% max. Board mounting processes may cause the current gain error to widen to as much as 10% for devices with the internal sense resistor option. Contact factory for on-board recalibration procedure for devices with the internal sense resistor option to improve accuracy.
DS2760 Thermocouple Kit (#28022)
1-Wire® Thermocouple Interface

Introduction

Thermocouples provide a low-cost, reliable means of measuring temperature over a wide range. The challenge when using a thermocouple is accurately measuring the very low Seebeck output voltage (fractional to low millivolts) from the element, and providing for cold junction temperature compensation.

The Dallas/Maxim DS2760 High Precision Li+ Battery Monitor is very easily configured into an effective thermocouple interface. The Parallax DS2760 Thermocouple Module capitalizes on this application and provides a complete connection between the BASIC Stamp and a standard thermocouple element.

Features

- 1-Wire® interface allows multiple devices with just one Stamp IO pin
- Cold Junction measurement: 0°C to +127°C (0.125°C resolution)
- Low power consumption:
  -- Active current: 90 µA max
  -- Sleep current: 2 µA max

Packing List

Verify that your DS2760 kit is complete in accordance with the list below:

- DS2760 Thermocouple Module #550-28022
- (3) Thermocouple elements:
  -- (1) K-type (Chromel / Alumel) #800-00011
  -- (1) J-type (Iron / Constantan) #800-00012
  -- (1) T-type (Copper / Constantan) #800-00010
- This documentation

Note: DS2760 demonstration software may be downloaded from www.parallax.com.
Connections

Before connecting the DS2760 Thermocouple Module to the BASIC Stamp you will need to prepare a thermocouple element, and then connect it to the cold junction port of the module. Start by carefully removing about one inch (250 mm) of the outer sleeve from each end of the element. From each lead on the temperature measurement end, remove about ¼ inch (125 mm) of insulation and then carefully twist together (using pliers if necessary) and trim as shown in Figure 1.

Figure 1: Thermocouple Junction

On the cold junction (DS2760 module) end of the element, remove only ¼ inch (60 mm) of insulation from each lead. Route these leads through the bottom of the thermocouple module PCB and insert snuggly into the pin sockets as shown in Figure 2.

Figure 2: Cold Junction Connection to DS2760 PCB

Use this table to ensure that you make the proper thermocouple connections to the module. If the leads are reversed, the measured temperature will be incorrect.

<table>
<thead>
<tr>
<th>Type</th>
<th>Materials</th>
<th>SNS</th>
<th>Vss</th>
</tr>
</thead>
<tbody>
<tr>
<td>K</td>
<td>Chromel / Alumel</td>
<td>Red</td>
<td>Yellow</td>
</tr>
<tr>
<td>J</td>
<td>Iron / Constantan</td>
<td>Red</td>
<td>White</td>
</tr>
<tr>
<td>T</td>
<td>Copper / Constantan</td>
<td>Red</td>
<td>Blue</td>
</tr>
</tbody>
</table>

Finally, the DS2760 Thermocouple Module is connected to the BASIC Stamp as shown in Figure 3 below (Note that the module includes a 4.7 kΩ pull-up on the 1-Wire® data line).

Figure 3: DS2760 Connections to BASIC Stamp

2  Parallax, Inc. · DS2760 Thermocouple Kit (#28022) · 01/2004
BASIC Stamp Application

The following BASIC Stamp application will run on either the BS2p or BS2pe and demonstrates how easy measuring wide-range temperatures can be when using the DS2760 Thermocouple Module. Other Stamps will require a Serial-to-1-Wire protocol converter, as well as code to manage the large tables across program slots, and are not covered in this document.

A little background: When two dissimilar metal wires are joined, a voltage will be developed across the open end that is proportional to the temperature difference between the joined and open ends. This effect was discovered by Thomas Seebeck in 1821. Through empirical testing, voltage tables have been established that correspond to the thermocouple junction temperature. These tables, however, use a cold junction (voltage measurement point) reference of zero degrees Celsius, forcing electronic devices to employ cold junction compensation.

Using the DS2760 we can measure the Seebeck voltage from the thermocouple with a resolution of 15.625 microvolts, then measure the cold junction temperature with a resolution of 0.125 degrees Celsius. A simple table look-up using the cold junction temperature will give us the cold junction compensation voltage. This is combined with the Seebeck voltage and, using a modified binary search algorithm, we can determine the compensated temperature from the thermocouple data table.

---[ Program Description ]-----------------------------------------------

This program lets a BS2p or BS2pe read the temperature from the Parallax DS2760 thermocouple module. User input of thermocouple type (K, J, or T) and temperature display is via the DEBUG window.

---[ Revision History ]-----------------------------------------------------

---[ I/O Definitions ]-----------------------------------------------------

OW PIN 8  ' 1-Wire buss pin

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' ----- [ Constants ]-------------------------------------------------------

ReadNet    CON    $33    ' read OW net address
SkipNet    CON    $CC    ' skip OW net address
RdReg      CON    $69    ' read register

' ----- [ Variables ]-------------------------------------------------------

idx        VAR    Nib    ' loop counter
type       VAR    Nib    ' device type
char       VAR    Byte   ' display byte/char
vIn        VAR    Word   ' in millivolts
tmpCJ      VAR    Word   ' device temp in C
tCuV       VAR    Word   ' thermocouple millivolts
sign       VAR    Word   ' TC sign bit
cjComp     VAR    Word   ' temp compensation
tempC      VAR    Word   ' temp in Celsius
tempF      VAR    Word   ' temp in Fahrenheit
tblLo      VAR    Word   ' table pointers
tblHi      VAR    Word
eePtr      VAR    Word
testVal    VAR    Word   ' test value from table
error      VAR    Bit    ' 1 = out of range

' ----- [ EEPROM Data ]------------------------------------------------------

' ----- [ Initialization ]-----------------------------------------------------

Stamp_Check:
  #IF ($stamp < BS2P) #THEN
    #ERROR "This program requires BS2p or BS2pe"
  #ENDIF

Check_Device:
  OWW    OW, $0001, [ReadNet]    ' get serial number
  OWIN   OW, $0010, [SPSTR 8]    ' store in SPRAM
  GET    idx, char    ' read device type
  IF (char <> $30) THEN
    DEBUG "No DS2760 found."
    STOP    ' stop program
  ENDIF
Menu:
DEBUG CLS,
"==================================", CR,
" DS2760 Thermocouple Interface ", CR,
"==================================", CR,
CR,
"Select TC Type (1 - 3)", CR,
CR,
"(1) K - Chromel/Alumel", CR,
"(2) J - Iron/Constantan", CR,
"(3) T - Copper/Constantan", CR,
CR,
">> "

DEBUGIN DEC1 type
IF (type < 1) OR (type > 3) THEN Menu
DEBUG CRSRXY, 0, 3, CLRDN
STORE type

Show_SN:
DEBUG CRSRXY, 0, 4, "Device SN... 
FOR idx = 0 TO 7
  GET idx, char
  DEBUG HEX2 char
NEXT

Show_Type:
DEBUG CRSRXY, 0, 6, "TC Type...... 
LOOKUP (type - 1), ["KJT"], char
DEBUG char

----- [ Program Code ] --------------------------------------------------------

Main:
DO
  GOSUB Read_TC_Volts
  GOSUB Read_CJ_Temp
  READ (tmpCJ * 2), Word cjComp
  ' combine cjComp and tCuV
  IF sign THEN
    ' TC below cold junction
    IF (tCuV < cjComp) THEN
      cjComp = cjComp - tCuV
    ELSE
      cjComp = 0
    ENDIF

Parallax, Inc. • DS2760 Thermocouple Kit (#28022) • 01/2004
ELSE
    ' TC above cold junction
    cjComp = cjComp + tCuV
ENDIF

LOOKUP type, [1023, 1023, 400], tblHi    ' set high end of search
GOSUB TC_Lookup    ' reverse lookup of table
tempF = tempC * 9 / 5 + 32    ' x 1.8 + 32

IF (error = 0) THEN
    DEBUG CRSRXY, 0, 7,
        "Temp °C..... ", SDEC tempC, CLREOL
    DEBUG CRSRXY, 0, 8,
        "Temp °F..... ", SDEC tempF, CLREOL
ELSE
    DEBUG CRSRXY, 0, 7,
        "Temp °C..... Out of Range", CLREOL
    DEBUG CRSRXY, 0, 8,
        "Temp °F..... Out of Range", CLREOL
ENDIF

PAUSE 1000
LOOP
END

-----[ Subroutines ]---------------------------------------------------------------

' Reads device input voltage (Vin pin)
' -- mV in millivolts (max reading is 4.75 volts)

Read_Vin:
    OWOUT OW, %0001, [SkipNet, RdReg, $0C]
    OWIN OW, %0010, [vIn.BYTE1, vIn.BYTE0]
    IF (vIn.BIT15) THEN
        vIn = 0    ' check sign
    ELSE
        vIn = vIn >> 5 */ $4E1    ' x 4.88 millivolts
    ENDIF
    RETURN

' Reads current register to get TC voltage
' -- each raw bit = 15.625 uV
' -- tCuV in microvolts

Read_TC_Volts:
    OWOUT OW, %0001, [SkipNet, RdReg, $0E]    ' read current register
    OWIN OW, %0010, [tCuV.BYTE1, tCuV.BYTE0]
sign = tCuV.BIT15

IF sign THEN
    tCuV = tCuV | $F000  
ENDIF

tCuV = ABS tCuV */ 4000  
RETURN

' Reads cold junction (device) temperature
' -- each raw bit = 0.125 degrees C
' -- returns tmpCJ in whole degrees C

Read_CJ_Temp:
OWOUT OW, %0001, [SkipNet, RdReg, $18]  
OWIN OW, %0010, [tmpCJ.BYTE1, tmpCJ.BYTE0]  
IF (tmpCJ.BIT15) THEN  
    tmpCJ = 0  
ELSE
    tmpCJ = tmpCJ.HIGHBYTE  
ENDIF
RETURN

' Search currently selected TC table for nearest entry
' -- uses modified binary algorithm to find cjComp
' -- high end of search set before calling (tblHi)
' -- successful search sets tempC

TC_Lookup:
    tblLo = 0  
    tempC = 22  
    READ (tblHi * 2), Word testVal
    IF (cjComp > testVal) THEN  
        error = 1  
    ELSE
        eePntr = (tblLo + tblHi) / 2  
        READ (eePntr * 2), Word testVal
        IF (cjComp = testVal) THEN  
            EXIT  
        ELSEIF (cjComp < testVal) THEN
            tblHi = eePntr
        ELSE
            tblLo = eePntr  
        ENDIF
    ENDIF
IF ((tblHi - tblLo) < 2) THEN 
  eePntr = tblLo
  EXIT
ENDIF
LOOP
tempC = eePntr
ENDIF
RETURN

Additional Resources

- Advanced thermocouple interface software (download from Parallax)
- Web Links:
  -- www.maxim-ic.com/quick_view2.cfm/qv_pk/2931
  -- instserv.com/mocoupl.htm
  -- instrumentation-central.com/pages/thermocouple_reference_table.htm

DS2760 Module Schematic