LAMPIRAN
WR_CTRL_REG EQU 2000H
WR_DATA_REG EQU 2001H
RD_CTRL_REG EQU 2002H
RD_DATA_REG EQU 2003H
COUNTER EQU 39H

ORG 0000H
AJMP MAIN

ORG 100H

MAIN:
    MOV SP,#70H
    ACALL INIT_LCD

LOGO:
    ACALL PRT_TITLE1
    ACALL PRT_TITLE2
    JB P1.7,ZERO_DIAL ;OFF HOOK?
    SJMP LOGO

ZERO_DIAL:
    ACALL PRT_MESSAGE2 ;ENTER YOUR NUMBER

WAIT:
    JB P1.6,NEXT
    SJMP WAIT

NEXT:
    ACALL ZERO_TEST
    JNB P15,STOP ;P15 = 0 = PROTECTED
    JBC P14,LOGO

PROCESS:
    JB P1.6,DATA_READ ;DIAL DITEKAN?
    JNB P1.7,LOGO ;OFF HOOK?
    SJMP PROCESS

STOP:
    SETB P3.0 ;relay on
    ACALL PRT_FAIL
    SJMP STOP

;-------------------------------------------------------------
ZERO_TEST:
    PUSH DPH
    PUSH DPL
    PUSH PSW

    ACALL READ_DATA
    ACALL DATA_OUT
CJNE A,#0,ASSIGN2
AJMP SLJJ
ASSIGN2: CJNE A,#1,ASSIGNX
SJMP READ33
ASSIGNX: AJMP ASSIGN
READ33: JB P1.6,SECOND
;DIAL DITEKAN?
SJMP READ33
SECOND: ACALL READ_DATA
MOV A,BUFFER
ACALL DATA_OUT
CJNE A,#0,ASSIGN
READ33: JB P1.6,THIRD
;DIAL DITEKAN?
SJMP READ33
THIRD: MOV R7,#6
;READ 3Th NUMBER
ACALL READ_DATA
ACALL DATA_OUT
CJNE A,#1,ASSIGN
SLJJ: ACALL PRT_MESSAGE1
;SLJJ
ACALL PASSWORD_READ
ACALL COMPARE
JNB EOS,UNPROTECT
ACALL PRT_MESSAGE4
;ILEGAL CONTACT
SJMP CONTINUED
UNPROTECT: ACALL PRT_MESSAGE3
;LEGAL CONTACT
SETB P3.0
;INIT CONTACT
CLR P3.0
ACALL PRT_MESSAGE2
PROCESS2: JB P1.6,DATA_READ2
;DIAL DITEKAN?
JNB P1.7,LOGO3
SJMP PROCESS2
LOGO3: AJMP LOGO
DATA_READ2: ACALL READ_DATA

NORMAL2: ACALL DATA_OUT
MOV COUNTER,#1
SJMP PROCESS2

CONTINUED: POP PSW
POP DPL
POP DPH
RET

---------------------------------------------------------------------~-----

PASSWORD_READ: PUSH DPH
PUSH DPL
PUSH PSW

READ: JB P1.6,PASSWORD_RD ;DIAL DITEKAN?
SJMP READ

PASSWORD_RD: ACALL READ_DATA
ACALL DATA_OUT

POP PSW
POP DPL
POP DPH
RET

;---------------------------------------------------------------------~-----

COMPARE: PUSH DPH
PUSH DPL
PUSH PSW

UNFAIL2: MOV A,DIGIT2
CJNE A,#5,FAIL
CLR EOS ;EOT = 1 IF MATCH

UNFAIL3: MOV A,DIGIT3
CJNE A,#1,FAIL
CLR EOS ;EOT = 1 IF MATCH

UNFAIL4: MOV A,DIGIT4
CJNE A,#9,FAIL
CLR EOS ;EOT = 1 IF MATCH

UNFAIL5: MOV A, DIGIT5
CJNE A, #4, FAIL
CLR EOS ;EOT = 1 IF MATCH

UNFAIL6: MOV A, DIGIT6
CJNE A, #5, FAIL
CLR EOS ;EOT = 1 IF MATCH
SJMP EXIT

FAIL: SETB EOS

EXIT: POP PSW
POP DPL
POP DPH
RET

;-------------------------------------------------------------------------
PRT TITLE1: PUSH DPH
PUSH DPL
MOV DPTR, #HEADER1
ACALL OUT_CHAR
ACALL LOCATE2
MOV DPTR, #HEADER2
ACALL OUT_CHAR
MOV DPTR, #HEADER3
ACALL OUT_CHAR
MOV DPTR, #HEADER4
ACALL OUT_CHAR
POP DPL
POP DPH
RET

;-------------------------------------------------------------------------
PRT TITLE2: PUSH DPH
PUSH DPL
MOV DPTR, #HEADER5
ACALL OUT_CHAR
MOV DPTR, #HEADER6
ACALL OUT_CHAR
MOV DPTR,#HEADER7
ACALL OUT_CHAR
MOV DPTR,#HEADER8
ACALL OUT_CHAR

POP DPL
POP DP1I
RET

;-----------------------------------------------------------------------------

PRT MESSAGE1:    PUSH DPH
PUSH DPL
MOV DPTR,#HEADER9
ACALL OUT_CHAR
MOV DPTR,#HEADER10
ACALL OUT_CHAR

POP DPL
POP DPH
RET

;-----------------------------------------------------------------------------

PRT MESSAGE2:    PUSH DPH
PUSH DPL
MOV DPTR,#HEADER11
ACALL OUT_CHAR
MOV DPTR,#HEADER12
ACALL OUT_CHAR

POP DPL
POP DPH
RET

;-----------------------------------------------------------------------------

PRT MESSAGE3:    PUSH DPH
PUSH DPL
MOV DPTR,#HEADER13
ACALL OUT_CHAR
MOV DPTR,#HEADER14
ACALL OUT_CHAR

POP DPL
POP DPH
RET

;-----------------------------------------------------------------------------

PRT MESSAGE4:    PUSH DPH
PUSH DPL
MOV DPTR,#HEADER15
ACALL OUT_CHAR
MOV DPTR,#HEADER16
ACALL OUT_CHAR
POP DPL
POP DPH
RET

;-----------------------------------

INIT_LCD:   PUSH DPH
PUSH DPL
PUSH PSW
PUSH ACC
MOV R0,#OFFH
ACALL DELAY_LOOP
MOV R0,#OFFH
ACALL DELAY_LOOP
MOV R0,#OFFH
ACALL DELAY_LOOP
MOV R0,#OFFH
ACALL DELAY_LOOP
MOV A,#0011000B
ACALL CTRL_OUT
MOV R0,#OFFH
ACALL DELAY_LOOP
MOV A,#0011000B
ACALL CTRL_OUT
MOV R0,#OFFH
ACALL DELAY_LOOP
MOV R0,#OFFH
ACALL DELAY_LOOP
MOV R0,#OFFH
ACALL DELAY_LOOP
MOV A,#0011000B
ACALL CTRL_OUT
MOV R0,#OFFH
ACALL DELAY_LOOP
MOV A,#0011000B
ACALL CTRL_OUT
MOV R0,#OFFH
ACALL DELAY_LOOP
MOV A,#0000001B
ACALL CTRL_OUT
MOV R0,#0FFH
ACALL DELAY_LOOP
MOV A,#00000110B
ACALL CTRL_OUT
POP ACC
POP PSW
POP DPL
POP DPH
RET

;-----------------------------------------------------------------------------------------
CLEAR_DISPLAY:
PUSH DPH
PUSH DPL
MOV A,#00000001B
ACALL CTRL_OUT
MOV R0,#0FFH
ACALL DELAY_LOOP
POP DPL
POP DPH
RET

;-----------------------------------------------------------------------------------------
DELAY_5S:
PUSH DPH
PUSH DPL
DEL3:
    MOV R5,#8H
    DJNZ R5,DEL3
POP DPL
POP DPH
RET

;-----------------------------------------------------------------------------------------
PRT_FAIL:
PUSH DPH
PUSH DPL
MOV DPTR,#FAIL1
ACALL OUT_CHAR
MOV DPTR,#FAIL2
ACALL OUT_CHAR
POP DPL
POP DPH
RET

;-----------------------------------------------------------------------------------------
HEADER1 DB 'MICROCONTROLLER'
HEADER2 DB 'DRIVEN '
HEADER3 DB 'TELEPHONE '
HEADER4 DB 'PROTECTOR '
HEADER5 DB 'DESIGNED BY: '
HEADER6 DB 'HIDAYAT SETIAWAN'
## Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply voltage $V_{DD}$, $V_{SS}$</td>
<td>$V_{DD}$</td>
<td>6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Voltage on any pin</td>
<td>$V_{SS}$</td>
<td>$-0.3$</td>
<td>$V_{DD}$</td>
<td>$0.3$</td>
</tr>
<tr>
<td>Current at any pin (other than supply)</td>
<td>$I_{O}$</td>
<td>$10$</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>$T_{A}$</td>
<td>$-40$</td>
<td>$+85$</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td></td>
<td>$-65$</td>
<td>$+150$</td>
<td>°C</td>
</tr>
<tr>
<td>Package power dissipation</td>
<td></td>
<td></td>
<td>$1000$</td>
<td>mW</td>
</tr>
</tbody>
</table>

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.*

*At above $15^\circ C$ at $36$ mV/°C, all leads soldered to board.*

## Recommended Operating Conditions

- Voltages are with respect to ground ($V_{SS}$) unless otherwise stated.

### Characteristics

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Positive Supply Voltages</td>
<td>$V_{DD}$</td>
<td>$5$</td>
<td></td>
<td>$5.25$</td>
<td>V</td>
</tr>
<tr>
<td>Oscillator Clock Frequency</td>
<td>$f_{c}$</td>
<td>$3.579545$</td>
<td>$92$</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>Oscillator Frequency Tolerance</td>
<td>$\Delta f_{c}$</td>
<td>$0.1$</td>
<td>$0.3$</td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>

*Typical figures are at $25^\circ C$ and are for design aid only. Not guaranteed and not subject to production testing.*

## DC Electrical Characteristics

- Voltages are with respect to ground ($V_{SS}$) unless otherwise stated.

### Characteristics

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating supply voltage</td>
<td>$V_{DD}$</td>
<td>$4.75$</td>
<td>$5$</td>
<td>$5.25$</td>
<td>V</td>
</tr>
<tr>
<td>Operating supply current</td>
<td>$I_{O}$</td>
<td>$30$</td>
<td>$90$</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Power consumption</td>
<td>$P_{D}$</td>
<td>$15$</td>
<td>$45$</td>
<td>mW</td>
<td></td>
</tr>
<tr>
<td>High level input voltage</td>
<td>$V_{IH}$</td>
<td>$3.5$</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Low level input voltage</td>
<td>$V_{IL}$</td>
<td>$1.5$</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input leakage current</td>
<td>$I_{IL}$</td>
<td>$0.1$</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Input leakage (source) current</td>
<td>$I_{OH}$</td>
<td>$2.5$</td>
<td>$15$</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Input impedance (N = -1, N = +1)</td>
<td>$R_{IN}$</td>
<td>$10$</td>
<td></td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>Steerling threshold voltage</td>
<td>$V_{SSL}$</td>
<td>$2.2$</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Low level output voltage</td>
<td>$V_{OL}$</td>
<td>$2.5$</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>High level output voltage</td>
<td>$V_{OH}$</td>
<td>$V_{DD}$</td>
<td>$0.03$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output low (sink) current</td>
<td>$I_{OL}$</td>
<td>$1$</td>
<td>$2.5$</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Output high (source) current</td>
<td>$I_{OH}$</td>
<td>$0.4$</td>
<td>$0.8$</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$V_{OUT}$ (sink) current</td>
<td>$I_{OUT}$</td>
<td>$2.4$</td>
<td>$2.7$</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$V_{OUT}$ (source) current</td>
<td>$R_{OH}$</td>
<td>$10$</td>
<td>$12$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Typical figures are at $25^\circ C$ and are for design aid only. Not guaranteed and not subject to production testing.*
Features

- Complete DTMF Receiver
- Low Power Consumption
- Internal Gain Setting Amplifier
- Adjustable Guard Time
- Central Office Quality

Applications

- Receiver System for British Telecom (BT) or CEPT Spec (MT8870B-1)
- Paging Systems
- Repeater Systems/Mobile Radio
- Credit Card Systems
- Remote Control
- Personal Computers

Description

The MT8870B/MT8870B-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated in Mitel's double poly ISO2-CMOS technology. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three-state bus interface.

Figure 1 - Functional Block Diagram
### Operating Characteristics

**Gain Setting Amplifier**

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input leakage current</td>
<td>I_{IN}</td>
<td>100</td>
<td></td>
<td></td>
<td>nA</td>
<td>V_{SS} ≤ V_{IN} ≤ V_{DD}</td>
</tr>
<tr>
<td>Input resistance</td>
<td>R_{IN}</td>
<td>10</td>
<td></td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>Input offset voltage</td>
<td>V_{OS}</td>
<td>25</td>
<td></td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Power supply rejection</td>
<td>PSRR</td>
<td>60</td>
<td></td>
<td></td>
<td>dB</td>
<td>1 kHz</td>
</tr>
<tr>
<td>Common mode rejection</td>
<td>CMRR</td>
<td>60</td>
<td></td>
<td></td>
<td>dB</td>
<td>-3.0V ≤ V_{IN} ≤ 3.0V</td>
</tr>
<tr>
<td>DC open loop voltage gain</td>
<td>A_{VOL}</td>
<td>65</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Open loop unity gain bandwidth</td>
<td>f_C</td>
<td>1.5</td>
<td></td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>Output voltage swing</td>
<td>V_{O}</td>
<td>4.5</td>
<td></td>
<td></td>
<td>V</td>
<td>V_{PP} ≥ 100kΩ to V_{SS}</td>
</tr>
<tr>
<td>Maximum capacitive load (GS)</td>
<td>C_L</td>
<td>100</td>
<td></td>
<td></td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Maximum resistive load (GS)</td>
<td>R_L</td>
<td>50</td>
<td></td>
<td></td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>Common mode range</td>
<td>V_{CM}</td>
<td>3.0</td>
<td></td>
<td></td>
<td>V</td>
<td>No Load</td>
</tr>
</tbody>
</table>

### MT8870B AC Electrical Characteristics

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Valid input signal levels (each tone of composite signal)</td>
<td>-29</td>
<td>27.5</td>
<td></td>
<td></td>
<td>dBm</td>
<td>1,2,3,5,6,9</td>
</tr>
<tr>
<td>Positive twist accept</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>dB</td>
<td>2,3,6,9</td>
</tr>
<tr>
<td>Negative twist accept</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>dB</td>
<td>2,3,6,9</td>
</tr>
<tr>
<td>Freq. deviation accept</td>
<td>± 1.5% ± 2 Hz</td>
<td>Nom.</td>
<td></td>
<td></td>
<td>%</td>
<td>2,3,5,9</td>
</tr>
<tr>
<td>Freq. deviation reject</td>
<td>± 3.5%</td>
<td>Nom.</td>
<td></td>
<td></td>
<td>%</td>
<td>2,3,5,9</td>
</tr>
<tr>
<td>Third tone tolerance</td>
<td>-16</td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
<td>2,3,4,5,9</td>
</tr>
<tr>
<td>Noise tolerance</td>
<td>-12</td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
<td>2,3,4,5,7,9,10</td>
</tr>
<tr>
<td>Dial tone tolerance</td>
<td>± 22</td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
<td>2,3,4,5,8,9,11</td>
</tr>
</tbody>
</table>

1. V_{DD} = 5 V, V_{SS} = 0 V, T_A = 25°C and f_L = 379545 Hz using test circuit shown in Figure 2

**Notes**

1. dBm = decibels above or below a reference power of 1 mW into a 600 Ohm load
2. Digit sequence consists of all DTMF tones
3. Tone duration = 40 ms, tone pause = 40 ms
4. Signal condition consists of nominal DTMF frequencies
5. Both tones in composite signal have an equal amplitude
6. Tone pair is deviated by ± 1.5% ± 2 Hz
7. Bandwidth limited (3 kHz) Gaussian noise
8. The precise deviation frequencies are (350 Hz and 440 Hz) ± 2 Hz
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal
11. Referenced to the minimum valid accept level
### MT8870B-1 AC Electrical Characteristics

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Signal conditions</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>Valid input signal levels (each tone of composite signal)</td>
<td>-31</td>
<td>21.8</td>
<td>+1</td>
<td>1, 2, 3, 5, 6, 9</td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>Valid input signal levels (each tone of composite signal)</td>
<td>869</td>
<td>1, 2, 3, 5, 6, 9</td>
<td></td>
<td></td>
<td>mVpp</td>
<td></td>
</tr>
<tr>
<td>2. Input Signal Level Reject</td>
<td>-37</td>
<td>10.9</td>
<td></td>
<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>Positive twist accept</td>
<td></td>
<td>6</td>
<td></td>
<td></td>
<td>dB</td>
<td>2.3, 6, 9</td>
</tr>
<tr>
<td>Negative twist accept</td>
<td></td>
<td>6</td>
<td></td>
<td></td>
<td>dB</td>
<td>2.3, 6, 9</td>
</tr>
<tr>
<td>5. Freq. deviation accept</td>
<td></td>
<td></td>
<td>±1.5% ± 2 Hz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6. Freq. deviation reject</td>
<td></td>
<td></td>
<td>±3.5%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7. Third tone tolerance</td>
<td></td>
<td></td>
<td>-18.5</td>
<td></td>
<td>dB</td>
<td>2.3, 4, 5, 9, 12</td>
</tr>
<tr>
<td>8. Noise tolerance</td>
<td></td>
<td></td>
<td>-12</td>
<td></td>
<td>dB</td>
<td>2.3, 4, 5, 7, 9, 10</td>
</tr>
<tr>
<td>9. Dial tone tolerance</td>
<td></td>
<td></td>
<td>+22</td>
<td></td>
<td>dB</td>
<td>2.3, 4, 5, 8, 9, 11</td>
</tr>
</tbody>
</table>

† $V_{DD} = 5\, V, V_{SS} = 0\, V, T_a = 25^\circ\, C$ and $f_c = 3,795\, 45\, MHz$ using test circuit shown in Figure 2.

**Notes:**
1. 2dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration = 40 ms, tone pause = 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5% ± 2 Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are 350 Hz and 440 Hz ± 2%.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Referenced to Fig. 10 Input DTMF Tone Level at -25 dBm (-28 dBm at GS Pin) interference frequency Range between 400-3400 Hz.
### AC Electrical Characteristics

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tone present detect time</td>
<td>TPD</td>
<td>5</td>
<td>11</td>
<td>14</td>
<td>ms</td>
<td>see Figure 3</td>
</tr>
<tr>
<td>Tone absent detect time</td>
<td>TPA</td>
<td>0.5</td>
<td>4</td>
<td>8.5</td>
<td>ms</td>
<td>see Figure 3</td>
</tr>
<tr>
<td>Tone duration accept</td>
<td>TREC</td>
<td></td>
<td></td>
<td></td>
<td>ms</td>
<td>User adjustable</td>
</tr>
<tr>
<td>Tone duration reject</td>
<td>TREC</td>
<td></td>
<td></td>
<td></td>
<td>ms</td>
<td>User adjustable</td>
</tr>
<tr>
<td>Interdigit pause accept</td>
<td>ID</td>
<td></td>
<td></td>
<td></td>
<td>ms</td>
<td>User adjustable</td>
</tr>
<tr>
<td>Interdigit pause reject</td>
<td>ID</td>
<td></td>
<td></td>
<td></td>
<td>ms</td>
<td>User adjustable</td>
</tr>
<tr>
<td>Propagation delay (S1 to Q)</td>
<td>TPU</td>
<td>8</td>
<td>11</td>
<td></td>
<td>μs</td>
<td>TOE = VDD</td>
</tr>
<tr>
<td>Propagation delay (S1 to S1D)</td>
<td>TPSD</td>
<td>12</td>
<td></td>
<td></td>
<td>μs</td>
<td>TOE = VDD</td>
</tr>
<tr>
<td>Output data set up (Q to S1D)</td>
<td>TOSD</td>
<td>3.4</td>
<td></td>
<td></td>
<td>μs</td>
<td>TOE = VDD</td>
</tr>
<tr>
<td>Propagation delay (TOE to Q ENABLE)</td>
<td>TTE</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
<td>RL = 10KΩ, CL = 50 pF</td>
</tr>
<tr>
<td>Propagation delay (TOE to Q DISABLE)</td>
<td>TTO</td>
<td>300</td>
<td></td>
<td></td>
<td>ns</td>
<td>RL = 10KΩ, CL = 50 pF</td>
</tr>
<tr>
<td>Crystal/clock frequency</td>
<td>fC</td>
<td>3.5759</td>
<td>3.5755</td>
<td>3.5831</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>Clock input rise time</td>
<td>tHCLS</td>
<td>110</td>
<td></td>
<td></td>
<td>ns</td>
<td>Ext. clock</td>
</tr>
<tr>
<td>Clock input fall time</td>
<td>tLCLS</td>
<td>110</td>
<td></td>
<td></td>
<td>ns</td>
<td>Ext. clock</td>
</tr>
<tr>
<td>Clock input duty cycle</td>
<td>DCC</td>
<td>40</td>
<td>50</td>
<td>60</td>
<td>%</td>
<td>Ext. clock</td>
</tr>
<tr>
<td>Capacitive load (OSC2)</td>
<td>C1O</td>
<td></td>
<td></td>
<td></td>
<td>μF</td>
<td></td>
</tr>
</tbody>
</table>

*VDD = 5.0V, VSS = 0V, T_a = 25°C and f_c = 3.579545 MHz. Using test circuit shown in Figure 2.*

*Typical figures are at 25°C and are for design and only not guaranteed and not subject to production testing.*

---

**Figure 2 - Single-Ended Input Configuration**
<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IN+</td>
<td>Non-Inverting Op-Amp (Input).</td>
</tr>
<tr>
<td>2</td>
<td>IN−</td>
<td>Inverting Op-Amp (Input).</td>
</tr>
<tr>
<td>3</td>
<td>GS</td>
<td>Gain Select. Gives access to output of front end differential amplifier for connection of feedback resistor.</td>
</tr>
<tr>
<td>4</td>
<td>V_{\text{Ref}}</td>
<td>Reference Voltage (Output). Nominally V_{DD}/2 is used to bias inputs at mid-rail (see Fig. 2).</td>
</tr>
<tr>
<td>5</td>
<td>IC</td>
<td>Internal Connection. Must be tied to V_{SS}.</td>
</tr>
<tr>
<td>6</td>
<td>IC</td>
<td>Internal Connection. Must be tied to V_{SS}.</td>
</tr>
<tr>
<td>7</td>
<td>OSC1</td>
<td>Clock (Input)</td>
</tr>
<tr>
<td>8</td>
<td>OSC2</td>
<td>Clock (Output): A 3.579545 MHz crystal connected between pins OSC1 and OSC2 completes the internal oscillator circuit.</td>
</tr>
<tr>
<td>9</td>
<td>V_{SS}</td>
<td>Negative Power Supply (Input).</td>
</tr>
<tr>
<td>10</td>
<td>TOE</td>
<td>Three State Output Enable (Input). Logic high enables the outputs Q1-Q4. This pin is pulled up internally.</td>
</tr>
<tr>
<td>11-14</td>
<td>Q1-Q4</td>
<td>Three State Data (Output). When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1). When TOE is logic low, the data outputs are high impedance.</td>
</tr>
<tr>
<td>15</td>
<td>STD</td>
<td>Delayed Steering (Output). Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on SUGT falls below V_{SS}.</td>
</tr>
<tr>
<td>16</td>
<td>EST</td>
<td>Early Steering (Output). Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause EST to return to a logic low.</td>
</tr>
<tr>
<td>17</td>
<td>SUGT</td>
<td>Steering Input/Guard time (Output) Bidirectional. A voltage greater than V_{SS} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{SS} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of EST and the voltage on St.</td>
</tr>
<tr>
<td>18</td>
<td>V_{DD}</td>
<td>Positive power supply (Input).</td>
</tr>
</tbody>
</table>
80C51BH/80C31BH

CHMOS SINGLE CHIP 8-BIT MICROCOMPUTER
60C51BH—4 KBYTE OF FACTORY MASK-PROGRAMMABLE ROM
60C31BH—CPU WITH RAM AND I/O

- 80C51BH/80C31BH — 3.5 to 12 MHz, VCC = 5V ±20%
- 80C51BH-1/80C31BH-1 — 3.5 to 16 MHz, VCC = 5V ±20%
- 80C51BH-2/80C31BH-2 — 0.5 to 12 MHz, VCC = 5V ±20%

- Power Control Modes
- 128 x 8-Bit RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- 64K Program Memory Space
- 64K Data Memory Space

- High Performance CHMOS Process
- Boolean Processor
- 5 Interrupt Sources
- Programmable Serial Port
- 'ONCE™ (On-Circuit Emulation) Mode

The MCS-51 CHMOS products are fabricated on Intel's CHMOS III process and are functionally compatible with the standard MCS-51 HMOS and EPROM products: CHMOS III is a technology which combines the high speed and density characteristics of HMOS with the low power attributes of CHMOS. This combination expands the effectiveness of the powerful MCS-51 architecture and instruction set.

Like the MCS-51 HMOS versions, the MCS-51 CHMOS products have the following features: 4 Kbyte of ROM (80C51BH/80C51BH-1/80C51BH-2 only); 128 bytes of RAM; 32 I/O lines; two 16-bit timer/counters; a 5-source two-level interrupt structure; a full-duplex serial port; and on-chip oscillator and clock circuitry. In addition, the MCS-51 CHMOS products have two software selectable modes of reduced activity for further power reduction—Idle and Power Down.

The Idle mode freezes the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.
The ONCETM Mode

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 80C51BH/80C31BH without removing the device from the circuit. The ONCE Mode is invoked by:

1. Pull ALE low while the device is in reset and PSEN is high.
2. Hold ALE low as RST is deactivated.

PACKAGES

<table>
<thead>
<tr>
<th>Part</th>
<th>Prefix</th>
<th>Package Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>80C51BH/80C31BH*</td>
<td>P</td>
<td>40-Pin Plastic DIP</td>
</tr>
<tr>
<td></td>
<td>D</td>
<td>40-Pin CERDIP</td>
</tr>
<tr>
<td></td>
<td>N</td>
<td>44-Pin PLCC</td>
</tr>
<tr>
<td></td>
<td>S</td>
<td>44-Pin QFP</td>
</tr>
</tbody>
</table>

*The 80C51BH-1, 80C51BH-2, 80C31BH-1, and 80C31BH-2 have the same package types.
Notice: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Ambient Temperature Under Bias: -40°C to +70°C
Storage Temperature: -65°C to +150°C

Voltage on any Pin to VSS: -0.5V to VCC +0.5V
Voltage on VCC to VSS: -0.5V to 6.5V
Maximum IOL per I/O pin: 15 mA
Power Dissipation: 1.0W

*This value is based on the maximum allowable die temperature and the thermal resistance of the package.

Operating Conditions:

TA (under Bias) = 0°C to +70°C; VCC = 5V ±20%; VSS = 0V

D.C. CHARACTERISTICS (under Operating Conditions)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL1</td>
<td>Input Low Voltage (Except XTAL1, RST)</td>
<td>-0.5</td>
<td></td>
<td>0.2 VCC +0.1</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>VIL2</td>
<td>Input Low Voltage (Except XTAL1, RST)</td>
<td>-0.5</td>
<td></td>
<td>0.2 VCC +0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VIH1</td>
<td>Input High Voltage (Except XTAL1, RST)</td>
<td>0.2 VCC + 0.9</td>
<td>VCC + 0.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIH2</td>
<td>Input High Voltage (XTAL1, RST)</td>
<td>0.7 VCC</td>
<td>VCC + 0.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOH1</td>
<td>Output High Voltage (Port 0, ALE, PSEN)</td>
<td>2.4</td>
<td></td>
<td>0.75 VCC</td>
<td>V</td>
<td>IOL = 16 mA (1)</td>
</tr>
<tr>
<td>VOH2</td>
<td>Output High Voltage (Port 0 in External Bus Mode)</td>
<td>2.4</td>
<td></td>
<td>0.9 VCC</td>
<td>V</td>
<td>IOL = 3.2 mA (1)</td>
</tr>
<tr>
<td>VOH3</td>
<td>Output High Voltage (Port 0 in External Bus Mode)</td>
<td>0.75 VCC</td>
<td></td>
<td>0.9 VCC</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IOH1</td>
<td>Logical 0 Input Current (Port 1, 2, 3)</td>
<td>0.5</td>
<td></td>
<td>10 µA</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>IOH2</td>
<td>Logical 1 to 0 Transition Current (Port 1, 2, 3)</td>
<td>650</td>
<td></td>
<td>2000 µA</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>IL1</td>
<td>Input Leakage Current (Port 0, EA)</td>
<td>±10</td>
<td></td>
<td>4.5 µA</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>RST</td>
<td>Reset Pulldown Resistor</td>
<td>50</td>
<td></td>
<td>150 KΩ</td>
<td>KΩ</td>
<td></td>
</tr>
<tr>
<td>CIO</td>
<td>Pin Capacitance</td>
<td>10</td>
<td></td>
<td>10 pF</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>IOC</td>
<td>Power Supply Current: Active Mode, 12 MHz</td>
<td>11</td>
<td></td>
<td>20 mA</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Idle Mode, 12 MHz</td>
<td>1.7</td>
<td></td>
<td>6.5 mA</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Power Down Mode</td>
<td>5</td>
<td></td>
<td>50 µA</td>
<td>µA</td>
<td></td>
</tr>
</tbody>
</table>

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Operating Conditions:

TA (under Bias) = 0°C to +70°C; VCC = 5V ±20%; VSS = 0V
1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VCC of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.9 V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.

2. Capacitive loading on Ports 0 and 2 may cause the VCC on ALE and PSEN to momentarily fall below the 0.9 VCC specification when the address bits are stabilizing.

3. "Typicals" are based on a limited number of samples taken from early manufacturing lots and are not guaranteed. The values listed are at room temperature, 5V.

4. ICCMAX at other frequencies is given by:
   - Active Mode: $\text{ICCMAX} = 0.47 \times \text{FREQ} + 2.35 \text{mA}$
   - Idle Mode: $\text{ICCMAX} = 0.33 \times \text{FREQ} + 1.05 \text{mA}$
   where FREQ is the external oscillator frequency in MHz. ICCMAX is given in mA. See Figure 5.

5. See Figures 6 through 8 for ICC test conditions. Minimum VCC for Power Down is 2V.

6. Under steady state (non-transient) conditions, ICC must be externally limited as follows:
   - Maximum $I_{CC}$ per port pin: 10 mA
   - Maximum $I_{CC}$ per 8-bit port: 70 mA
   - Port 0: 20 mA
   - Port 1, 2, and 3: 15 mA

7. Maximum total $I_{CC}$ for all output pins: 71 mA

If $I_{CC}$ exceeds the test condition, $V_{CC}$ may exceed the minimum specification. Pins are not guaranteed to sink current greater than the listed test conditions.

---

Figure 5. ICC vs. Frequency
Valid only within frequency specifications of the device under test.

Figure 6. ICC Test Condition, Active Mode
All other pins are disconnected. Refers to the test condition given in Figures 5 and 6.

Figure 7. ICC Test Condition, Idle Mode
All other pins are disconnected.
National Semiconductor

LM2901/LM339J Low Power Low Offset Voltage
Quad Comparators

General Description
The LM139 series consists of four independent precision
voltage comparators with an offset voltage specification as
low as 2 mV max for all four comparators. These were de-
signed specifically to operate from a single power supply
over a wide range of voltages. Operation from split power
supplies is also possible and the low power supply current
drain is independent of the magnitude of the power supply
voltage. These comparators also have a unique characteris-
tic in that the input common-mode voltage range includes
ground, even though operated from a single power supply
voltage.

Application areas include limit comparators; pulse, squarewave and time delay gener-
ators; wide range VCO; MOS clock timers; multivibrators
and high voltage digital logic gates. The LM139 series was
designed to directly interface with TTL and CMOS. When
operated from both plus and minus power supplies, they will
directly interface with MOS logic—where the low power
drain of the LM339 is a distinct advantage over standard
comparators.

Advantages
• High precision comparators
• Reduced Vos drift over temperature

Features
• Wide single supply voltage range of dual supplies
  LM139 series: 2 Vdc to ±6 Vdc or
  LM139A series, LM2901
  ±1 Vdc to ±18 Vdc
  LM339J: 2 Vdc to ±25 Vdc
  or ±1 Vdc to ±14 Vdc
• Very low supply current drain (2.8 mA) — independent
  of supply voltage
• Low input biasing current
  25 nA
• Low input offset current
  ±5 nA
• Low input offset voltage
  ±3 mV
• Input common-mode voltage range includes GND
• Differential input voltage range equal to the power
  supply voltage
• Low output saturation voltage
  250 mV at 4 mA
• Output voltage compatible with TTL, ECL, MOS
  and CMOS logic systems

Schematic and Connection Diagrams

Dual-in-Line Package

Order Number LM139J, LM139AJ, LM239J, LM239AJ,
See NS Package Number J14A

Order Number LM339AM, LM339M or LM2901M
See NS Package Number M14A

Order Number LM339H, LM339AH,
LM2901H or LM3302H
See NS Package Number H14A
### Absolute Maximum Ratings

If military/aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 10)

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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage, $V^+$</td>
<td>36 V_{OC} or ±18 V_{OC}</td>
<td>28 V_{OC} or ±14 V_{OC}</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>36 V_{OC}</td>
<td>28 V_{OC}</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage</td>
<td>-0.3 V_{OC} to +0.3 V_{OC}</td>
<td>-0.3 V_{OC} to +0.3 V_{OC}</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>Operating Temperature Range</td>
<td>-40°C to +85°C</td>
<td>0°C to +70°C</td>
<td>25°C to +85°C</td>
<td>-40°C to +85°C</td>
<td>-55°C to +125°C</td>
</tr>
<tr>
<td>Power Dissipation (Note 1)</td>
<td>Dual-In-Line Package</td>
<td>1050 mW</td>
<td>1050 mW</td>
<td>0°C to +70°C</td>
<td>25°C to +85°C</td>
<td>0°C to +85°C</td>
</tr>
<tr>
<td>Molded DIP</td>
<td>1190 mW</td>
<td>760 mW</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cavity Dip</td>
<td>1050 mW</td>
<td>760 mW</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Small Outline Package</td>
<td>Continuous</td>
<td>Continuous</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Soldering Information</td>
<td>Continuous</td>
<td>Continuous</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead Temperature</td>
<td>-55°C to +125°C</td>
<td>-55°C to +125°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Soldering, 10 seconds</td>
<td>Continuous</td>
<td>Continuous</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ESD Rating</td>
<td>1.5 kV in series with 100 pf</td>
<td>600V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Electrical Characteristics ($V^+ = 5$ V, $T_A = 25$°C, unless otherwise stated)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Offset Voltage</td>
<td>(Note 9)</td>
<td>±1.0</td>
<td>±2.0</td>
<td>±1.0 ±2.0</td>
<td>±2.0</td>
<td>±5.0</td>
<td>±2.0</td>
<td>±5.0</td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>$I_{OC(+)}$ or $I_{OC(-)}$ with OutPut in Linear Range, (Note 5), $V_{OC} = 0$</td>
<td>25</td>
<td>100</td>
<td>25 ±50</td>
<td>25</td>
<td>100</td>
<td>25</td>
<td>100</td>
</tr>
<tr>
<td>Input Offset Current</td>
<td>$I_{OC(+) - I_{OC(-)}}, V_{OC} = 0$</td>
<td>±3.0</td>
<td>±2.5</td>
<td>±3.0 ±2.5</td>
<td>±3.0</td>
<td>±50</td>
<td>±3.0</td>
<td>±50</td>
</tr>
<tr>
<td>Input Common-Mode Voltage Range</td>
<td>$V^+ = 30$ V (LM3302), $V^+ = 20$ V (Note 9)</td>
<td>0</td>
<td>V^+ ±1.5</td>
<td>0  V^+ ±1.5</td>
<td>0  V^+ ±1.5</td>
<td>0  V^+ ±1.5</td>
<td>0  V^+ ±1.5</td>
<td></td>
</tr>
<tr>
<td>Supply Current</td>
<td>$R_L = \infty$ on all Comparators, $R_I = \infty, V^+ = 5$ V, (LM3302, $V^+ = 20$ V)</td>
<td>0.8</td>
<td>2.0</td>
<td>0.8 ±2.0</td>
<td>0.8</td>
<td>2.0</td>
<td>0.8</td>
<td>2.0</td>
</tr>
<tr>
<td>Voltage Gain</td>
<td>$R_L \geq 15$ kΩ, $V^+ = 15$ V, $V_{OC} = 1$ V or 11 V</td>
<td>50</td>
<td>200</td>
<td>50 ±200</td>
<td>50</td>
<td>200</td>
<td>50</td>
<td>200</td>
</tr>
<tr>
<td>Large Signal Response Time</td>
<td>$V_{IN} = \text{TTL Logic Swing}, V_{IN} = 3.3$ V, $V_{HI} = 5$ V, $V_{IL} = 5.1$ kΩ</td>
<td>300</td>
<td>300</td>
<td>300</td>
<td>300</td>
<td>300</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>Response Time</td>
<td>$V_{RL(+) = 6}$ V, $R_L = 6$ kΩ, (Note 7)</td>
<td>1.3</td>
<td>1.3</td>
<td>1.3</td>
<td>1.3</td>
<td>1.3</td>
<td>1.3</td>
<td>1.3</td>
</tr>
<tr>
<td>Output Sink Current</td>
<td>$V_{IN(-)} = 1$ V, $V_{IN(+)} = 0$, $V_{DO} \leq 15$ V</td>
<td>6.0</td>
<td>16.0</td>
<td>6.0 ±16</td>
<td>6.0</td>
<td>16.0</td>
<td>6.0</td>
<td>16.0</td>
</tr>
<tr>
<td>Parameter</td>
<td>Conditions</td>
<td>LM139A</td>
<td>LM139A, LM330</td>
<td>LM139</td>
<td>LM2901</td>
<td>LM3302</td>
<td></td>
<td></td>
</tr>
<tr>
<td>-------------------------------</td>
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<td>--------</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>Saturation Voltage</td>
<td>$V_{IN}(-) = 1, V_{OC}$, $V_{IN}(+) = 0$, $I_{SATE} \leq 4, mA$</td>
<td>250</td>
<td>400</td>
<td></td>
<td>250</td>
<td>400</td>
<td></td>
<td>250</td>
</tr>
<tr>
<td>Output Leakage Current</td>
<td>$V_{IN}(-) = 1, V_{OC}$, $V_{IN}(+) = 0$, $V_{O} = 5, V_{OC}$</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
</tr>
</tbody>
</table>

**Electrical Characteristics** ($V^+ = 5\, V_{OC}$, $T_A = 25\, ^\circ C$, unless otherwise stated) (Continued)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>LM139A</th>
<th>LM139A, LM330</th>
<th>LM139</th>
<th>LM2901</th>
<th>LM3302</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
<td>Typ</td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>(Note 6)</td>
<td>-2.40</td>
<td>-1.40</td>
<td>-0.90</td>
<td>9.00</td>
<td>9.00</td>
</tr>
<tr>
<td>Input Offset Current</td>
<td>$I_{IN}(-) - I_{IN}(+) = V_{CM} = 0V$</td>
<td>2.100</td>
<td>1.500</td>
<td>1.000</td>
<td>1.500</td>
<td>1.500</td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>$I_{IN}(-) = I_{IN}(+)$ with Output in Linear Range, $V_{CM} = 0V$</td>
<td>300</td>
<td>400</td>
<td>400</td>
<td>400</td>
<td>500</td>
</tr>
<tr>
<td>Input Common-Mode Voltage Range</td>
<td>$V^+ = 30, V_{OC}$ ($LM3302$, $V^+ = 28, V_{OC}$) (Note 8)</td>
<td>0</td>
<td>$V^+ - 2.0$</td>
<td>0</td>
<td>$V^+ - 2.0$</td>
<td>0</td>
</tr>
<tr>
<td>Saturation Voltage</td>
<td>$I_{SAT} = 1, V_{OC}$, $I_{SAT} = 0$, $I_{SATE} \leq 4, mA$</td>
<td>700</td>
<td>700</td>
<td>700</td>
<td>700</td>
<td>700</td>
</tr>
<tr>
<td>Output Leakage Current</td>
<td>$I_{OUT}(-) = 1, V_{OC}$, $I_{OUT}(+) = 0$, $V_{O} = 28, V_{OC}$</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>Keep all $V_{IN} \geq 0, V_{OC}$ (or $V^-$)</td>
<td>36</td>
<td>36</td>
<td>36</td>
<td>36</td>
<td>36</td>
</tr>
</tbody>
</table>

**Note**: For operating at high temperatures, the LM339/LM339A/LM2901/LM3302 may be derated based on a 125°C maximum junction temperature and a thermal resistance of 89°C/W which applies for the device soldered in a printed circuit board, operating in a still air environment. The LM329 and LM139A must be derated based on a 100°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the output keeps the chip dissipation very small (50 mW or less), provided the output transistors are allowed to saturate.

**Note 2**: Short circuits from the output to $V^+$ can cause excessive heating and eventual destruction. When connecting short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of $V^+$.

**Note 3**: This current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input bipolar transistors becoming forward biased and thereby acting as input diodes.

**Note 4**: In this diode action, there is also lateral PNP parasitic transistor action on the IC output. This transistor action can cause the output voltages of the comparators to go to the $V^+$ voltage level (or to ground for a reverse bias) for the time duration that an input becomes negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $\pm 0.3\, V_{OC}$ at 25°C.

**Note 5**: These specifications are limited to $-55\, ^\circ C \leq T_A \leq +125\, ^\circ C$, for the LM139A LM139A. With the LM339A/LM3302, all temperature specifications are limited to $-25\, ^\circ C \leq T_A \leq +85\, ^\circ C$, the LM339A/LM3302, temperature specifications are limited to $0\, ^\circ C \leq T_A \leq +70\, ^\circ C$, and the LM2901/LM3302 temperature range is $-40\, ^\circ C \leq T_A \leq +80\, ^\circ C$.

**Note 6**: The results of the input current is at the output of the input stage. This current is essentially constant, independent of the state of the output so no power change exists to the reference or input lines.

**Note 7**: The direction of the input current is out of the chip due to the PNP input stage. This current is essentially constant, independent of the state of the output so no power change exists to the reference or input lines.

**Note 8**: The input common-mode voltages of either input signal voltage should not be allowed to go negative by more than $0.2\, V_{OC}$. The upper and lower common-mode voltage ranges are $V^+ = -0.5\, V_{OC}$ at 25°C, but either or both inputs can go to $± 30\, V_{OC}$ without damage $25\, ^\circ C$ for LM3302, independent of the magnitude of $V^+$.

**Note 9**: The response time specified is a 100 mV input step with a 1 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

**Note 10**: Positive or negative input overvoltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\, V_{OC}$ for 0.3 mA below the magnitude of the negative power supply, it will exceed at 25°C.

**Note 11**: The input offset voltage, $V_{O} = 1.4\, V_{OC}$, $V_{O} = 0$ with $V^+$ from 0 V to $30\, V_{OC}$ and over the full input common-mode range (0 V to $V^+$ = $1\, V_{OC}$ at 25°C). For LM339A, $V^+$ from 0 V to 30 VDC.
Typical Performance Characteristics

Supply Current

- $I_{CC}$ vs. $V_{CC}$ for $T_{A} = -40^\circ C$, $T_{A} = +85^\circ C$

Input Current

- $I_{I}$ vs. $V_{I}$ for $T_{A} = -40^\circ C$, $T_{A} = +85^\circ C$

Output Saturation Voltage

- $V_{O}$ vs. $I_{O}$ for $T_{A} = -40^\circ C$, $T_{A} = +85^\circ C$

Response Time for Various Input Overdrive—Negative Transition

- $\tau_{rise}$ vs. $V_{O}$ for $T_{A} = -40^\circ C$, $T_{A} = +85^\circ C$

Response Time for Various Input Overdrive—Positive Transition

- $\tau_{fall}$ vs. $V_{O}$ for $T_{A} = -40^\circ C$, $T_{A} = +85^\circ C$

Typical Performance Characteristics

Supply Current

- $I_{CC}$ vs. $V_{CC}$ for $T_{A} = -40^\circ C$, $T_{A} = +85^\circ C$

Input Current

- $I_{I}$ vs. $V_{I}$ for $T_{A} = -40^\circ C$, $T_{A} = +85^\circ C$

Output Saturation Voltage

- $V_{O}$ vs. $I_{O}$ for $T_{A} = -40^\circ C$, $T_{A} = +85^\circ C$

Response Time for Various Input Overdrive—Negative Transition

- $\tau_{rise}$ vs. $V_{O}$ for $T_{A} = -40^\circ C$, $T_{A} = +85^\circ C$

Response Time for Various Input Overdrive—Positive Transition

- $\tau_{fall}$ vs. $V_{O}$ for $T_{A} = -40^\circ C$, $T_{A} = +85^\circ C$