EQU 3000H
EQU 3001H
EQU 3002H
EQU 3003H
EQU 1000H
EQU 1001H
EQU 1002H
EQU 1003H
EQU 30H
EQU 31H
EQU 32H
EQU 33H
EQU 34H
EQU 35H
EQU 36H
EQU 37H
EQU 38H
EQU 39H
EQU 41H
EQU 42H
EQU 43H
EQU 44H
EQU 45H
EQU 46H
ORG 100
AJMP MAIN
ORG 0003H
AJMP ISR_0
ORG 100H
CLR RS0
CLR RS1
MOV SP,#70H
ACALL INIT_LCD
ACALL INIT_PPI

ACALL PRT_TITLE
ACALL DELAY_5S
ACALL CLEAR_DISPLAY

ACALL PRT_TITLE2
ACALL DELAY_5S
ACALL CLEAR_DISPLAY

ACALL THRESHOLD_SETTING
ACALL TRIP_SETTING
ACALL READ_ADC
ACALL FAIL_DETECT ; BUFFER1,2,3 > THRESHOLD
ACALL OUTPUT
SJMP D
OLD_SETTING: PUSH DPH
PUSH DPL

ACALL PRT_DIR
MOV INPUT,THRESHOLD
ACALL HEX2BCD

.IN:
ACALL THRESHOLD_RESULT
ACALL BCD2HEX1
ACALL THRESHOLD_DISPLAY

ACALL DELAY_1S
MOV A, KEY_TEST
CJNE A, #0Fh, DO_AGAIN
MOV KEY_TEST, #1

POP DPL
POP DPH
RET

SETTING:
PUSH DPH
PUSH DPL

ACALL PRT_TRIP_DIR
MOV INPUT, TIME_TRIP
ACALL HEX2BCD

AGAIN2:
ACALL TRIP_RESULT
MOV DIGIT3, #0
ACALL BCD2HEX2
ACALL TRIP_DISPLAY

ACALL DELAY_1S
MOV A, KEY_TEST
CJNE A, #0Fh, DO_AGAIN2
MOV KEY_TEST, #1

POP DPL
POP DPH
RET

PPI:
PUSH DPH
PUSH DPL
MOV DPTR, #CONTROL_REG
MOV A, #10001001B
MOVX @DPTR, A
POP DPL
POP DPH
RET

LCD:
PUSH DPH
PUSH DPL
ACALL DELAY_1S
MOV A, #00111000B
ACALL CTRL_OUT
ACALL DELAY_1S
MOV A, #00111000B
ACALL CTRL_OUT
ACALL DELAY_1S
MOV A, #00111000B
ACALL CTRL_OUT
MOV A, #00111000B
ACALL CTRL_OUT
MOV A, #00050100B
ACALL CTRL_OUT
MOV A, #00050100B
ACALL CTRL_OUT
MOV A, #0000001B
ACALL CTRL_OUT
MOV A, #00000110B
ACALL CTRL_OUT
POP DPL
POP DPH
RET

_DISPLAY: PUSH DPH
PUSH DPL
MOV A,#00000001B
ACALL CTRL OUT
ACALL DELAY_1S
POP DPL
POP DPH
RET

Y_5S:

PUSH DPH
PUSH DPL
PUSH ACC
PUSH PSW
MOV R5,#8H
MOV A,#OFFH
MOV B,#OFFH
DJNZ B,$
DJNZ ACC,DEL2
DJNZ R5,DEL3
POP PSW
POP ACC
POP DPL
POP DPH
RET

Y_2S:

PUSH DPH
PUSH DPL
PUSH ACC
PUSH PSW
MOV R5,#06H
MOV A,#OFFH
MOV B,#OFFH
DJNZ B,$
DJNZ ACC,DEL4
DJNZ R5,DEL3
POP PSW
POP ACC
POP DPL
POP DPH
RET

Y_1S:

PUSH DPH
PUSH DPL
PUSH ACC
PUSH PSW
MOV R5,#05H
MOV A,#0FH
MOV B,#02FH
DJNZ B,$
DJNZ ACC,DEL6
DJNZ R5,DEL5
POP PSW
POP ACC
POP DPL
POP DPH
RET

Y_11S:

PUSH DPH
PUSH DPL
PUSH ACC
PUSH PSW
MOV R5,#0FH
MOV A,#01FH
MOV B,#02FH
DJNZ B,$
DJNZ ACC, DEL68
DJNZ R5, DEL58
POP PSW
POP ACC
POP DPL
POP DPH
RET

;:
PUSH DPH
PUSH DPL
PUSH ACC
PUSH PSW
MOV R5, TIME_DELAY
MOV A, #OFFH
MOV B, #OFFH
DJNZ B, $
DJNZ ACC, DEL8
DJNZ R5, DEL7
POP PSW
POP ACC
POP DPL
POP DPH
RET

TITLE:
PUSH DPH
PUSH DPL
MOV R7, #1
ACALL LOCATE1
MOV DPTR, #HEADER1
ACALL OUT_CHAR
MOV R7, #1
ACALL LOCATE2
MOV DPTR, #HEADER2
ACALL OUT_CHAR
ACALL DELAY_5S
ACALL CLEAR_DISPLAY
MOV R7, #1
ACALL LOCATE1
MOV DPTR, #HEADER3
ACALL OUT_CHAR
MOV R7, #1
ACALL LOCATE2
MOV DPTR, #HEADER4
ACALL OUT_CHAR
ACALL DELAY_5S
ACALL CLEAR_DISPLAY
MOV R7, #1
ACALL LOCATE1
MOV DPTR, #BY1
ACALL OUT_CHAR
MOV R7, #1
ACALL LOCATE2
MOV DPTR, #BY2
ACALL OUT_CHAR
POP DPL
POP DPH
RET

TITLE2:
PUSH DPH
PUSH DPL
MOV R7, #1
ACALL LOCATE1
MOV DPTR, #HEADER7
ACALL OUT_CHAR
MOV R7, #1
ACALL LOCATE2
MOV DPTR, #HEADER8
ACALL OUT_CHAR
ACALL DELAY_5S
ACALL CLEAR_DISPLAY

POP DPL
POP DPH
RET

DIR:
PUSH DPH
PUSH DPL
MOV R7, #0
ACALL LOCATE1
MOV DPTR, #HEADER9
ACALL OUT_CHAR
MOV R7, #0
ACALL LOCATE2
MOV DPTR, #HEADER10
ACALL OUT_CHAR
ACALL DELAY_5S
ACALL DELAY_5S
ACALL CLEAR_DISPLAY

POP DPL
POP DPH
RET

HEX1:
PUSH DPH
PUSH DPL
CLR C
MOV R5, DIGIT2 ; d2
MOV B, R5
MOV A, #10
MUL AB
ADD A, DIGIT1 ; d1
ADD A, R2
MOV R6, A
MOV THRESHOLD, R6 ; OUTPUT IN THRESHOLD

POP DPL
POP DPH
RET

IVB1:
PUSH DPH
PUSH DPL
CLR C
MOV B, R5
MOV A, #100
MOV A, #100
MUL AB
ADD A, R3
MOV R3, A
```assembly
POP DPL
POP DPH
RET

SHOLD_DISPLAY:  PUSH DPH
                    PUSH DPL
                    MOV R7,#1
                    ACALL LOCATE1
                    MOV DPTR,#HEADER11
                    ACALL OUT_CHAR
                    MOV R7,#1
                    ACALL LOCATE2
                    MOV DPTR,#HEADER12
                    ACALL OUT_CHAR

                    POP DPL
                    POP DPH
                    RET

TRIP_DIR:  PUSH DPH
                    PUSH DPL
                    MOV R7,#0
                    ACALL LOCATE1
                    MOV DPTR,#HEADER13
                    ACALL OUT_CHAR
                    MOV R7,#0
                    ACALL LOCATE2
                    MOV DPTR,#HEADER14
                    ACALL OUT_CHAR

                    ACALL DELAY_5S
                    ACALL DELAY_5S
                    ACALL CLEAR_DISPLAY

                    POP DPL
                    POP DPH
                    RET

DISPLAY:  PUSH DPH
                    PUSH DPL

                    MOV R7,#1
                    ACALL LOCATE1
                    MOV DPTR,#HEADER15
                    ACALL OUT_CHAR
                    MOV R7,#1
                    ACALL LOCATE2
                    MOV DPTR,#HEADER16
                    ACALL OUT_CHAR

                    POP DPL
                    POP DPH
                    RET

DETECT:  PUSH DPH
                    PUSH DPL

                    CLR C

                    MOV A,BUFFER3
                    SUBB A,THRESHOLD
                    JC LOOP1
                    SETB TEST2
```
SJMP LOOP11

1:    ACALL PRT_R_FAIL
CLR TEST2

11:   CLR C

MOV A, BUFFER2
SUBB A, THRESHOLD
JC LOOP2
SETB TEST3
SJMP LOOP22

2:    ACALL PRT_S_FAIL
CLR TEST3

22:   CLR C

MOV A, BUFFER1
SUBB A, THRESHOLD
JC LOOP3
SETB TEST4
SJMP LOOP33

3:    ACALL PRT_T_FAIL
CLR TEST4

33:   POP DPL
POP DPH
RET

-----------------------------------
R_FAIL:
PUSH DPH
PUSH DPL

MOV R7, #1
ACALL LOCATE1
MOV DPTR, #R1
ACALL OUT_CHAR
MOV R7, #1
ACALL LOCATE2
MOV DPTR, #R2
ACALL OUT_CHAR
ACALL DELAY_5S

POP DPL
POP DPH
RET

-----------------------------------
S_FAIL:
PUSH DPH
PUSH DPL

MOV R7, #1
ACALL LOCATE1
MOV DPTR, #S1
ACALL OUT_CHAR
MOV R7, #1
ACALL LOCATE2
MOV DPTR, #S2
ACALL OUT_CHAR
ACALL DELAY_5S

POP DPL
POP DPH
RET
T_FAIL:
  PUSH DPH
  PUSH DPL
  MOV R7,#1
  ACALL LOCATE1
  MOV DPTR,#T1
  ACALL OUT_CHAR
  MOV R7,#1
  ACALL LOCATE2
  MOV DPTR,#T2
  ACALL OUT_CHAR
  ACALL DELAY_5S

  POP DPL
  POP DPH
  RET

TIME:
  PUSH DPH
  PUSH DPL
  MOV R7,#1
  ACALL LOCATE1
  MOV DPTR,#TIME1
  ACALL OUT_CHAR
  MOV R7,#1
  ACALL LOCATE2
  MOV DPTR,#TIME2
  ACALL OUT_CHAR
  ACALL DELAY_5S

  POP DPL
  POP DPH
  RET

_ADC:
  PUSH DPH
  PUSH DPL

_CH1:
  MOV DPTR,#PORT_A
  MOV A,#1111100B
  MO VX @DPTR,A

  MOV A,#1111000B
  MOVX @DPTR,A

_CH1:
  JBC FO,READ_ADC_CH1
  SJMP WAIT_CH1

_ADC_CH1:
  MOV A,P1
  MOV BUFFER1,A
  ACALL TOTAL_RESULT
  ACALL DELAY_2S

_CH2:
  MOV DPTR,#PORT_A
  MOV A,#11111101B
  MO VX @DPTR,A

  MOV A,#1111001B
  MOVX @DPTR,A

_CH2:
  JBC FO,READ_ADC_CH2
  SJMP WAIT_CH2

_ADC_CH2:
  MOV A,P1
  MOV BUFFER2,A
  ACALL TOTAL_RESULT2
  ACALL DELAY_2S
CH3:
  MOV DPTR,#PORT A
  MOV A,#11111110B
  MOVX @DPTR,A

  MOV A,#11111010B
  MOVX @DPTR,A

CH3:
  JBC FO,READ_ADC_CH3
  SJMP WAIT_CH3

ADC_CH3:
  MOV A,P1
  MOV BUFFER3,A
  ACALL TOTAL_RESULT3
  ACALL DELAY_2S

EXIT:
  POP DPL
  POP DPH
  RET

UT:
  PUSH DPH
  PUSH DPL

E_0:
  JB TEST2,STATE_1
  JB TEST3,STATE_1
  JB TEST4,STATE_1
  ACALL RELAY_OFF

E_1:
  JB TEST2,STATE_2
  JB TEST3,STATE_2
  JNB TEST4,STATE_2
  ACALL K3_ON
  ACALL TIMER_ON

E_2:
  JB TEST2,STATE_3
  JNB TEST3,STATE_3
  JB TEST4,STATE_3
  ACALL K2_ON
  ACALL TIMER_ON

E_3:
  JB TEST2,STATE_4
  JNB TEST3,STATE_4
  JNB TEST4,STATE_4
  ACALL K2_ON
  ACALL TIMER_ON

E_4:
  JNB TEST2,STATE_5
  JB TEST3,STATE_5
  JB TEST4,STATE_5
  ACALL K1_ON
  ACALL TIMER_ON

E_5:
  JNB TEST2,STATE_6
  JB TEST3,STATE_6
  JNB TEST4,STATE_6
  ACALL K1_ON
  ACALL TIMER_ON

E_6:
  JNB TEST2,STATE_7
  JNB TEST3,STATE_7
  JB TEST4,STATE_7
  ACALL K2_ON
  ACALL TIMER_ON
E_7:

JNB TEST2,OUTPUT_EXIT
JNB TEST3,OUTPUT_EXIT
JNB TEST4,OUTPUT_EXIT
ACALL K2_ON
MOV A, #0
ORL A, RELAY_BUFFER
MOV DPTR, #PORT_B
MOVX @DPTR, A

UT_EXIT:

POP DPL
POP DPH
RET

PB2=K3 PB3=MAIN

N:

PUSH DPH
PUSH DPL

MOV DPTR, #PORT_B
MOV A, #00000001B
MOV RELAY_BUFFER, A
MOVX @DPTR, A

POP DPL
POP DPH
RET

PB3=MAIN

N:

PUSH DPH
PUSH DPL

MOV DPTR, #PORT_B
MOV A, #00000010B
MOV RELAY_BUFFER, A
MOVX @DPTR, A

POP DPL
POP DPH
RET

PB1=K2

N:

PUSH DPH
PUSH DPL

MOV DPTR, #PORT_B
MOV A, #00000001B
MOV RELAY_BUFFER, A
MOVX @DPTR, A

POP DPL
POP DPH
RET

Y_OFF:

PUSH DPH
PUSH DPL

MOV DPTR, #PORT_B
MOV A, #0H
MOVX @DPTR, A

POP DPL
POP DPH
RET

R_ON:

PUSH DPH
PUSH DPL
MOV COUNTER_TIMER, TIME_TRIP

MOV TL1, #OH
MOV TH1, #OH
MOV TH0, #0FFH
MOV TL0, #0E5H
MOV TMOD, #01000001B ; T1 = Counter T0 = Timer

SETB TR0

N1:
JBC TEST1, AGAIN2
SJMP AGAIN1

N2:
CLR TR0
ACALL TR_TIME
ACALL READ_ADC
ACALL FAIL_DETECT ; BUFFER1, 2, 3 > THRESHOLD
JNB TEST2, GO_ON ; RESTORE SYSTEM
JNB TEST3, GO_ON
JNB TEST4, GO_ON
SJMP RESTORE

N:
DJNZ COUNTER_TIMER, SET_TIMER
SJMP FAIL ; SYSTEM DISABLE

Timer:
MOV TL0, #0D8H
MOV TH0, #0FFH
SETB TR0
SJMP AGAIN1

ORE:
LCALL PRT_RESTORE
MOV A, #0
ORL A, RELAY_BUFFER
MOV DPTR, #PORT_B
MOVX @DPTR, A
SJMP TIMER_EXIT

LCALL PRT_DISABLE
MOV DPTR, #PORT_B
MOV A, #00001000B ; PB3
ORL A, RELAY_BUFFER
MOVX @DPTR, A
ACALL DELAY_5S
ACALL DELAY_5S

MOV DPTR, #PORT_B
MOV A, #00000000B ; PB3
MOVX @DPTR, A

R_EXIT:
POP DPL
POP DPH
RET

R_0:
PUSH DPH
PUSH DPL
SETB TEST1
POP DPL
POP DPH
RETI

RESTORE:
PUSH DPH
**General Description**

The MAX114/MAX118 are microprocessor-compatible, 8-bit, 4-channel and 8-channel analog-to-digital converters (ADCs). They operate from a single +5V supply and use a half-flash technique to achieve a 660ns conversion time (1 Msps). A power-down (PWRDN) pin reduces current consumption typically to 1μA. The devices return from power-down mode to normal operating mode in less than 200ns, allowing large supply current reductions in burst-mode applications (in burst mode, the ADC wakes up from a low-power state at specified intervals to sample the analog input signals). Both converters include a track/hold, enabling the ADC to digitize fast analog signals.

Microprocessor (μP) interfaces are simplified because the ADC can appear as a memory location or I/O port without external interface logic. The data outputs use latched, three-state buffer circuitry for direct connection to an 8-bit parallel μP data bus or system input port. The MAX114/MAX118 input/reference configuration enables ratiometric operation.

The 4-channel MAX114 is available in a 24-pin DIP or SSOP. The 8-channel MAX118 is available in a 28-pin DIP or SSOP. For +3V applications, refer to the MAX113/MAX117 data sheet.

**Features**

- Single +5V Supply Operation
- 4 (MAX114) or 8 (MAX118) Analog Input Channels
- Low Power: 40mW (operating mode) 5μW (power-down mode)
- Total Unadjusted Error: ±1 LSB
- Fast Conversion Time: 660ns per Channel
- No External Clock Required
- Internal Track/Hold
- 1MHz Full-Power Bandwidth
- Internally Connected 8th Channel Monitors Reference Voltage (MAX118)

**Ordering Information**

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP. RANGE</th>
<th>PIN-PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX114CNG</td>
<td>0°C to +70°C</td>
<td>24 Narrow Plastic DIP</td>
</tr>
<tr>
<td>MAX114CAG</td>
<td>0°C to +70°C</td>
<td>24 SSOP</td>
</tr>
<tr>
<td>MAX114CD</td>
<td>0°C to +70°C</td>
<td>Dice*</td>
</tr>
<tr>
<td>MAX114ENC</td>
<td>-40°C to +85°C</td>
<td>24 Narrow Plastic DIP</td>
</tr>
<tr>
<td>MAX114EAG</td>
<td>-40°C to +85°C</td>
<td>24 SSOP</td>
</tr>
<tr>
<td>MAX114ERG</td>
<td>-55°C to +125°C</td>
<td>24 Narrow CERDIP**</td>
</tr>
</tbody>
</table>

Ordering Information continued on last page.

*Dice are specified at TA = +25°C. DC parameters only.
**Contact factory for availability.
Pin Configurations appear on last page.

**Applications**

- High-Speed DSP
- Portable Equipment
- Communications Systems

**Functional Diagram**

For free samples & the latest literature: [http://www.maxim-ic.com](http://www.maxim-ic.com), or phone 1-800-998-8800
+5V, 1MSPS, 4 & 8-Channel, 8-Bit ADCs with 1μA Power-Down

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>CONDITIONS</th>
<th>SYMBOL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd to GND</td>
<td>.........</td>
</tr>
<tr>
<td>Digital Input Voltage to GND</td>
<td>.........</td>
</tr>
<tr>
<td>Digital Output Voltage to GND</td>
<td>.........</td>
</tr>
<tr>
<td>REF + to GND</td>
<td>.........</td>
</tr>
<tr>
<td>REF - to GND</td>
<td>.........</td>
</tr>
<tr>
<td>IN - to GND</td>
<td>.........</td>
</tr>
<tr>
<td>REF+ to GND</td>
<td>.........</td>
</tr>
<tr>
<td>REF- to GND</td>
<td>.........</td>
</tr>
<tr>
<td>IN_ to GND</td>
<td>.........</td>
</tr>
<tr>
<td>REF+ to GND</td>
<td>.........</td>
</tr>
<tr>
<td>REF- to GND</td>
<td>.........</td>
</tr>
<tr>
<td>Operating Temperature Ranges</td>
<td>.........</td>
</tr>
</tbody>
</table>

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(\(V_{\text{DD}} = +5V \pm 5\%\), \(\text{REF} + = 5V\), \(\text{REF} - = \text{GND}\), Read Mode (MODE = GND), \(TA = T_{\text{MIN}}\) to \(T_{\text{MAX}}\), unless otherwise noted.)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>R</td>
<td></td>
<td>8</td>
<td></td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>Total</td>
<td>TUE</td>
<td></td>
<td>±1</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Nonlinearity</td>
<td>DNL</td>
<td>No missing-codes guaranteed</td>
<td>±1</td>
<td>LSB</td>
<td></td>
<td></td>
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<tr>
<td>Zero-Code Error</td>
<td></td>
<td></td>
<td>±1</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full-Range Error</td>
<td></td>
<td></td>
<td>±1</td>
<td>LSB</td>
<td></td>
<td></td>
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<tr>
<td>Channel-to-Channel Mismatch</td>
<td></td>
<td></td>
<td>±1/4</td>
<td>LSB</td>
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<tr>
<td>Signal-to-Noise Plus Distortion Ratio</td>
<td>SINAD</td>
<td>MAX114_CE, fSAMPLE = 1MHz, fn = 195.8kHz</td>
<td>45</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Harmonic Distortion</td>
<td>THD</td>
<td>MAX114_CE, fSAMPLE = 1MHz, fn = 195.8kHz</td>
<td>45</td>
<td>dB</td>
<td></td>
<td></td>
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<tr>
<td>Spurious-Free Dynamic Range</td>
<td>SFDR</td>
<td>MAX114_CE, fSAMPLE = 1MHz, fn = 195.8kHz</td>
<td>50</td>
<td>dB</td>
<td></td>
<td></td>
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<tr>
<td>Input Voltage Range</td>
<td>VIN</td>
<td>VREF</td>
<td>VREF +</td>
<td>V</td>
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<td></td>
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<tr>
<td>Input Leakage Current</td>
<td>IIN</td>
<td>GND &lt; VIN &lt; VDD</td>
<td>±3</td>
<td>μA</td>
<td></td>
<td></td>
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<tr>
<td>Input Capacitance</td>
<td>CIN</td>
<td>32</td>
<td>pf</td>
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<tr>
<td>Reference</td>
<td>REFF</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>kΩ</td>
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<tr>
<td>Reference Voltage Range</td>
<td>VREF</td>
<td>VDD</td>
<td>V</td>
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<tr>
<td>REF- Voltage Range</td>
<td>GND</td>
<td>VREF -</td>
<td>V</td>
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</tbody>
</table>
## ELECTRICAL CHARACTERISTICS (continued)

(VDD = +5V ±5%, REF+ = 5V, REF = GND, Read Mode (MODE = GND), TA = TMIN to TMAX, unless otherwise noted.)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>LOGIC INPUTS</strong></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Input High Voltage</td>
<td>V\text{IH}</td>
<td>CS, WR, RD, PWRDN, A0, A1, A2</td>
<td>2.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input Low Voltage</td>
<td>V\text{IL}</td>
<td>CS, WR, RD, PWRDN, A0, A1, A2</td>
<td>0.8</td>
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<td></td>
<td>V</td>
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<tr>
<td>Input High Current</td>
<td>I\text{IH}</td>
<td>CS, RD, PWRDN, A0, A1, A2</td>
<td>±1</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>Input Low Current</td>
<td>I\text{IL}</td>
<td>CS, WR, RD, PWRDN, MODE, A0, A1, A2</td>
<td>±1</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>Input Capacitance (Note 2)</td>
<td>C\text{IN}</td>
<td>CS, WR, RD, PWRDN, MODE, A0, A1, A2</td>
<td>5</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td><strong>LOGIC OUTPUTS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Low Voltage</td>
<td>V\text{OL}</td>
<td>IS\text{INK} = 1.6mA, INT, D0-D7</td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output High Voltage</td>
<td>V\text{OH}</td>
<td>IS\text{OURCE} = 360μA, INT, D0-D7</td>
<td>4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Three-State Current</td>
<td>I\text{LKG}</td>
<td>D0-D7, RDY, digital outputs = 0V to VDD</td>
<td>±3</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>Three-State Capacitance (Note 2)</td>
<td>C\text{OUT}</td>
<td>D0-D7, RDY</td>
<td>5</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td><strong>POWER REQUIREMENTS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>V\text{DD}</td>
<td></td>
<td>4.75</td>
<td>5.25</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V\text{DD} Supply Current</td>
<td>I\text{PD}</td>
<td>CS = RD = 0V, PWRDN = VDD</td>
<td>11</td>
<td>15</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Power-Down V\text{DD} Current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power-Supply Rejection</td>
<td>PSR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 2:** Guaranteed by design.
**Note 3:** Power-down current increases if logic inputs are not driven to GND or VDD.
**+5V, 1Mps, 4 & 8-Channel, 8-Bit ADCs with 1μA Power-Down**

**TIMING CHARACTERISTICS**

(\(V_{DD} = \pm 4.75\) V, \(TA = +25^\circ\)C, unless otherwise noted.) (Note 4)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>(TA = +25^\circ)C ALL GRADES</th>
<th>(TA = \text{TMIN to TMAX})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conversion Time (WR-RD Mode)</td>
<td>tWR</td>
<td>RD &lt; tINTL, (Note 5)</td>
<td>(CL = 20)pF</td>
<td>(CL = 1000)pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>460</td>
<td>685</td>
</tr>
<tr>
<td>Conversion Time (RD Mode)</td>
<td>tCROD</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>700</td>
<td>875</td>
</tr>
<tr>
<td>Power-Up Time</td>
<td>tUP</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>320</td>
<td>370</td>
</tr>
<tr>
<td>CS to RD, WR Setup Time</td>
<td>tCSS</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>CS to RD, WR Hold Time</td>
<td>tCSH</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>CS to RDY Delay</td>
<td>tRDY</td>
<td>(CL = 50)pF, (RL = 5.1k)Ω to (V_{DD})</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>70</td>
<td>85</td>
</tr>
<tr>
<td>Data Access Time (RD Mode)</td>
<td>tACC0</td>
<td>(CL = 1000)pF (Note 5)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(t_{CD} - \frac{50}{65})</td>
<td>(t_{CD} + \frac{75}{65})</td>
</tr>
<tr>
<td>RD to INT Delay (RD Mode)</td>
<td>tINTH</td>
<td>(CL = 50)pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>50</td>
<td>80</td>
</tr>
<tr>
<td>Data Hold Time</td>
<td>tDH</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Minimum Acquisition Time</td>
<td>tACQ</td>
<td>(Note 6)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>160</td>
<td>185</td>
</tr>
<tr>
<td>WR Pulse Width</td>
<td>tWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.25</td>
<td>10</td>
</tr>
<tr>
<td>Delay Between WR and RS Pulses</td>
<td>tRD</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.25</td>
<td>0.35</td>
</tr>
<tr>
<td>RD Pulse Width (WR-RD Mode)</td>
<td>tREAD1</td>
<td>RD &lt; tINTL, determined by tACM</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>160</td>
<td>205</td>
</tr>
<tr>
<td>Data Access Time (WR-RD Mode)</td>
<td>tACC1</td>
<td>RD &lt; tINTL, (CL = 1000)pF (Note 5)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>185</td>
<td>235</td>
</tr>
<tr>
<td>RD to INT Delay</td>
<td>tRD</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>150</td>
<td>185</td>
</tr>
<tr>
<td>WR to INT Delay</td>
<td>tINTL</td>
<td>(CL = 50)pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>380</td>
<td>500</td>
</tr>
<tr>
<td>RD Pulse Width (WR-RD Mode)</td>
<td>tREAD2</td>
<td>RD &gt; tINTL, determined by tACM</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>65</td>
<td>75</td>
</tr>
<tr>
<td>Data Access Time (WR-RD Mode)</td>
<td>tACC2</td>
<td>RD &gt; tINTL, (CL = 1000)pF (Note 5)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>90</td>
<td>110</td>
</tr>
<tr>
<td>WR to INT Delay</td>
<td>tWR</td>
<td>Pipelined mode, (CL = 50)pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>80</td>
<td>100</td>
</tr>
<tr>
<td>Data Access Time after INT</td>
<td>tD</td>
<td>Pipelined mode, (CL = 1000)pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>45</td>
<td>60</td>
</tr>
<tr>
<td>Multiplexer Address Hold Time</td>
<td>tAH</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>30</td>
<td>35</td>
</tr>
</tbody>
</table>

**UNITS**

- ns
- μs

**Note 4:** Input control signals are specified with \(t_{r} = t_{f} = 5\)ns, 10% to 90% of \(V_{DD}\), and timed from a voltage level of 1.6V.

**Note 5:** See Figure 1 for load circuit. Parameter defined as the time required for the output to cross 0.8V or 2.4V.

**Note 6:** See Figure 2 for load circuit. Parameter defined as the time required for the data lines to change 0.5V.

**Note 7:** Also defined as the Minimum Address-Valid to Convert Start Time.
+5V, 1Msps, 4 & 8-Channel, 8-Bit ADCs with 1μA Power-Down

Typical Operating Characteristics

(VDD = +5V, TA = +25°C, unless otherwise noted.)
+5V, 1Msps, 4 & 8-Channel, 8-Bit ADCs with 1μA Power-Down

**Pin Description**

<table>
<thead>
<tr>
<th>PIN</th>
<th>MAX114</th>
<th>MAX118</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>IN6</td>
<td>Analog Input Channel 6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>IN5</td>
<td>Analog Input Channel 5</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>3</td>
<td>IN4</td>
<td>Analog Input Channel 4</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>4</td>
<td>IN3</td>
<td>Analog Input Channel 3</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>5</td>
<td>IN2</td>
<td>Analog Input Channel 2</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>6</td>
<td>IN1</td>
<td>Analog Input Channel 1</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>7</td>
<td>MODE</td>
<td>Mode Selection Input. Internally pulled low with a 50μA current source. MODE = 0 activates read mode; MODE = 1 activates write-read mode (see Digital Interface Section).</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>8</td>
<td>DO</td>
<td>Three-State Data Output (LSB)</td>
<td></td>
</tr>
<tr>
<td>7, 8, 9</td>
<td>9, 10, 11</td>
<td>D1, D2, D3</td>
<td>Three-State Data Outputs</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>12</td>
<td>RD</td>
<td>Read Input. RD must be low to access data (see Digital Interface section).</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>13</td>
<td>INT</td>
<td>Interrupt Output. INT goes low to indicate end of conversion (see Digital Interface section).</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>14</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>15</td>
<td>REF-</td>
<td>Lower Limit of Reference Span. REF- sets the zero-code voltage. Range is GND ≤ VREF- &lt; VREF+.</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>16</td>
<td>REF+</td>
<td>Upper Limit of Reference Span. REF+ sets the full-scale input voltage. Range is VREF- &lt; VREF+ ≤ VDD. Internally hard-wired to IN8 (Table 1).</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>17</td>
<td>W/RDY</td>
<td>Write-Control Input/Ready Status Output (see Digital Interface section).</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>18</td>
<td>CS</td>
<td>Chip-Select Input. CS must be low for the device to recognize WR or RD inputs.</td>
<td></td>
</tr>
<tr>
<td>17, 18, 19</td>
<td>19, 20, 21</td>
<td>D4, D5, D6</td>
<td>Three-State Data Outputs</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>22</td>
<td>D7</td>
<td>Three-State Data Output (MSB)</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>23</td>
<td>A2</td>
<td>Multiplexer Channel Address Input (MSB)</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>24</td>
<td>A1</td>
<td>Multiplexer Channel Address Input</td>
<td></td>
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<td>23</td>
<td>25</td>
<td>A0</td>
<td>Multiplexer Channel Address Input (LSB)</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>26</td>
<td>PWREN</td>
<td>Power-Down Input. PWREN reduces supply current when low.</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>27</td>
<td>VDD</td>
<td>Positive Supply, +5V</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>28</td>
<td>IN7</td>
<td>Analog Input Channel 7</td>
<td></td>
</tr>
</tbody>
</table>
Detailed Description

Converter Operation

The MAX114/MAX118 use a half-flash conversion technique (see Functional Diagram) in which two 4-bit flash ADC sections achieve an 8-bit result. Using 15 comparators, the flash ADC compares the unknown input voltage to the reference ladder and provides the upper four data bits. An internal digital-to-analog converter (DAC) uses the four most significant bits (MSBs) to generate both the analog result from the first flash conversion and a residue voltage that is the difference between the unknown input and the DAC voltage. The residue is then compared again with the flash comparators to obtain the lower four data bits (LSBs).

An internal analog multiplexer enables the devices to read four (MAX114) or eight (MAX118) different analog voltages under microprocessor (μP) control. One of the MAX118's analog channels, IN8, is internally hardwired and always reads VREF+ when selected.

Power-Down Mode

In burst-mode or low sample-rate applications, the MAX114/MAX118 can be shut down between conversions, reducing supply current to microamp levels (see Typical Operating Characteristics). A logic low on the PWRDN pin shuts the devices down, reducing supply current typically to 1 μA when powered from a single +5V supply. A logic high on PWRDN wakes up the MAX114/MAX118, and the selected analog input enters the track mode. The signal is fully acquired after 360ns (this includes both the power-up delay and the track/hold acquisition time), and a new conversion can be started. If the power-down feature is not required, connect PWRDN to Vpp. For minimum current consumption, keep digital inputs at the supply rails in power-down mode. Refer to the Reference section for information on reducing reference current during power-down.

Digital Interface

The MAX114/MAX118 have two basic interface modes, which are set by the MODE pin. When MODE is low, the converters are in read mode; when MODE is high, the converters are set up for write-read mode. The AD, A1, A2 inputs control channel selection, as shown in Table 1. The address must be valid for a minimum time, tACQ, before the next conversion starts.

Table 1. Truth Table for Input Channel Selection

<table>
<thead>
<tr>
<th></th>
<th>MAX114</th>
<th>MAX118</th>
<th>SELECTED CHANNEL</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>A0</td>
<td>A2</td>
<td>A1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>0</td>
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<td>1</td>
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<tr>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

Read Mode (MODE = 0)

In read mode, conversions and data access are controlled by the RD input (Figure 3). The comparator inputs track the analog input voltage for the duration of tACQ. Initiate a conversion by driving CS and RD low. With μPs that can be forced into a wait state, hold RD low until output data appears. The μP starts the conversion, waits, and then reads data with a single read instruction.
In read mode, WR/RODY is configured as a status output (RODY), so it can drive the ready or wait input of a μP. RODY is an open-collector output (no internal pull-up) that goes low after the falling edge of CS and goes high at the end of the conversion. If not used, the WR/RODY pin can be left unconnected. The INT output goes low at the end of the conversion and returns high on the rising edge of CS or RO.

**Write-Read Mode (MODE = 1)**

Figures 4 and 5 show the operating sequence for write-read mode. The comparator inputs track the analog input voltage for the duration of tACQ. The conversion is initiated by a falling edge of WR. When WR returns high, the result of the four-MSBs flash is latched into the output buffers and the conversion of the four-LSBs flash starts. INT goes low, indicating conversion end, and the lower four data bits are latched into the output buffers. The data is then accessible after RO goes low (see **Timing Characteristics**).

A minimum acquisition time (tACQ) is required from INT going low to the start of another conversion (WR going low).

Options for reading data from the converter include using internal delay, reading before delay, and pipelined operation (discussed in the following sections).

**Using Internal Delay**

The μP waits for the INT output to go low before reading the data (Figure 4). INT goes low after the rising edge of WR, indicating that the conversion is complete and the result is available in the output latch. With CS low, data outputs D0-D7 can be accessed by pulling RO low. INT is then reset by the rising edge of CS or RO.

**Fastest Conversion: Reading Before Delay**

Figure 5 shows an external method of controlling the conversion time. The internally generated delay (tINTL) varies slightly with temperature and supply voltage, and can be overridden with RD to achieve the fastest conversion time. RD is brought low after the rising edge of WR, but before INT goes low. This completes the conversion and enables the output buffers that contain the conversion result (DO-D7). INT also goes low after the falling edge of RD and is reset on the rising edge of RD or CS. The total conversion time is therefore: tWR + tRD + tACQ = 660 ns.
+5V, 1Mmps, 4 & 8-Channel, 8-Bit ADCs with 1µA Power-Down

**Pipelined Operation**

Besides the two standard write-read-mode options, pipelined operation can be achieved by connecting WR to RD (Figure 6). With CS low, driving WR and RD low initiates a conversion and concurrently reads the result of the previous conversion.

**Analog Considerations**

**Reference**

Figures 7a, 7b, and 7c show typical reference connections. The voltages at REF+ and REF- set the ADC's analog input range (see Figure 10). The voltage at REF- defines the input that produces an output code of all zeros, and the voltage at REF+ defines the input that produces an output code of all ones.

The internal resistance from REF+ to REF- can be as low as 1kΩ, and current will flow through it even when the MAX114/MAX118 are shut down. Figure 7d shows how an N-channel MOSFET can be connected to REF-.
+5V, 1Msps, 4 & 8-Channel, 8-Bit ADCs with 1µA Power-Down

**Initial Power-Up**

When power is first applied, perform a conversion to initialize the MAX114/MAX118. Disregard the output data.

**Bypassing**

Use a 4.7µF electrolytic in parallel with a 0.1µF ceramic capacitor to bypass VDD to GND. Minimize capacitor lead lengths.

Bypass the reference inputs with 0.1µF capacitors, as shown in Figures 7a, 7b, and 7c.

**Analog Inputs**

Figure 8 shows the equivalent circuit of the MAX114/MAX118 input. When a conversion starts and WR is low, VIN is connected to sixteen 0.6pF capacitors. During this acquisition phase, the input capacitors charge to the input voltage through the resistance of the internal analog switches. In addition, about 22pF of stray capacitance must be charged. The input can be modeled as an equivalent RC network (Figure 9). As source impedance increases, the capacitors take longer to charge.

The typical 32pF input capacitance allows source resistance as high as 8000Ω without setup problems. For larger resistances, the acquisition time (TACQ) must be increased.

Internal protection diodes, which clamp the analog input to VDD and GND, allow the channel input pins to swing from GND - 0.3V to VDD + 0.3V without damage. However, for accurate conversions near full scale, the inputs must not exceed VDD by more than 50mV or be lower than GND by 50mV. If the analog input exceeds 50mV beyond the supplies, limit the input current to no more than 2mA, as excessive current will degrade the conversion accuracy of the on channel.

**Track/Hold**

The track/hold enters hold mode when a conversion starts (RD low or WR low). INT goes low at the end of the conversion, at which point the track/hold enters track mode. The next conversion can start after the minimum acquisition time, TACQ.
+5V, 1MSPS, 4 & 8-Channel, 8-Bit ADCs with 1μA Power-Down

Transfer Function

Figure 10 shows the MAX114/MAX118's nominal transfer function. Code transitions occur halfway between successive-integer LSB values. Output coding is binary with 1LSB = (VREF+ - VREF-) / 256.

Conversion Rate

The maximum sampling rate (fMAX) for the MAX114/MAX118 is achieved in write-read mode (tRD < tINTL), and is calculated as follows:

\[ f_{\text{MAX}} = \frac{1}{t_{WR} + t_{RD} + t_{RI} + t_{ACQ}} \]

where \( t_{WR} \) is the write pulse width, \( t_{RD} \) is the delay between write and read pulses, \( t_{RI} = \text{RD to INT delay} \), and \( t_{ACQ} = \text{minimum acquisition time} \).

Signal-to-Noise Ratio and Effective Number of Bits

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to all other ADC output signals. The output spectrum is limited to frequencies above DC and below one-half the ADC sample rate.

The theoretical minimum analog-to-digital noise is caused by quantization error, and results directly from the ADC's resolution: SNR = (6.02N + 1.76)dB, where N is the number of bits of resolution. Therefore, a perfect 8-bit ADC can do no better than 50dB.

The FFT Plot (see Typical Operating Characteristics) shows the result of sampling a pure 195.8kHz sinusoid at a 1MHz rate. This FFT plot of the output shows the output level in various spectral bands.

The effective resolution (or "effective number of bits") the ADC provides can be measured by transposing the equation that converts resolution to SNR: N = (SINAD - 1.76) / 6.02 (see Typical Operating Characteristics).

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal (in the frequency band above DC and below one-half the sample rate) to the fundamental itself. This is expressed as:

\[ \text{THD} = 20 \log \left( \sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots + V_N^2} / V_1 \right) \]

where \( V_1 \) is the fundamental RMS amplitude, and \( V_2 \) through \( V_N \) are the amplitudes of the 2nd through Nth harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually the next largest spectral component occurs at some harmonic of the input frequency. However, if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor. See the Signal-to-Noise Ratio graph in Typical Operating Characteristics.
+5V, 1Msps, 4 & 8-Channel, 8-Bit ADCs with 1μA Power-Down

**Ordering Information (continued)**

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP. RANGE</th>
<th>PIN-PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX118CPI</td>
<td>0°C to +70°C</td>
<td>28 Wide Plastic DIP</td>
</tr>
<tr>
<td>MAX118CAI</td>
<td>0°C to +70°C</td>
<td>28 SSOP</td>
</tr>
<tr>
<td>MAX118CD</td>
<td>0°C to +70°C</td>
<td>Dice*</td>
</tr>
<tr>
<td>MAX118EPI</td>
<td>-40°C to +85°C</td>
<td>28 Wide Plastic DIP</td>
</tr>
<tr>
<td>MAX118EAI</td>
<td>-40°C to +85°C</td>
<td>28 SSOP</td>
</tr>
<tr>
<td>MAX118MII</td>
<td>-55°C to +125°C</td>
<td>28 Wide CERDIP**</td>
</tr>
</tbody>
</table>

*Dice are specified at TA = +25°C. DC parameters only.
**Contact factory for availability.

**Pin Configurations**

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