LAMPIRAN A

RANGKAIAN SKEMATIK
DAFTAR KOMPONEN
GAMBAR RANGKAIAN I

C1 = 10 nF
C2 = 1 nF
C3 = 1 nF
C4 = 10 nF
C5 = 100 nF
C6 = 10 nF
C7 = 100 nF
C8 = 100 nF
C9 = 100 nF

D1 = 1N4148
D2 = 1N4148
D3 = 1N4148
D4 = 1N4148

R1 = 22 KΩ
R2 = 47 KΩ
R3 = 4,7 MΩ
R4 = 47 KΩ
R5 = 1 MΩ
R6 = 100 KΩ
R7 = 5 KΩ
R8 = 470 Ω
R9 = 470 Ω
R10 = 10 KΩ
DAFTAR KOMPONEN
GAMBAR RANGKAIAN II

C1 = 10 µF
C2 = 22 pF
C3 = 22 pF
C4 = 2200 µF / 25 Volt
C5 = 1000 µF / 16 Volt
C6 = 100 nF
C7 = 100 nF
C8 = 100 nF
D1 = 1N4148
R4 = 10 KΩ
R11 = 100 KΩ
X1 = 14 MHz
8751BH
SINGLE-CHIP 8-BIT MICROCOMPUTER
WITH 4K BYTES OF EPROM PROGRAM MEMORY

- Program Memory Lock
- 128 Bytes Data Ram
- Quick Pulse Programming™ Algorithm
- 12.75 Volt Programming Voltage
- Boolean Processor
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- 5 Interrupt Sources
- Programmable Serial Channel
- 64K External Program Memory Space
- 64K External Data Memory Space

Figure 1. 8751BH Block Diagram
PACKAGES

<table>
<thead>
<tr>
<th>Part</th>
<th>Prefix</th>
<th>Package Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>8751BH</td>
<td>P</td>
<td>40-Pin Plastic DIP</td>
</tr>
<tr>
<td></td>
<td>N</td>
<td>44-Pin PLCC</td>
</tr>
</tbody>
</table>

PIN DESCRIPTIONS

V<sub>CC</sub>: Supply voltage.

V<sub>SS</sub>: Circuit ground.

Port 0: Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink 8 LS TTL inputs. Port 0 pins that have 1s written to them float and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to External Program and Data Memory. In this application it uses strong internal pullups when emitting 1s, and can source and sink 8 LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source 4 LS TTL inputs. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I<sub>IL</sub>, on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address bytes during EPROM programming and program verification.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source 4 LS TTL inputs. Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I<sub>IL</sub>, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from External Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @OPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external Data Memory that use 8-bit addresses (MOVX @A), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits during EPROM programming and program verification.
Port 2: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/ source 4 LS TTL inputs. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_L) on the data sheet because of the pullups.

Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:

<table>
<thead>
<tr>
<th>Port Pin</th>
<th>Alternate Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>P3.0</td>
<td>RXD (serial input port)</td>
</tr>
<tr>
<td>P3.1</td>
<td>TXD (serial output port)</td>
</tr>
<tr>
<td>P3.2</td>
<td>INT0 (external interrupt 0)</td>
</tr>
<tr>
<td>P3.3</td>
<td>INT1 (external interrupt 1)</td>
</tr>
<tr>
<td>P3.4</td>
<td>T0 (Timer 0 external input)</td>
</tr>
<tr>
<td>P3.5</td>
<td>T1 (Timer 1 external input)</td>
</tr>
<tr>
<td>P3.6</td>
<td>WR (external data memory write strobe)</td>
</tr>
<tr>
<td>P3.7</td>
<td>RD (external data memory read strobe)</td>
</tr>
</tbody>
</table>

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/PROG: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during EPROM programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that an ALE pulse is skipped during each access to external Data Memory.

PSEN: Program Store Enable is the read strobe to External Program Memory.

When the 8751BH is executing code from external Program Memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to External Data Memory.

EA/V_pp: External Access enable. EA must be strapped to VSS in order to enable the device to fetch code from External Program Memory locations starting at 0000H up to FFFFH. Note, however, that if either of the Lock Bits are programmed, EA will be internally latched on reset.

EA should be strapped to VCC for internal program executions.

This pin also receives the 12.75V programming supply voltage (Vpp) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

**OSCILLATOR CHARACTERISTICS**

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Applications Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be grounded, while XTAL2 is driven, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

**DESIGN CONSIDERATIONS**

If an 8751BH is replacing an 8751H in an existing design, the user should carefully compare both data sheets for DC or AC Characteristic differences. Note that the Vpp and I_H specifications for the EA pin differ significantly between the 8751H and 8751BH.
**SOLUTE MAXIMUM RATINGS**

- Ambient Temperature Under Bias: 
  -0°C to +70°C
- Page Temperature: 
  -65°C to +150°C
- Page on VCC Pin to VSS: 
  - 0.5V to +13.0V
- Page on Any Other Pin to VSS: 
  - 0.5V to +7V
- Minimum VCC Per I/O Pin: 15 mA
- Over Dissipation: 1.5W

*Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**NOTICE: Specifications contained within the following tables are subject to change.**

### CHARACTERISTICS (TA = 0°C to +70°C; VCC = 5V ± 10%; VSS = 0V)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>I1</td>
<td>Input Low Voltage (Except EA)</td>
<td>-0.5</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I2</td>
<td>Input Low Voltage EA</td>
<td>VSS</td>
<td>0.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>H1</td>
<td>Input High Voltage (Except XTAL2, RST, EA)</td>
<td>2.0</td>
<td>VCC + 0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>H2</td>
<td>Input High Voltage to EA</td>
<td>4.5</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>OL</td>
<td>Output Low Voltage (Note 3) (Ports 1, 2, and 3)</td>
<td>0.45</td>
<td></td>
<td>V</td>
<td>IOL = 1.6 mA (Note 1)</td>
</tr>
<tr>
<td>OL1</td>
<td>Output Low Voltage (Note 3) (Ports 0, ALE/PROG, PSEN)</td>
<td>0.45</td>
<td></td>
<td>V</td>
<td>IOL = 3.2 mA (Notes 1, 2)</td>
</tr>
<tr>
<td>OH</td>
<td>Output High Voltage (Ports 1, 2, 3, ALE/PROG and PSEN)</td>
<td>2.4</td>
<td></td>
<td>V</td>
<td>IOH = -80 µA</td>
</tr>
<tr>
<td>OH1</td>
<td>Output High Voltage (Port 0 in External Bus Mode)</td>
<td>2.4</td>
<td></td>
<td>V</td>
<td>IOH = -400 µA</td>
</tr>
<tr>
<td>L1</td>
<td>Logical 0 Input Current (Ports 1, 2, 3, and RST)</td>
<td>-1</td>
<td></td>
<td>mA</td>
<td>VIN = 0.45V</td>
</tr>
<tr>
<td>L2</td>
<td>Logical 0 Input Current (EA)</td>
<td>-10</td>
<td></td>
<td>mA</td>
<td>VIN = VSS</td>
</tr>
<tr>
<td>L3</td>
<td>Logical 0 Input Current (XTAL2)</td>
<td>-3.2</td>
<td></td>
<td>mA</td>
<td>VIN = 0.45V XTAL1 = VSS</td>
</tr>
<tr>
<td>L1</td>
<td>Input Leakage Current (Port 0)</td>
<td>±10</td>
<td></td>
<td>µA</td>
<td>0.45 &lt; VIN &lt; VCC</td>
</tr>
<tr>
<td>L1</td>
<td>Logical 1 Input Current (EA)</td>
<td>1</td>
<td></td>
<td>mA</td>
<td>4.5V &lt; VIN &lt; 5.5V</td>
</tr>
<tr>
<td>H1</td>
<td>Input Current to RST to Activate Reset</td>
<td>500</td>
<td></td>
<td>µA</td>
<td>VIN &lt; (VCC - 1.5V)</td>
</tr>
<tr>
<td>OC</td>
<td>Power Supply Current</td>
<td>175</td>
<td></td>
<td>mA</td>
<td>All Outputs Disconnected</td>
</tr>
<tr>
<td>CO</td>
<td>Pin Capacitance</td>
<td>10pF</td>
<td></td>
<td></td>
<td>Test Freq = 1kHz</td>
</tr>
</tbody>
</table>

**NOTES:**
- Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VCC of ALE/PROG and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins take 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE/PROG pin may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address which uses a Schmitt Trigger STROBE input.
- ALE/PROG refers to a pin on the 8751BH. ALE refers to a timing signal that is output on the ALE/PROG pin.
- Under steady state (non-transient) conditions, Ib must be externally limited as follows:
  - Maximum Ib per port pin: 10 mA
  - Maximum Ib per 8-bit port: 26 mA
  - Maximum total Ib for all output pins: 71 mA
  - If Ib exceeds the test condition, VCC may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
A.C. CHARACTERISTICS (TA = -6°C to +70°C; VCC = 5V ± 10%; VSS = 0V); Load Capacitance for Port 0, ALE/PROG, and PSEN = 100 pF; Load Capacitance for All Other Outputs = 80 pF

EXTERNAL PROGRAM MEMORY CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>12 MHz Osc</th>
<th>Variable Oscillator</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>1/2TCLCL</td>
<td>Oscillator Frequency</td>
<td>3.5</td>
<td>12.0 MHz</td>
<td>ns</td>
</tr>
<tr>
<td>TLLML</td>
<td>ALE Pulse Width</td>
<td>127</td>
<td>2TCLCL - 40</td>
<td>ns</td>
</tr>
<tr>
<td>TAVLL</td>
<td>Address Valid to ALE Low</td>
<td>43</td>
<td>TCLCL - 40</td>
<td>ns</td>
</tr>
<tr>
<td>TLLAX</td>
<td>Address Hold After ALE Low</td>
<td>48</td>
<td>TCLCL - 35</td>
<td>ns</td>
</tr>
<tr>
<td>TLLIV</td>
<td>ALE Low to Valid Instruction In</td>
<td>233</td>
<td>4TCLCL - 100</td>
<td>ns</td>
</tr>
<tr>
<td>TLLPL</td>
<td>ALE Low to PSEN Low</td>
<td>58</td>
<td>TCLCL - 25</td>
<td>ns</td>
</tr>
<tr>
<td>TPLPH</td>
<td>PSEN Pulse Width</td>
<td>215</td>
<td>3TCLCL - 35</td>
<td>ns</td>
</tr>
<tr>
<td>TPLIV</td>
<td>PSEN Low to Valid Instruction In</td>
<td>125</td>
<td>3TCLCL - 125</td>
<td>ns</td>
</tr>
<tr>
<td>TPXX</td>
<td>Input Instr Hold After PSEN</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>TPXZ</td>
<td>Input Instr Float After PSEN</td>
<td>63</td>
<td>TCLCL - 20</td>
<td>ns</td>
</tr>
<tr>
<td>TPXAV</td>
<td>PSEN to Address Valid</td>
<td>75</td>
<td>TCLCL - 8</td>
<td>ns</td>
</tr>
<tr>
<td>TAVIV</td>
<td>Address to Valid Instruction In</td>
<td>302</td>
<td>5TCLCL - 115</td>
<td>ns</td>
</tr>
<tr>
<td>TPLAZ</td>
<td>PSEN Low to Address Float</td>
<td>20</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>TLRH</td>
<td>RD Pulse Width</td>
<td>400</td>
<td>6TCLCL - 100</td>
<td>ns</td>
</tr>
<tr>
<td>TWLWH</td>
<td>WR Pulse Width</td>
<td>400</td>
<td>6TCLCL - 100</td>
<td>ns</td>
</tr>
<tr>
<td>TRLDV</td>
<td>RD Low to Valid Data In</td>
<td>252</td>
<td>5TCLCL - 165</td>
<td>ns</td>
</tr>
<tr>
<td>TRHDX</td>
<td>Data Hold After RD</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>TRHDZ</td>
<td>Data Float After RD</td>
<td>97</td>
<td>2TCLCL - 70</td>
<td>ns</td>
</tr>
<tr>
<td>TLLDV</td>
<td>ALE Low to Valid Data In</td>
<td>517</td>
<td>8TCLCL - 150</td>
<td>ns</td>
</tr>
<tr>
<td>TAVDV</td>
<td>Address to Valid Data In</td>
<td>585</td>
<td>9TCLCL - 165</td>
<td>ns</td>
</tr>
<tr>
<td>TLLWL</td>
<td>ALE Low to RD or WR Low</td>
<td>200</td>
<td>3TCLCL - 50</td>
<td>ns</td>
</tr>
<tr>
<td>TAVVL</td>
<td>Address to RD or WR Low</td>
<td>203</td>
<td>4TCLCL - 130</td>
<td>ns</td>
</tr>
<tr>
<td>TQVWX</td>
<td>Data Valid to WR Transition</td>
<td>23</td>
<td>TCLCL - 60</td>
<td>ns</td>
</tr>
<tr>
<td>TQVWH</td>
<td>Data Valid to WR High</td>
<td>433</td>
<td>7TCLCL - 150</td>
<td>ns</td>
</tr>
<tr>
<td>TQVHX</td>
<td>Data Hold After WR</td>
<td>33</td>
<td>TCLCL - 50</td>
<td>ns</td>
</tr>
<tr>
<td>TRLAZ</td>
<td>RD Low to Address Float</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>TWHLH</td>
<td>RD or WR High to ALE High</td>
<td>43</td>
<td>TCLCL - 40</td>
<td>ns</td>
</tr>
</tbody>
</table>
SERIAL PORT TIMING — SHIFT REGISTER MODE

TEST CONDITIONS (TA = 0°C to +70°C; VCC = 5V ± 10%; VSS = 0V; Load Capacitance = 80 pF)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>12MHz Osc</th>
<th>Variable Oscillator</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>TXLXL</td>
<td>Serial Port Clock Cycle Time</td>
<td>1.0</td>
<td></td>
<td>12 TCLKL</td>
</tr>
<tr>
<td>TQVXH</td>
<td>Output Data Setup to Clock Rising Edge</td>
<td>700</td>
<td></td>
<td>10 TCLKL – 133 ns</td>
</tr>
<tr>
<td>TXHOX</td>
<td>Output Data Hold After Clock Rising Edge</td>
<td>50</td>
<td></td>
<td>2 TCLKL – 117 ns</td>
</tr>
<tr>
<td>TXHOX</td>
<td>Input Data Hold After Clock Rising Edge</td>
<td>0</td>
<td></td>
<td>0               ns</td>
</tr>
<tr>
<td>TXHOV</td>
<td>Clock Rising Edge to Input Data Valid</td>
<td>700</td>
<td></td>
<td>10 TCLKL – 133 ns</td>
</tr>
</tbody>
</table>

Shift Register Mode Timing Waveforms

External Clock Drive Waveforms
EXTERNAL CLOCK DRIVE

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/TCCL</td>
<td>Oscillator Frequency</td>
<td>3.5</td>
<td>12</td>
<td>MHz</td>
</tr>
<tr>
<td>TCHCX</td>
<td>High Time</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TCLKX</td>
<td>Low Time</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TCHCL</td>
<td>Rise Time</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TCHCL</td>
<td>Fall Time</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

EPROM CHARACTERISTICS

Programming the EPROM

To be programmed, the part must be running with a 4 to 6 MHz oscillator. (The reason the oscillator needs to be running is that the internal bus is being used to transfer address and program data to appropriate internal registers.) The address of an EPROM location to be programmed is applied to Port 1 and pins P2.0 - P2.3 of Port 2, while the code byte to be programmed into that location is applied to Port 0. The other Port 2 and 3 pins, and RST, PSEN, and EA/Vpp should be held at the “Program” levels indicated in Table 1. ALE/PROG is pulsed low to program the code byte into the addressed EPROM location. The setup is shown in Figure 5.

Normally EA/Vpp is held at a logic high until just before ALE/PROG is to be pulsed. Then EA/Vpp is raised to Vpp, ALE/PROG is pulsed low, and then EA/Vpp is returned to a valid high voltage. The voltage on the EA/Vpp pin must be at the valid EA/Vpp high level before a verify is attempted. Waveforms and detailed timing specifications are shown in later sections of this data sheet.

Note that the EA/Vpp pin must not be allowed to go above the maximum specified Vpp level for any amount of time. Even a narrow glitch above that voltage level can cause permanent damage to the device. The Vpp source should be well regulated and free of glitches.

AC TESTING INPUT/OUTPUT WAVEFORMS

![AC Testing Input/Output Waveforms](image)

Figure 5. Programming the EPROM
Table 1. EPROM Programming Modes

<table>
<thead>
<tr>
<th>MODE</th>
<th>RST</th>
<th>PSEN</th>
<th>ALE/PROG</th>
<th>EA/ Vpp</th>
<th>P2.7</th>
<th>P2.6</th>
<th>P3.6</th>
<th>P3.7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Program Code Data</td>
<td>1</td>
<td>0</td>
<td>0*</td>
<td>Vpp</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Verify Code Data</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Program Encryption Table</td>
<td>1</td>
<td>0</td>
<td>0*</td>
<td>Vpp</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Use Addresses 0-1FH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Program Lock Bits (L.Bx)</td>
<td>x=1</td>
<td>1</td>
<td>0</td>
<td>Vpp</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>x=2</td>
<td>1</td>
<td>0</td>
<td>0*</td>
<td>Vpp</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Read Signature</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

NOTES:
"0" = Valid high for that pin
"0*" = Valid high for that pin
"Vpp" = +12.75V ±0.25V
* ALE/PROG is pulsed low for 100 μS for programming. (Quick-Pulse Programming™)

QUICK-PULSE PROGRAMMING™ ALGORITHM

The 8751BH can be programmed using the Quick-Pulse Programming Algorithm for microcontrollers. The features of the new programming method are a lower Vpp (12.75 volts as compared to 21 volts) and a shorter programming pulse. It is possible to program the entire 4K Bytes of EPROM memory in less than 13 seconds with this algorithm.

To program the part using the new algorithm, Vpp must be 12.75 ± 0.25 Volts. ALE/PROG is pulsed low for 100 μS, 25 times. Then, the byte just programmed may be verified. After programming, the entire array should be verified. The Program Lock features are programmed using the same method, but with the setup as shown in Table 1. The only difference in programming Lock features is that the lock features cannot be directly verified. Instead, verification of programming is by observing that their features are enabled.

PROGRAM VERIFICATION

If the Lock Bits have not been programmed, the on-chip Program Memory can be read out for verification purposes, if desired, either during or after the programming operation. The address of the Program Memory location to be read is applied to Port 1 and pins P2.0 - P2.3. The other pins should be held at the "Verify" levels indicated in Table 1. The contents of the addressed location will come out on Port 0. External pullups are required on Port 0 for this operation. (If the Encryption Array in the EPROM has been programmed, the data present at Port 0 will be Code Data XNOR Encryption Data. The user must know the Encryption Array contents to manually "unencrypt" the data during verify.)

The setup, which is shown in Figure 6, is the same as for programming the EPROM except that pin P2.7 is held at a logic low, or may be used as an active low read strobe.
PROGRAM MEMORY LOCK

The two-level Program Lock system consists of 2 Lock bits and a 32-byte Encryption Array which are used to protect the program memory against software piracy.

Encryption Array

Within the EPROM array are 32 bytes of Encryption Array that are initially unprogrammed (all 1s). Every time that a byte is addressed during a verify, 5 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NORed (XNOR) with the code byte, creating an Encrypted Verify byte. The algorithm, with the array in the unprogrammed state (all 1s), will return the code in its original, unmodified form.

It is recommended that whenever the Encryption Array is used, at least one of the Lock Bits be programmed as well.

Lock Bits

Also included in the EPROM Program Lock scheme are two Lock Bits which function as shown in Table 2.

<table>
<thead>
<tr>
<th>Lock Bits</th>
<th>Logic Enabled</th>
</tr>
</thead>
<tbody>
<tr>
<td>LB1</td>
<td>LB2</td>
</tr>
<tr>
<td>U</td>
<td>U</td>
</tr>
<tr>
<td>P</td>
<td>U</td>
</tr>
<tr>
<td>P</td>
<td>P</td>
</tr>
<tr>
<td>U</td>
<td>P</td>
</tr>
</tbody>
</table>

Table 2, Lock Bits and their Features

To ensure proper functionality of the chip, the internally latched value of the EA pin must agree with its external state.

ERASURE CHARACTERISTICS

This device is in a plastic package without a window and, therefore, cannot be erased.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low, the values returned are:

(030H) = 89H indicates manufactured by Intel
(031H) = 51H indicates 8751BH
### EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T<sub>A</sub> = 21°C to 27°C, V<sub>CC</sub> = 5.0V ± 10%, V<sub>SS</sub> = 0V)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>Programming Supply Voltage</td>
<td>12.5</td>
<td>13.0</td>
<td>V</td>
</tr>
<tr>
<td>IPP</td>
<td>Programming Supply Current</td>
<td>50</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>1/TCLCL</td>
<td>Oscillator Frequency</td>
<td>4</td>
<td>6</td>
<td>MHz</td>
</tr>
<tr>
<td>TAVGL</td>
<td>Address Setup to PROG Low</td>
<td>48TCLCL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TGMAX</td>
<td>Address Hold After PROG</td>
<td>48TCLCL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TDVGL</td>
<td>Data Setup to PROG Low</td>
<td>48TCLCL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TGHDX</td>
<td>Data Hold After PROG</td>
<td>48TCLCL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TEHSH</td>
<td>P2.7 ENABLE High to V&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>48TCLCL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TSHGL</td>
<td>V&lt;sub&gt;pp&lt;/sub&gt; Setup to PROG Low</td>
<td>10</td>
<td></td>
<td>μsec</td>
</tr>
<tr>
<td>TGHSL</td>
<td>V&lt;sub&gt;pp&lt;/sub&gt; Hold After PROG</td>
<td>10</td>
<td></td>
<td>μsec</td>
</tr>
<tr>
<td>TGLGH</td>
<td>PROG Width</td>
<td>90</td>
<td>110</td>
<td>μsec</td>
</tr>
<tr>
<td>TAVOV</td>
<td>Address to Data Valid</td>
<td>48TCLCL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TEOV</td>
<td>ENABLE Low to Data Valid</td>
<td>48TCLCL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TEHOZ</td>
<td>Data Float After ENABLE</td>
<td>0</td>
<td></td>
<td>μsec</td>
</tr>
<tr>
<td>TGHGL</td>
<td>PROG High to PROG Low</td>
<td>10</td>
<td></td>
<td>μsec</td>
</tr>
</tbody>
</table>

#### EPROM Programming and Verification Waveforms

![EPROM Programming and Verification Waveforms](image-url)
ADC0801, ADC0802, ADC0803, ADC0804, ADC0805 8-Bit μP Compatible A/D Converters

General Description
The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS020A derivative control bus with TRI-DATA output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features
- Compatible with 8080 μP derivatives—no interfacing logic needed - access time - 125 ns
- Easy interface to all microprocessors, or operates “stand alone”

Key Specifications
- Resolution 8 bits
- Total error ± 1/2 LSB, ± 1/4 LSB and ± 1 LSB
- Conversion time 100 μs

Typical Applications

Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Full-Scale Adjusted</th>
<th>( V_{REF}/2 = 2.500 \text{ VDC} )</th>
<th>( V_{REF}/2 = \text{No Connection} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC0801</td>
<td>± 1/2 LSB</td>
<td>(No Adjustments)</td>
<td>(No Adjustments)</td>
</tr>
<tr>
<td>ADC0802</td>
<td>± 1/4 LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC0803</td>
<td>± 1/2 LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC0804</td>
<td>± 1 LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC0805</td>
<td>± 1 LSB</td>
<td></td>
<td>± 1 LSB</td>
</tr>
</tbody>
</table>
**Absolute Maximum Ratings (Notes 1 & 2)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (VCC) (Note 3)</td>
<td>6.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic Control Inputs</td>
<td>-0.3V to +18V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>All Other Input and Outputs</td>
<td>-0.3V to (VCC + 0.3V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead Temp. (Soldering; 10 seconds)</td>
<td>Dual-In-Line Package (plastic) 260°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Dual-In-Line Package (ceramic) 300°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Surface Mount Package Vapor Phase (50 seconds) 215°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Infrared (15 seconds) 220°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Operating Ratings (Notes 1 & 2)**

<table>
<thead>
<tr>
<th>Temperature Range</th>
<th>ADC0801/02/LJ</th>
<th>ADC0801/02/03/04LCJ</th>
<th>ADC0801/02/03/05LCN</th>
<th>ADC0804LCN</th>
<th>ADC0802/03/04LV</th>
<th>ADC0802/03/04LCVM</th>
<th>Range of VCC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>4.5 VCC to 6.3 VCC</td>
</tr>
<tr>
<td>Package Dissipation at TA = 25°C</td>
<td>875 mW</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>800V</td>
</tr>
<tr>
<td>ESD Susceptibility (Note 10)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Electrical Characteristics**

The following specifications apply for VCC = 5 VCC, TMIN ≤ TA ≤ TMAX and fCLK = 640 kHz unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC0801; Total Adjusted Error (Note 8)</td>
<td>With Full-Scale Adj. (See Section 2.5.2)</td>
<td>±1/2</td>
<td></td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>ADC0802; Total Unadjusted Error (Note 8)</td>
<td>VREF/2 = 2,500 VCC</td>
<td>±1/2</td>
<td></td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>ADC0803; Total Adjusted Error (Note 8)</td>
<td>With Full-Scale Adj. (See Section 2.5.2)</td>
<td>±1/4</td>
<td></td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>ADC0804; Total Unadjusted Error (Note 8)</td>
<td>VREF/2 = 2,500 VCC</td>
<td>±1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC0805; Total Unadjusted Error (Note 8)</td>
<td>VREF/2 = No Connection</td>
<td>±1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VREF/2 Input Resistance (Pin 9)</td>
<td>ADC0801/02/03/05</td>
<td>2.5</td>
<td>8.0</td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td></td>
<td>ADC0804 (Note 9)</td>
<td>0.75</td>
<td>1.1</td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>Analog Input Voltage Range (Note 4) VI (+) or VI (−)</td>
<td>Gnd -0.05</td>
<td>VCC + 0.05</td>
<td></td>
<td>VCC</td>
<td></td>
</tr>
<tr>
<td>DC Common-Mode Error</td>
<td>Over Analog Input Voltage Range</td>
<td>±1/8</td>
<td></td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>Power Supply Sensitivity</td>
<td>VCC = 5 VCC ± 10% Over Allowed VIN (+) and VIN (−) Voltage Range (Note 4)</td>
<td>±1/8</td>
<td></td>
<td></td>
<td>LSB</td>
</tr>
</tbody>
</table>

**AC Electrical Characteristics**

The following specifications apply for VCC = 5 VCC and TA = 25°C unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>TC1</td>
<td>Conversion Time</td>
<td>fCLK = 640 kHz (Note 6)</td>
<td>100</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>TC2</td>
<td>Conversion Time</td>
<td>(Note 5, 6)</td>
<td>65</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>fCLK</td>
<td>Clock Frequency</td>
<td>VCC = 5V, (Note 5)</td>
<td>100</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>Clock Duty Cycle</td>
<td>(Note 5)</td>
<td>40</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CR</td>
<td>Conversion Rate in Free-Running Mode</td>
<td>INTA tied to WR with CS = 0 VCC, fCLK = 640 kHz</td>
<td>8770</td>
<td></td>
<td></td>
<td>conv/s</td>
</tr>
<tr>
<td>LW</td>
<td>Width of WR Input (Start Pulse Width)</td>
<td>CS = 0 VCC (Note 7)</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>ACC</td>
<td>Access Time (Delay from Falling Edge of RD to Output Data Valid)</td>
<td>Cl = 100 pF</td>
<td>135</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TR1</td>
<td>TRI-STATE Control (Delay from Falling Edge of RD to Hi-Z State)</td>
<td>Cl = 10 pF, Rs = 10k (See TRI-STATE Test Circuits)</td>
<td>125</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TR2</td>
<td>Delay from Falling Edge of WR or RD to Reset of INTA</td>
<td></td>
<td>300</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>VCC</td>
<td>Input Capacitance of Logic Control Inputs</td>
<td></td>
<td>5</td>
<td>7.5</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>COUT</td>
<td>TRI-STATE Output Capacitance (Data Buffers)</td>
<td></td>
<td>5</td>
<td>7.5</td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>

**CONTROL INPUTS (Note: CLK IN on Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vth</td>
<td>Logical &quot;1&quot; Input Voltage (Except Pin 4 CLK IN)</td>
<td>VCC = 5.25 VCC</td>
<td>2.0</td>
<td></td>
<td></td>
<td>Vcc</td>
</tr>
</tbody>
</table>
### AC Electrical Characteristics (Continued)

The following specifications apply for VCC = 5Vdc and TMIN ≤ TA ≤ TMAX, unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN (0)</td>
<td>Logical &quot;0&quot; Input Voltage (Except Pin 4 CLKB IN)</td>
<td>VCC = 4.75 Vdc</td>
<td>0.8</td>
<td>Vdc</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIN (1)</td>
<td>Logical &quot;1&quot; Input Current (All Inputs)</td>
<td>VIN = 5 Vdc</td>
<td>0.005</td>
<td>1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>VIN (0)</td>
<td>Logical &quot;0&quot; Input Current (All Inputs)</td>
<td>VIN = 0 Vdc</td>
<td>-1</td>
<td>-0.005</td>
<td>μA</td>
<td></td>
</tr>
</tbody>
</table>

### CLOCK IN AND CLOCK OUT

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VTT+</td>
<td>CLK IN (Pin 4) Positive Going Threshold Voltage</td>
<td></td>
<td>2.7</td>
<td>3.1</td>
<td>3.5</td>
<td>Vdc</td>
</tr>
<tr>
<td>VTT-</td>
<td>CLK IN (Pin 4) Negative Going Threshold Voltage</td>
<td></td>
<td>1.5</td>
<td>1.8</td>
<td>2.1</td>
<td>Vdc</td>
</tr>
<tr>
<td>VTH</td>
<td>CLK IN (Pin 4) Hysteresis (VTT+ - VTT-)</td>
<td></td>
<td>0.6</td>
<td>1.3</td>
<td>2.0</td>
<td>Vdc</td>
</tr>
</tbody>
</table>

### DATA OUTPUTS AND INTR

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOUT (0)</td>
<td>Logical &quot;0&quot; Output Voltage</td>
<td>Data Outputs</td>
<td>IOUT = 1.6 mA, VCC = 4.75 Vdc</td>
<td>0.4</td>
<td>Vdc</td>
<td></td>
</tr>
<tr>
<td>VOUT (1)</td>
<td>Logical &quot;1&quot; Output Voltage</td>
<td></td>
<td>IOUT = 1.0 mA, VCC = 4.75 Vdc</td>
<td>0.4</td>
<td>Vdc</td>
<td></td>
</tr>
<tr>
<td>VOUT (1)</td>
<td>Logical &quot;1&quot; Output Voltage</td>
<td>INTR Output</td>
<td>IOUT = 10 μA, VCC = 4.75 Vdc</td>
<td>4.5</td>
<td>Vdc</td>
<td></td>
</tr>
<tr>
<td>IOUT</td>
<td>TRI-STATE Disabled Output Leakage (All Data Buffers)</td>
<td></td>
<td>-3</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>ISINK</td>
<td>VOUT Short to Gnd, TA = 25°C</td>
<td></td>
<td>4.5</td>
<td>6</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>ISC</td>
<td>VOUT Short to VCC, TA = 25°C</td>
<td></td>
<td>9.0</td>
<td>16</td>
<td>μA</td>
<td></td>
</tr>
</tbody>
</table>

### POWER SUPPLY

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Icc</td>
<td>Supply Current (Includes Ladder Current)</td>
<td></td>
<td>1.1</td>
<td>1.8</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>IS</td>
<td>ICLL = 640 kHz, VREF/2 = VC, TA = 25°C and CS = 5V</td>
<td></td>
<td>1.9</td>
<td>2.5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>IS</td>
<td>ADD804/04/04/LC/LCM/LC/LCMX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A GND point should always be wired to the O Gnd.

Note 3: A spare diode exists, internally, from VCC to Gnd and has a typical breakdown voltage of 7 VDC.

Note 4: For VCC(+) = VCC(-) the digital output code will be 0000 0000. Two analog diodes are used to each analog input (see block diagram). We ignored conduct for analog input voltages one diode drop below ground or one diode drop greater than the VCC voltage. Be careful, during testing at low VCC levels (1.3V) as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near 0V level. The spec allows 50 mV forward bias of anode diode. The means that as long as the analog VCC does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 Vdc to 5 VDC input voltage range we therefore require a maximum supply voltage of 4.550 VDC over temperature variations, input tolerance and loading.

Note 5: Accuracy is guaranteed at VCC = 640 kHz. At higher clock frequencies accuracy can degrade. For low clock frequencies, the duty cycle limits can be extended to as long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 4 clock periods may be required before the internal clock phases are proper to start the conversion process. The clock required is internally latched, see Figure 2 and section 2.6.

Note 7: The CS input is assumed to be connected to the WR strobe input and therefore timing is dependent on the WR pulse width. An arbitrary wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the WR pulse (see timing diagrams).

Note 8: None of these ADs require a zero adjust (see section 2.2.1). To obtain zero codes at other analog input voltages see section 2.5 and Figure 2.

Note 9: The VIN/2 pin is the center point of a two resistor divider connected from VCC to ground. Each resistor is 2.5k, except for the ADD804/LCMX where each resistor is 1k. Total selected input resistance is the sum of the two equal resistors.
Typical Performance Characteristics

- Logic Input Threshold Voltage vs. Supply Voltage
- Delay From Falling Edge of RD to Output Data Valid vs. Load Capacitance
- CLK IN Schmitt Trip Levels vs. Supply Voltage
- fCLK vs. Clock Capacitor
- Full-Scale Error vs Conversion Time
- Effect of Unadjusted Offset Error vs VREF/2 Voltage
- Output Current vs Temperature
- Power Supply Current vs Temperature (Note 9)
- Linearity Error at Low VREF/2 Voltages
TRI-STATE Test Circuits and Waveforms

Timing Diagrams (All timing is measured from the 50% voltage points)

Output Enable and Reset INTA

Note: Read probe must occur 4 clock periods (B/CLK) after assertion of interrupt to guarantee reset of INTA.
LAMPIRAN B

PERANGKAT LUNAK
Listing programs

WR_CTRL_REG EQU 2000H % Inisialisasi prosesor 87C51 &
WR_DATA_REG EQU 2001H
RD_CTRL_REG EQU 2002H
RD_DATA_REG EQU 2003H
TIME_DELAY EQU 21H
DSP1 EQU 22H
DSP2 EQU 23H
DSP3 EQU 24H
DSP4 EQU 25H
BUFFER EQU 28H
INPUT EQU 29H
PRINT_COUNTER EQU 30H

ORG 0000H
AJMP MAIN

ORG 100H

MAIN:
MOV SP,#70H
ACALL INIT_LCD

MOV A,#00001100B
ACALL CTRL_OUT

LOGO:
ACALL CLEAR_DISPLAY % mencetak header logo %
ACALL PRT_TITLE1
ACALL DELAY_5S
ACALL CLEAR_DISPLAY
ACALL PRT_TITLE2
ACALL DELAY_5S
ACALL CLEAR_DISPLAY

MEASURE:
ACALL READ_P1 % membaca ADC dan
MOV BUFFER,INPUT % menampilkan di LCD %
ACALL TOTAL_RESULT
ACALL DELAY_2S
SJMP MEASURE

READ_P1:
PUSH DPH % membaca pada Port P1 %
PUSH DPL
MOV A,P1
MOV INPUT,A
CLR C
SUBB A,#3
JNC REAL_DISP
MOV INPUT,#0
SJMP EXIT_RD_P1

REAL_DISP:
MOV A,#255
SUBB A,INPUT
MOV INPUT,A

REAL_DISP:
Listing programs

CLR C
SUBB A,#200
JC LOW_DISP

HIGH_DISP:
SJMP EXIT_RD_P1

LOW_DISP:
MOV A,INPUT
MOV B,#6
DIV AB
MOV INPUT,A

EXIT_RD_P1:
POP DPL
POP DPH
RET

TOTAL_RESULT:
PUSH DPH
PUSH DPL
MOV R7,#0
ACALL LOCATE1
MOV DPTR,#OUTPUT
ACALL OUT_CHAR

MOV R7,#0
ACALL LOCATE2
MOV DPTR,#OUTPUT2
ACALL OUT_CHAR

MOV R7,#5
ACALL LOCATE2
MOV A,DSP3
ACALL DATA_OUT

MOV R7,#6
ACALL LOCATE2
MOV A,DSP2
ACALL DATA_OUT

MOV R7,#7
ACALL LOCATE2
MOV A,DSP1
ACALL DATA_OUT

POP DPL
POP DPH
RET

PRT_TITLE1:
PUSH DPH
PUSH DPL
MOV R7,#0
ACALL LOCATE1
MOV DPTR,#HEADER1
ACALL OUT_CHAR
MOV R7,#0
ACALL LOCATE2
MOV DPTR,#HEADER2
ACALL OUT_CHAR
ACALL DELAY_5S
ACALL CLEAR_DISPLAY

MOV R7, #0
ACALL LOCATE1
MOV DPTR, #HEADER3
ACALL OUT_CHAR
MOV R7, #0
ACALL LOCATE2
MOV DPTR, #HEADER4
ACALL OUT_CHAR

ACALL DELAY_5S
ACALL CLEAR_DISPLAY

POP DPL
POP DPH
RET

PRT_TITLE2:
PUSH DPH
PUSH DPL

MOV R7, #0
ACALL LOCATE1
MOV DPTR, #HEADER5
ACALL OUT_CHAR
MOV R7, #0
ACALL LOCATE2
MOV DPTR, #HEADER6
ACALL OUT_CHAR

ACALL DELAY_5S
ACALL CLEAR_DISPLAY

MOV R7, #0
ACALL LOCATE1
MOV DPTR, #HEADER7
ACALL OUT_CHAR
MOV R7, #0
ACALL LOCATE2
MOV DPTR, #HEADER8
ACALL OUT_CHAR

ACALL DELAY_5S
ACALL CLEAR_DISPLAY

POP DPL
POP DPH
RET
INIT_LCD:
  PUSH DPH
  PUSH DPL
  PUSH PSW
  PUSH ACC
  MOV R0,#OFFH
  ACALL DELAY_LOOP
  MOV A,#00111000B
  ACALL CTRL_OUT
  MOV R0,#50H
  ACALL DELAY_LOOP
  MOV A,#00111000B
  ACALL CTRL_OUT
  MOV A,#00111000B
  ACALL CTRL_OUT
  MOV A,#00001000B
  ACALL CTRL_OUT
  MOV A,#00000001B
  ACALL CTRL_OUT
  MOV A,#00000110B
  ACALL CTRL_OUT
  POP ACC
  POP PSW
  POP DPL
  POP DPH
  RET

DELAY_LOOP:
  PUSH DPH
  PUSH DPL

DEL_LOOP:
  DEC R0
  NOP
  NOP
  NOP
  CJNE R0,#0H,DEL_LOOP
  POP DPL
  POP DPH
  RET

CLEAR_DISPLAY:
  PUSH DPH
  PUSH DPL
  MOV A,#00000001B
  ACALL CTRL_OUT
  MOV R0,#OFFH
  ACALL DELAY_LOOP
  POP DPL
  POP DPH
  RET

DELAY_5S:
  PUSH DPH
  PUSH DPL
  PUSH ACC
  PUSH PSW

Listing programs

% inisialisasi LCD %

% membersihkan layar %

% delay 5 detik %
DELI:

DEL2:
MOV A,#0FFH
MOV B,#0FFH
DJNZ B, $
DJNZ ACC, DEL2
DJNZ R5, DEL3
POP PSW
POP ACC
POP DPL
POP DPH
RET

DELAY_2S:
PUSH DPH
% delay 2 detik %
PUSH DPL
PUSH ACC
PUSH PSW
MOV R5, #06H

DEL3:
MOV A,#0FFH

DEL4:
MOV B,#0FFH
DJNZ B, $
DJNZ ACC, DEL4
DJNZ R5, DEL3
POP PSW
POP ACC
POP DPL
POP DPH
RET

DELAY_1S:
PUSH DPH
% delay 1 detik %
PUSH DPL
PUSH ACC
PUSH PSW
MOV R5, #03H

DEL5:
MOV A,#0FFH

DEL6:
MOV B,#0FFH
DJNZ B, $
DJNZ ACC, DEL6
DJNZ R5, DEL5
POP PSW
POP ACC
POP DPL
POP DPH
RET

DELAY:
PUSH DPH
PUSH DPL
PUSH ACC
PUSH PSW
MOV R5, TIME_DELAY

DEL7:
MOV A,#0FFH

DEL8:
MOV B,#0FFH
DJNZ B, $
DJNZ ACC, DEL8
DJNZ R5, DEL7
POP PSW
POP ACC
POP DPL
Listing programs

POP DPH
RET

HEADER1: DB 'MICROCONTROLLER', 'Karakter yang akan
dicetak di LCD %
HEADER2: DB 'DRIVEN'
HEADER3: DB 'DIGITAL IODIUM'
HEADER4: DB 'TESTER'
HEADER5: DB 'DESIGNED BY: '
HEADER6: DB 'ANGKA WIJAYA'
HEADER7: DB 'FTE UNIKA'
HEADER8: DB 'WIDYA MANDALA'
OUTPUT: DB 'IODIUM CONTAIN'
OUTPUT2: DB 'ppm'

END
LAMPIRAN C

TABEL INSTRUKSI LCD
### 2.4 Instruction Outline

#### Table 5 List of instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Code</th>
<th>Function</th>
<th>Execution time</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1) Display clear</td>
<td>RS 0 DB7 DB6 DB5 DB4 DB3 DB2 DB1</td>
<td>Clears all display and returns cursor to home position (address 0)</td>
<td>1.64 ms</td>
</tr>
<tr>
<td>(2) Cursor Home</td>
<td>RS 0 DB7 DB6 DB5 DB4 DB3 DB2 DB1</td>
<td>Returns cursor to home position. Shifted display returns to home position and DD RAM contents do not change.</td>
<td>1.64 ms</td>
</tr>
<tr>
<td>(3) Entry Mode Set</td>
<td>RS 0 DB7 DB6 DB5 DB4 DB3 DB2 DB1</td>
<td>Sets direction of cursor movement and whether display will be shifted when data is written or read</td>
<td>49 μs</td>
</tr>
<tr>
<td>(4) Display ON/OFF control</td>
<td>RS 0 DB7 DB6 DB5 DB4 DB3 DB2 DB1</td>
<td>Turns ON/OFF total display (D) and cursor (C), and makes cursor position column start blinking (B)</td>
<td>49 μs</td>
</tr>
<tr>
<td>(5) Cursor/Display Shift</td>
<td>RS 0 DB7 DB6 DB5 DB4 DB3 DB2 DB1</td>
<td>Moves cursor and shifts display without changing DD RAM contents</td>
<td>49 μs</td>
</tr>
<tr>
<td>(6) Function Set</td>
<td>RS 0 DB7 DB6 DB5 DB4 DB3 DB2 DB1</td>
<td>Sets interface data length (DL)</td>
<td>49 μs</td>
</tr>
<tr>
<td>(7) CG RAM Address Set</td>
<td>RS 0 DB7 DB6 DB5 DB4 DB3 DB2</td>
<td>Sets CG RAM address to start transmitting or receiving CG RAM data</td>
<td>49 μs</td>
</tr>
<tr>
<td>(8) DD RAM Address Set</td>
<td>RS 0 DB7 DB6 DB5 DB4 DB3 DB2</td>
<td>Sets DD RAM address to start transmitting or receiving DD RAM data</td>
<td>49 μs</td>
</tr>
<tr>
<td>(9) BF/Address Read</td>
<td>RS 0 DB7 DB6 DB5 DB4 DB3 DB2</td>
<td>Reads BF indicating module in internal operation and AC contents (used for both CG RAM and DD RAM)</td>
<td>0.3 μs</td>
</tr>
<tr>
<td>(10) Data Write to CG RAM or DD RAM</td>
<td>RS 0 DB7 DB6 DB5 DB4 DB3 DB2</td>
<td>Writes data into DD RAM or CG RAM</td>
<td>40 μs</td>
</tr>
<tr>
<td>(11) Data Read from CG RAM or DD RAM</td>
<td>RS 0 DB7 DB6 DB5 DB4 DB3 DB2</td>
<td>Reads data from DD RAM or CG RAM</td>
<td>40 μs</td>
</tr>
</tbody>
</table>

* : Invalid bit
A<sub>CG</sub> : CG RAM address
A<sub>DD</sub> : DD RAM address

---

- RS | Input
- DB7, DB6, DB5, DB4, DB3, DB2, DB1 | Bit

#### Instruction Codes

- C = 1 : Cursor ON
- C = 0 : Cursor OFF
- A<sub>CG</sub> : CG RAM address
- A<sub>DD</sub> : DD RAM address
- B = 1 : Blink ON
- B = 0 : Blink OFF
- DL = 1 : 8 bits
- DL = 0 : 4 bits
- SR = 1 : Display shift
- SR = 0 : No display shift
- S = 1 : Display ON
- S = 0 : Display OFF
- BF = 1 : Instruction can be accepted
- BF = 0 : Instruction is in progress
- RA = 1 : Right shift
- RA = 0 : Left shift
- SF = 1 : Internal operation
- SF = 0 : No internal operation

---

AN.No.1632-711E
Table 3  Correspondence between character codes and character patterns

<table>
<thead>
<tr>
<th>Upper bit 4 bit</th>
<th>Lower bit 4 bit</th>
<th>0000</th>
<th>0010</th>
<th>0011</th>
<th>0100</th>
<th>0101</th>
<th>0110</th>
<th>0111</th>
<th>1010</th>
<th>1011</th>
<th>1100</th>
<th>1101</th>
<th>1110</th>
<th>1111</th>
</tr>
</thead>
<tbody>
<tr>
<td>CG RAM (1)</td>
<td></td>
<td>0000</td>
<td>0011</td>
<td>0100</td>
<td>0101</td>
<td>0110</td>
<td>0111</td>
<td>1010</td>
<td>1011</td>
<td>1100</td>
<td>1101</td>
<td>1110</td>
<td>1111</td>
<td></td>
</tr>
<tr>
<td>(2)</td>
<td></td>
<td>1100</td>
<td>1101</td>
<td>1110</td>
<td>1111</td>
<td>1010</td>
<td>1011</td>
<td>1100</td>
<td>1101</td>
<td>1110</td>
<td>1111</td>
<td>1010</td>
<td>1011</td>
<td>1100</td>
</tr>
<tr>
<td>(3)</td>
<td></td>
<td>0000</td>
<td>0011</td>
<td>0110</td>
<td>0111</td>
<td>1000</td>
<td>1001</td>
<td>1100</td>
<td>1101</td>
<td>1110</td>
<td>1111</td>
<td>1010</td>
<td>1011</td>
<td>1100</td>
</tr>
<tr>
<td>(4)</td>
<td></td>
<td>0000</td>
<td>0011</td>
<td>0100</td>
<td>0101</td>
<td>0110</td>
<td>0111</td>
<td>1010</td>
<td>1011</td>
<td>1100</td>
<td>1101</td>
<td>1110</td>
<td>1111</td>
<td>1010</td>
</tr>
<tr>
<td>(5)</td>
<td></td>
<td>0000</td>
<td>0011</td>
<td>0100</td>
<td>0101</td>
<td>0110</td>
<td>0111</td>
<td>1010</td>
<td>1011</td>
<td>1100</td>
<td>1101</td>
<td>1110</td>
<td>1111</td>
<td>1010</td>
</tr>
<tr>
<td>(6)</td>
<td></td>
<td>0000</td>
<td>0011</td>
<td>0100</td>
<td>0101</td>
<td>0110</td>
<td>0111</td>
<td>1010</td>
<td>1011</td>
<td>1100</td>
<td>1101</td>
<td>1110</td>
<td>1111</td>
<td>1010</td>
</tr>
<tr>
<td>(7)</td>
<td></td>
<td>0000</td>
<td>0011</td>
<td>0100</td>
<td>0101</td>
<td>0110</td>
<td>0111</td>
<td>1010</td>
<td>1011</td>
<td>1100</td>
<td>1101</td>
<td>1110</td>
<td>1111</td>
<td>1010</td>
</tr>
<tr>
<td>(8)</td>
<td></td>
<td>0000</td>
<td>0011</td>
<td>0100</td>
<td>0101</td>
<td>0110</td>
<td>0111</td>
<td>1010</td>
<td>1011</td>
<td>1100</td>
<td>1101</td>
<td>1110</td>
<td>1111</td>
<td>1010</td>
</tr>
</tbody>
</table>
FOTO ALAT
<table>
<thead>
<tr>
<th>Nama</th>
<th>ANGKA WIJAYA ANGGARA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nrp</td>
<td>5103094038</td>
</tr>
<tr>
<td>Nirm</td>
<td>94.7.003.31073.06042</td>
</tr>
<tr>
<td>Alamat</td>
<td>BABATAN PANTAI UTARA XV / 5</td>
</tr>
<tr>
<td>Tempat / Tgl Lahir</td>
<td>KOTABARU, 26 MEI 1974</td>
</tr>
<tr>
<td>Agama</td>
<td>KATOLIK</td>
</tr>
<tr>
<td>Hobby</td>
<td>OLAH RAGA (BASKET)</td>
</tr>
</tbody>
</table>

Riwayat Pendidikan:

Lulus SD Negri Sebatung, Kotabaru, tahun 1988
Lulus SMP Negri I, Kotabaru, tahun 1991
Lulus SMA Negri I, Kotabaru, tahun 1994