LAMPIRAN III : LISTING PROGRAM

1. LAMPIRAN PROGRAM UTAMA DALAM BAHASA ASEMBLER.

PA EQU 4000H
PB EQU 4001H
PC EQU 4002H
PCW EQU 4003H
CW EQU 0090H
DPA DATA 0021H
DPB DATA 0022H
DPC DATA 0022H
I DATA 0023H
SENSOR DATA 0024H

; -------------------------------
; PROGRAM MEMORY
; -------------------------------
.CODE
ORG 2000H

Dell
MOV R2,#OFFH
MOV R3,#OFFH
DJNZ R3,$
DJNZ R2, Dell
AJMP Start

ORG 2100H

; -------------------------------
; Initialization Proc.
; -------------------------------

Init
MOV TMOD,#00100010B ; T1 mode2, T0 mode2
MOV TL1,#0FAH ; T1 mode2 generate BR=9600 Bps
MOV TH1,#0FAH
MOV TCON,#01000000B ; T1 on, T0 off

; -------------------------------
; Init. Serial
; -------------------------------

MOV SCON,#01010000B ; Model, REN
MOV PCON,#080H ; SMOD=0

; -------------------------------
; Init Interrupt
; -------------------------------

MOV IE,#00000000B
RET
sclk

MOV R2,#$80H
DJNZ R2,$
RET

;--------------------------------
; MAIN PROGRAM LOCATION
;--------------------------------
Start
MOV P1,#$00H
MOV SP,#$40H
MOV IE,#$00H
ACALL Init

;--------------------------------
; INISIALISASI PPI
;--------------------------------
MOV DPTR,#PCW
MOV A,#CW
MOVX @DPTR,A

;--------------------------------
; ULANG
;--------------------------------
ULANG
MOV A,#$00H
MOV P1,A
MOV DPB,#$00H ; kondisi awal Port A
MOV DPB,#$8FH ; AKTIFKAN CHENEL 0
MOV DPMB,#$FB
MOV A,DPB
MOVB @DPTR,A
ACALL CLKADC
JNB TI,$
CLR TI

MOV DPB,#$8FH ; AKTIFKAN CHENEL 0
MOV DPMB,#$FB
MOV A,DPB
MOVB @DPTR,A
ACALL CLKADC
JNB TI,$
CLR TI

MOV DPB,#$0CFH
MOV DPMB,#$FB
MOV A,DPB
MOVB @DPTR,A
ACALL CLKADC
JNB TI,$
CLR TI

CLR P1.1
MOV A,SBUF
JNB A.0,HIDUP
CLR P1.1
AJMP MATI

HIDUP
SETB P1.1
CLR RI
AJMP ULANG

MATI
CLR RI
AJMP ULANG

CLKADC
MOV DPTR,#PC
MOV A,#00H ; PL = 0
MOVX @DPTR,A
MOV DPTR,#PC
MOV A,#01H ; PL = 1
MOVX @DPTR,A

MOV I,#08H ; CLOCK 8 KALI
CLOCK1
CLR P1.0
ACALL SCLK
SETB P1.0
ACALL SCLK
DJNZ I,CLOCK1

MOV DPTR,#PA
MOVX A,@DPTR
MOV DPA,A
MOV SBUF,DPA

MOV I,#02H ; CLOCK 2 KALI
CLOCK2
CLR P1.0
ACALL SCLK
SETB P1.0
ACALL SCLK
DJNZ I,CLOCK2
RET

END
2. PROGRAM PENGOLAHAN DATA DAN TAMPILAN SUHU DALAM

BAHASA PASCAL

PROGRAM TAMPILAN_SUHU;
uses crt,dos,GRAPH;
const RX_Buffer = $2F8; { RX Buffer COM2 }
TX_Buffer = $2F8; { TX Buffer COM2 }
Int_Enbl_Reg = $2F9; { Interrupt Enable Register }
Int_Indent_Reg = $3FA; { Interrupt Indentification Register }
Line_Cont_Reg = $2FB; { Line Control Register }
Modem_Const_Reg = $2FC; { Modem Control Register }
Line_Stat_Reg = $2FD; { Line Status Register }
Modem_Stat_Reg = $2FE; { Modem Status Register }
Gray10 : FillPatternType = ($AA, $AA, $AA, $AA, $AA, $AA, $AA, $AA, $AA, $AA);

type
complex = record
a,b : real;
c,d : byte;
end;

var data10,input : array [0..1023] of integer;
T,L : array [0..550] of REAL;
vT,vL : array [0..550] of byte;
gain : array [0..99] of word;
IntOC_Save : pointer; {interrupt service routine IRQ3 }
i, data,S : byte;
regs: registers;
Grdriver,Grmode: integer;
dummy : byte;
TERMO,LM,LM1,M: real;
tegangan:real;
DATA0,DATA1,FLAG:BYTE;
fil : file of complex;
data : complex;
n,x: word;
tempx, tempy: word;

procedure Intr_Com; interrupt;
begnin
data:=port[RX_Buffer]; { baca buffer RX }
port[$20]:=$20; { End Of Interrupt 8259 }
IF DATA=255 THEN FLAG:=0;
CASE FLAG OF
0 : FLAG:=1;
1 : BEGIN
FLAG:=2;
DATA0:=DATA;
TERMO := (data0*0.595041)+28;
END;
2 : BEGIN
FLAG :=0;

end;
DATA1:=DATA;
LM := ( DATA1*0.6603) - 55.849057;
END;
end;

Procedure Open_Com;
var dummy : byte;
begin
GetIntVec{$OB,IntOC_save);
SetIntVec{$OB,Addr(Intr_com)));
port[Line_Cnt_Reg ]:=80; { D7=1 set baud rate 9600 bps}
port[TX_Buffer ]:=OB; { divisor LSB $2F8=$OB }
port[IntEnbl_Reg ]:=0; { divisor MSB $2F9=0 }
port[Line_Cnt_Reg ]:=03; { 8 bit data, 1 stop bit, no parity }
port[IntEnbl_Reg ]:=01; { enable interrupt saat ada data RX }
port[Modem_Cnt_Reg ]:=09; { D0 = DTR = 0 => 89C51= Reset }
dummy:=port[RX_Buffer]; { kosongkan RX buffer }
port[$21] :=port[$21] and $F7; { Enable IRQ3 }
end;

Procedure Close_Com;
begin
port[$21] :=port[$21] or $08; { Disable IRQ3 }
SetIntvec($OB,IntOC_save);
end;

procedure Area;
var x,y:integer;
begin
SetFillPattern(Gray10,black); {rectangle}
Bar(50,60,570,360);
setColor(yellow);
line(50,40,50,437); { sb y}
line(50,437,480,437); { sb x}
setColor(yellow);
for y:=0to24 do line(51,53+(y*16),55,53+(y*16)); { grs kcl sb y}
for y:=0to20do line(50+(y*20),432,50+(y*20),437); { grs kcl sb x}
setColor(darkgray);
for x:=0to11 do line(55,53+(x*32),480,53+(x*32)); { hor line}
for x:=0 to 9 do line(90+(x*40),55,90+(x*40),437); { ver line}
outtextxy(150,15 ,’ GRAFIK PENGUKURAN TEGANGAN - SUHU’);
setColor(white);
outtextxy(12,26 ,’ Volt’);
outtextxy(10,50 ,’ 4.00’);
outtextxy(10,82 ,’ 3.66’);
outtextxy(10,114 ,’ 3.33’);
outtextxy(10,146 ,’ 3.00’);
outtextxy(10,178 ,’ 2.67’);
outtextxy(10,210 ,’ 2.33’);
outtextxy(10,242 ,’ 2.00’);
outtextxy(10,274 ,’ 1.67’);
outtextxy(10,306 ,’ 1.33’);
procedure InisialisasiGraph;
begin
  grdriver:= detect;
  grmode := VGAHi;
  Initgraph(grDriver,grMode,'c:\tp\bgi');
end:

procedure Capture;
begin
  assign(fil, 'SUHU.dat');
  rewrite(fil);
end;

{Program Utama}
begin
  clrscr;
  write(' MASUKAN SUHU MAX: ');READLN(S);
  CLRSCR;
  TEXTCOLOR(7);
  n:=0;
  writeln(' DATA PENGUKURAN SUHU ');
  capture;
  Open_com;

  repeat
    if LM>S then
      PORT[TX_BUFFER]:=$0
    else
      begin
      end
PORT[TX_BUFFER] := $1;
GOTOXY(10, 8); WRITELN('DATA 0 = ', DATA0:3);
GOTOXY(10, 10); WRITELN('TERMOKOPEL = ', TERMO:3:0);
GOTOXY(10, 12); WRITELN('DATA 1 = ', DATA1:3);
GOTOXY(10, 14); WRITELN('LM335 = ', LM:3:0);
l[n] := lm;
t[n] := termo;
v[l][n] := datal;
vt[n] := data0;
with dat do
begin
  a := lm;
  b := termo;
  c := datal;
  d := data0;
end;
write(fil, dat);
delay(1000);
inc(n);
END;
UNTIL (KEYPRESSED);
Close_com;
inisialisasigraph;
area;
x := 1;
repeat
  setcolor(10);
  if x = 1 then
    begin
      tempx := 52 + round(4*l[x]);
      tempy := 502 - round(1.84 * vl[x]);
      moveto(tempx, tempy);
    end
  else
    lineto(52 + round(4*l[x]), 502 - round(1.84 * vl[x]));
    inc(x);
  until x = n;
x := 1;
repeat
  setcolor(7);
  if x = 1 then
    begin
      tempx := 52 + round(4*t[x]);
      tempy := 427 - round(1.43 * vt[x]);
      moveto(tempx, tempy);
    end
  else
    lineto(52 + round(4*t[x]), 427 - round(1.43 * vt[x]));
    inc(x);
  until x = n;
readln;
close(fil);
closegraph;
end.
General Description

The MAX1112/MAX1113 are low-power, 8-bit, 8-channel analog-to-digital converters (ADCs) that feature an internal track/hold, voltage reference, clock, and serial interface. They operate from a single +4.5V to +5.5V supply and consume only 135μA while sampling at rates up to 50ksps. The MAX1112’s 8 analog inputs and the MAX1113’s 4 analog inputs are software-configurable, allowing unipolar/bipolar and single-ended/differential operation. Successive-approximation conversions are performed using either the internal clock or an external serial interface clock. The full-scale analog input range is determined by the 4.096V internal reference, or by an externally applied reference ranging from 1V to VDD. The 4-wire serial interface is compatible with the SPI™, QSPI™, and MICROWIRE™ serial-interface standards. A serial-strobe output provides the end-of-conversion signal for interrupt-driven processors.

The MAX1112/MAX1113 have a software-programmable, 2μA automatic power-down mode to minimize power consumption. Using power-down, the supply current is reduced to 13μA at 1ksps, and only 82μA at 10ksps. Power-down can also be controlled using the SHDN input pin. Accessing the serial interface automatically powers up the device.

The MAX1112 is available in 20-pin SSOP and DIP packages. The MAX1113 is available in small 16-pin QSOP and DIP packages.

Features

- +4.5V to +5.5V Single Supply
- Low Power: 135μA at 50ksps
  13μA at 1ksps
- 8-Channel Single-Ended or 4-Channel Differential Inputs (MAX1112)
- 4-Channel Single-Ended or 2-Channel Differential Inputs (MAX1113)
- Internal Track/ Hold; 50kHz Sampling Rate
- Internal 4.096V Reference
- SPI/QSPI/MICROWIRE-Compatible Serial Interface
- Software-Configurable Unipolar or Bipolar Inputs
- Total Unadjusted Error: ±1LSB (max)
  ±0.3LSB (typ)

Ordering Information

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP. RANGE</th>
<th>PIN-PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX1112CPP</td>
<td>0°C to +70°C</td>
<td>20 Plastic DIP</td>
</tr>
<tr>
<td>MAX1112CAP</td>
<td>0°C to +70°C</td>
<td>20 SSOP</td>
</tr>
<tr>
<td>MAX1112CD</td>
<td>0°C to +70°C</td>
<td>Dice*</td>
</tr>
</tbody>
</table>

*Dice are specified at TA = +25°C, DC parameters only.

Ordering Information continued at end of data sheet.

Applications

- Portable Data Logging
- Hand-Held Measurement Devices
- Medical Instruments
- System Diagnostics
- Solar-Powered Remote Systems
- 4-20mA-Powered Remote Data-Acquisition Systems

Pin Configurations appear at end of data sheet.

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# +5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

## ABSOLUTE MAXIMUM RATINGS

- V<sub>DD</sub> to AGND: -0.3V to 6V
- AGND to DGND: 0.3V to 3V
- CH0-CH7, COM, REFIN,
- REFOUT to AGND: -0.3V to (V<sub>DD</sub> + 0.3V)
- Digital Inputs to DGND: -0.3V to 6V
- Continuous Power Dissipation (TA = +70°C):
  - 16 Plastic DIP (derate 1.11 mW/°C above +70°C)...
  - 20 Plastic DIP (derate 1.11 mW/°C above +70°C) ...
  - 20 SSOP (derate 0.00 mW/°C above +70°C) ...
  - 20 CERDIP (derate 1.11 mW/°C above +70°C) ...
- AGND to DGND, CHO-CH7, COM REFIN:
- Digital Outputs to DGND:
- REFOUT to AGND:
- Operating Temperature Ranges:
  - MAX1112C_P/MAX1113C_E: 0°C to +70°C
  - MAX1112E_P/MAX1113E_E: -40°C to +85°C
  - MAX1112M_P/MAX1113M_E: -55°C to +125°C
- Storage Temperature Range: -65°C to +150°C
- Lead Temperature (soldering, 10sec): +300°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

**DC ACCURACY**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td></td>
<td></td>
<td>8</td>
<td></td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>Relative Accuracy (Note 1)</td>
<td>INL</td>
<td></td>
<td>±0.1</td>
<td>±0.5</td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>Differential Linearity</td>
<td>DNL</td>
<td>No missing codes over temperature</td>
<td>±1</td>
<td></td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>Offset Error</td>
<td></td>
<td></td>
<td>±0.3</td>
<td>±1</td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>Gain Error (Note 2)</td>
<td></td>
<td>Internal or external reference</td>
<td>±1</td>
<td></td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>Gain Temperature Coefficient</td>
<td></td>
<td>External reference, 4.096V</td>
<td>±0.8</td>
<td></td>
<td></td>
<td>ppm/°C</td>
</tr>
<tr>
<td>Total Unadjusted Error</td>
<td>TUE</td>
<td>MAX1111_CE</td>
<td>±0.3</td>
<td>±1</td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>Channel-to-Channel</td>
<td></td>
<td>Offset Matching</td>
<td>±0.1</td>
<td></td>
<td></td>
<td>LSB</td>
</tr>
</tbody>
</table>

**DYNAMIC SPECIFICATIONS**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>VALUE</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal-to-Noise and Distortion Ratio</td>
<td>SINAD</td>
<td></td>
<td>49</td>
<td>dB</td>
</tr>
<tr>
<td>Total Harmonic Distortion (up to the 5th harmonic)</td>
<td>THD</td>
<td></td>
<td>-70</td>
<td>dB</td>
</tr>
<tr>
<td>Spurious-Free Dynamic Range</td>
<td>SFDR</td>
<td></td>
<td>68</td>
<td>dB</td>
</tr>
<tr>
<td>Channel-to-Channel Crosstalk</td>
<td>VCCH</td>
<td>4.096Vp-p, 25kHz (Note 3)</td>
<td>-75</td>
<td>dB</td>
</tr>
<tr>
<td>Small-Signal Bandwidth</td>
<td></td>
<td>-3dB rolloff</td>
<td>1.5</td>
<td>MHz</td>
</tr>
<tr>
<td>Full-Power Bandwidth</td>
<td></td>
<td></td>
<td>800</td>
<td>kHz</td>
</tr>
</tbody>
</table>
## +5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

### ELECTRICAL CHARACTERISTICS (continued)

(V\text{DD} = +4.5\text{V} to +5.5\text{V}; unipolar input mode: \text{COV} = 0\text{V}; \text{f}_{\text{CLK}} = 500kHz; external clock (50\% duty cycle); 10 clocks/conversion cycle (50ksps); 1\text{pF} capacitor at \text{REFOUT}; T_A = T_{\text{MIN}} to T_{\text{MAX}} unless otherwise noted.)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CONVERSION RATE</strong></td>
<td></td>
<td>Internal clock</td>
<td>25</td>
<td>55</td>
<td></td>
<td>\mu s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>External clock, 500kHz, 10 clocks/conversion</td>
<td>20</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Track/Hold Acquisition Time</strong></td>
<td>T\text{ACQ}</td>
<td>External clock, 2MHz</td>
<td>1</td>
<td></td>
<td></td>
<td>\mu s</td>
</tr>
<tr>
<td><strong>Aperture Delay</strong></td>
<td></td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><strong>Aperture Jitter</strong></td>
<td></td>
<td>&lt;50</td>
<td></td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td><strong>Internal Clock Frequency</strong></td>
<td></td>
<td>400</td>
<td></td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td><strong>External Clock-Frequency Range</strong></td>
<td>(Note 5)</td>
<td>50</td>
<td>500</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
</tbody>
</table>

#### ANALOG INPUT

| INPUT VOLTAGE RANGE | Unipolar input, \text{COM} = 0\text{V} | 0 | | | V |
| | Bipolar input, \text{COM} = \text{VREFIN} / 2 | | | \text{COM} ± \text{VREFIN} / 2 | |

| MULTIPLEXER LEAKAGE CURRENT | On/off leakage current, \text{VCH} = 0\text{V} or \text{VDD} | | \pm0.01 | | \mu A |

| INPUT CAPACITANCE | | | 18 | | \text{pF} |

#### INTERNAL REFERENCE

| \text{REFOUT} Voltage | | 3.936 | 4.096 | 4.256 | V |
| \text{REFOUT} Short-Circuit Current | | | 6 | | mA |
| \text{REFOUT} Temperature Coefficient | | | | \pm30 | | ppm/\degree C |
| Load Regulation (Note 7) | | 0mA to 0.5mA output load | | 4.5 | | mV |
| Capacitive Bypass at \text{REFOUT} | | | 1 | | \mu F |

#### EXTERNAL REFERENCE AT \text{REFIN}

| INPUT VOLTAGE RANGE | | 1 | | \text{VDD} + 50mV | | V |
| INPUT CURRENT | (Note 8) | | | 1 | 20 | \mu A |

### POWER REQUIREMENTS

| SUPPLY VOLTAGE | \text{VDD} | 4.5 | 5.5 | V |
| SUPPLY CURRENT | I\text{DD} | Full-scale input \text{CLOAD} = 10\text{pF} | Operating mode | 135 | 250 | \mu A |
| | | Reference disabled | Software | 95 | | |
| | | Power-down | SHDN at DGND | 2 | 3.2 | 10 |
| POWER-SUPPLY REJECTION (Note 9) | PSR | \text{VDD} = 4.5\text{V} to 5.5\text{V}; external reference, 4.096\text{V}; full-scale input | | \pm0.4 | | \pm4 | mV |
+5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

ELECTRICAL CHARACTERISTICS (continued)

(VDD = +4.5V to +5.5V, unipolar input mode; COM = 0V; fSCLK = 500kHz, external clock (50% duty cycle); 10 clocks/conversion cycle (50ksps); 1μF capacitor at REFOUT, TA = TMIN to TMAX unless otherwise noted.)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIGITAL INPUTS: DIN, SCLK, CS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DIN, SCLK, CS Input High Voltage</td>
<td>Vih</td>
<td></td>
<td>3</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>DIN, SCLK, CS Input Low Voltage</td>
<td>Vil</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>DIN, SCLK, CS Input Hysteresis</td>
<td>VHyst</td>
<td></td>
<td>0.2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>DIN, SCLK, CS Input Leakage</td>
<td>VIN</td>
<td>Digital inputs = 0V or VDD</td>
<td>±1</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>DIN, SCLK, CS Input Capacitance</td>
<td>Cin</td>
<td>(Note 5)</td>
<td>15</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>SHDN INPUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SHDN Input High Voltage</td>
<td>Vsh</td>
<td></td>
<td>VDD - 0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SHDN Input Mid-Voltage</td>
<td>Vsm</td>
<td></td>
<td>1.1</td>
<td>VDD - 1.1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SHDN Voltage, Floating</td>
<td>Vflt</td>
<td>SHDN = open</td>
<td>VDD/2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SHDN Input Low Voltage</td>
<td>Vsl</td>
<td></td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SHDN Input Current</td>
<td></td>
<td></td>
<td>±4</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>SHDN Maximum Allowed Leakage for Mid-Input</td>
<td></td>
<td>SHDN = open</td>
<td>±100</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>DIGITAL OUTPUTS: DOUT, SSTRB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Low Voltage</td>
<td>Vol</td>
<td></td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output High Voltage</td>
<td>Voh</td>
<td></td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Three-State Leakage Current</td>
<td>Il</td>
<td>CS = VDD</td>
<td>±0.01</td>
<td>±10</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>Three-State Output Capacitance</td>
<td>Cout</td>
<td>CS = VDD (Note 5)</td>
<td>15</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>
+5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

TIMING CHARACTERISTICS (Figures 8 and 9)

(VOH = +4.5V to +5.5V, TA = TMIN to TMAX, unless otherwise noted.)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Track/Hold Acquisition Time</td>
<td>tACQ</td>
<td>Figure 1.</td>
<td>1</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>DIN to SCLK Setup</td>
<td>tDS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>DIN to SCLK-Hold</td>
<td>tDH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>SCLK Fall to Output Data Valid</td>
<td>tDO</td>
<td>Figure 1. CLOAD = 100pF</td>
<td>220</td>
<td>200</td>
<td>240</td>
<td>ns</td>
</tr>
<tr>
<td>CS Fall to Output Enable</td>
<td>tDV</td>
<td>Figure 1. CLOAD = 100pF</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CS Rise to Output Disable</td>
<td>tTR</td>
<td>Figure 2. CLOAD = 100pF</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CS to SCLK Rise Setup</td>
<td>tCSS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>SCLK Pulse Width High</td>
<td>tCH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>SCLK Pulse Width Low</td>
<td>tCL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>SCLK Fall to SSTRB</td>
<td>tSSTRB</td>
<td>CLOAD = 100pF</td>
<td>240</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CS Fall to SSTRB Output Enable</td>
<td>tSDV</td>
<td>Figure 1, external clock mode only, CLOAD = 100pF</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CS Rise to SSTRB Output Disable (Note 5)</td>
<td>tSTR</td>
<td>Figure 2, external clock mode only, CLOAD = 100pF</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>SSTRB Rise to SCLK Rise (Note 5)</td>
<td>tSCK</td>
<td>Figure 11, internal clock mode only</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Wakeup Time</td>
<td>tWAKE</td>
<td>External reference</td>
<td>20</td>
<td></td>
<td>24</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Internal reference (Note 10)</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Note 1: Relative accuracy is the analog value's deviation (at any code) from its theoretical value after the full-scale range is calibrated.
Note 2: VREFIN = 4.096V, offset nulled.
Note 3: On-channel grounded; sine wave applied to all off-channels.
Note 4: Conversion time is defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
Note 5: Guaranteed by design. Not subject to production testing.
Note 6: Common-mode range for the analog inputs is from AGND to VDD.
Note 7: External load should not change during the conversion for specified accuracy.
Note 8: External reference at 4.096V, full-scale input, 500kHz external clock.
Note 9: Measured as | VFS (4.5V) - VFS (5.5V) |.
Note 10: 1µF at REFOUT: internal reference settling to 0.5LSB.
**+5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs**

**Typical Operating Characteristics**

(Vdd = +5.0V; fSCLK = 500kHz; external clock (50% duty cycle); RL = ∞; TA = +25°C, unless otherwise noted.)
+5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

Pin Description

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX1112</td>
<td>MAX1113</td>
<td></td>
</tr>
<tr>
<td>1-4</td>
<td>CH0-CH3</td>
<td>Sampling Analog Inputs</td>
</tr>
<tr>
<td>5-8</td>
<td>CH14-CH7</td>
<td>Sampling Analog Inputs</td>
</tr>
<tr>
<td>9</td>
<td>COM</td>
<td>Ground Reference for Analog Inputs. Sets zero-code voltage in single-ended mode. Must be stable to ±0.5LSB.</td>
</tr>
<tr>
<td>10</td>
<td>SHDN</td>
<td>Three-Level Shutdown Input. Normally floats. Pulling SHDN low shuts the MAX1112/MAX1113 down to 10µA (max) supply current; otherwise, the devices are fully operational. Pulling SHDN high shuts down the internal reference.</td>
</tr>
<tr>
<td>11</td>
<td>REFIN</td>
<td>Reference Voltage Input for Analog-to-Digital Conversion. Connect to REFIN to use the internal reference.</td>
</tr>
<tr>
<td>12</td>
<td>REFOUT</td>
<td>Internal Reference Generator Output. Bypass with a 1µF capacitor to AGND.</td>
</tr>
<tr>
<td>13</td>
<td>AGND</td>
<td>Analog Ground</td>
</tr>
<tr>
<td>14</td>
<td>DGND</td>
<td>Digital Ground</td>
</tr>
<tr>
<td>15</td>
<td>DOUT</td>
<td>Serial-Data Output: Data is clocked out on SCLK's falling edge. High impedance when CS is high.</td>
</tr>
<tr>
<td>16</td>
<td>SSTRB</td>
<td>Serial-Strobe Output. In internal clock mode, SSTRB goes low when the MAX1112/MAX1113 begin the A/D conversion and goes high when the conversion is complete. In external clock mode, SSTRB pulses high for two clock periods before the MSB is shifted out. High impedance when CS is high (external clock mode only).</td>
</tr>
<tr>
<td>17</td>
<td>DIN</td>
<td>Active-Low Chip Select. Data is not clocked into DIN unless CS is low. When CS is high, DOUT is high impedance.</td>
</tr>
<tr>
<td>18</td>
<td>CS</td>
<td>Serial-Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed (duty cycle must be 45% to 55%).</td>
</tr>
<tr>
<td>19</td>
<td>SCLK</td>
<td>Positive Supply Voltage, +4.5V to +5.5V</td>
</tr>
</tbody>
</table>

Figure 1. Load Circuits for Enable Time

Figure 2. Load Circuits for Disable Time
**Detailed Description**

The MAX1112/MAX1113 analog-to-digital converters (ADCs) use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to an 8-bit digital output. A flexible serial interface provides easy interface to microprocessors (µPs). Figure 3 shows the Typical Operating Circuit.

**Pseudo-Differential Input**

The sampling architecture of the ADC's analog comparator is illustrated in Figure 4, the equivalent input circuit. In single-ended mode, IN+ is normally switched to the selected input channel, CH0, and IN- is switched to COM. In differential mode, IN+ and IN- are selected from the following pairs: CH0/CH1, CH2/CH3, CH4/CH5, and CH6/CH7. Configure the MAX1112 channels with Table 1 and the MAX1113 channels with Table 2.

In differential mode, IN- and IN+ are internally switched to either of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1 LSB for best results) with respect to AGND during a conversion. To accomplish this, connect a 0.1 µF capacitor from IN-(the selected analog input) to AGND if necessary. During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor CHOLD. The acquisition interval spans two SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on CHOLD as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching CHOLD from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply COM. This unbalances node ZERO at the input of the comparator. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 8-bit resolution. This action is equivalent to transferring a charge of 18pF x (VIN+ - VIN-) from CHOLD to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

**Track/Hold**

The T/H enters its tracking mode on the falling clock edge after the sixth bit of the 8-bit control byte has been shifted in. It enters its hold mode on the falling clock edge after the eighth bit of the control byte has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to COM, and the converter samples the "+" input; if it is set up for differential inputs, IN- connects to the "-" input, and the difference (IN+ - IN-) is sampled. At the end of the conversion, the positive input connects back to IN+, and CHOLD charges to the input signal.

---

**Figure 3. Typical Operating Circuit**

---

**Figure 4. Equivalent Input Circuit**
### Table 1a. MAX1112 Channel Selection in Single-Ended Mode (SGL/DIF = 1)

<table>
<thead>
<tr>
<th>SEL2</th>
<th>SEL1</th>
<th>SEL0</th>
<th>CH0</th>
<th>CH1</th>
<th>CH2</th>
<th>CH3</th>
<th>CH4</th>
<th>CH5</th>
<th>CH6</th>
<th>CH7</th>
<th>COM</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>+</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
<td>+</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
<td>+</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>+</td>
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<tr>
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<td>1</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>+</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>+</td>
<td></td>
</tr>
</tbody>
</table>

### Table 1b. MAX1112 Channel Selection in Differential Mode (SGL/DIF = 0)

<table>
<thead>
<tr>
<th>SEL2</th>
<th>SEL1</th>
<th>SEL0</th>
<th>CH0</th>
<th>CH1</th>
<th>CH2</th>
<th>CH3</th>
<th>CH4</th>
<th>CH5</th>
<th>CH6</th>
<th>CH7</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>+</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
<td>+</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
<td>+</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
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<td></td>
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</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td>+</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>+</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td>+</td>
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<td>1</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table 2a. MAX1113 Channel Selection in Single-Ended Mode (SGL/DIF = 1)

<table>
<thead>
<tr>
<th>SEL2</th>
<th>SEL1</th>
<th>SEL0</th>
<th>CH0</th>
<th>CH1</th>
<th>CH2</th>
<th>CH3</th>
<th>COM</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>X</td>
<td>+</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
<td></td>
<td>+</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td></td>
<td></td>
<td>+</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td>+</td>
<td></td>
</tr>
</tbody>
</table>

### Table 2b. MAX1113 Channel Selection in Differential Mode (SGL/DIF = 0)

<table>
<thead>
<tr>
<th>SEL2</th>
<th>SEL1</th>
<th>SEL0</th>
<th>CH0</th>
<th>CH1</th>
<th>CH2</th>
<th>CH3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>X</td>
<td>+</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td></td>
<td>+</td>
<td></td>
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<tr>
<td>1</td>
<td>0</td>
<td>X</td>
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<td></td>
<td>+</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be allowed between conversions. The acquisition time, \( t_{ACO} \), is the minimum time needed for the signal to be acquired. It is calculated by:

\[
t_{ACO} = 6 \times (R_s + R_n) \times 18\text{pF}
\]

where \( R_n = 5.5k\Omega \), \( R_s \) = the source impedance of the input signal, and \( t_{ACO} \) is never less than 1\( \mu \text{s} \). Note that source impedances below 2.4k\( \Omega \) do not significantly affect the AC performance of the ADC.

**Input Bandwidth**

The ADC's input tracking circuitry has a 1.5MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

**Analog Inputs**

Internal protection diodes, which clamp the analog input to \( V_{DD} \) and AGND, allow the channel input pins to swing from \((\text{AGND} - 0.3V)\) to \((V_{DD} + 0.3V)\) without damage. However, for accurate conversions near full scale, the inputs must not exceed \( V_{DD} \) by more than 50mV or be lower than AGND by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off channels over 2mA.

The MAX1112/MAX1113 can be configured for differential or single-ended inputs with bits 2 and 3 of the control byte (Table 3). In single-ended mode, analog inputs are internally referenced to COM with a full-scale input range from COM to \( V_{REFIN} \) + COM. For bipolar operation, set COM to \( V_{REFIN} / 2 \).

In differential mode, choosing unipolar mode sets the differential input range at 0V to \( V_{REFIN} \). In unipolar mode, the output code is invalid (code zero) when a negative differential input voltage is applied. Bipolar mode sets the differential input range to \( \pm V_{REFIN} / 2 \). Note that in this mode, the common-mode input range includes both supply rails. Refer to Table 4 for input voltage ranges.

**Quick Look**

To quickly evaluate the MAX1112/MAX1113's analog performance, use the circuit of Figure 5. The MAX1112/MAX1113 require a control byte to be written to DIN before each conversion. Tying DIN to +5V feeds

### Table 3. Control-Byte Format

<table>
<thead>
<tr>
<th>BIT 7 (MSB)</th>
<th>BIT 6</th>
<th>BIT 5</th>
<th>BIT 4</th>
<th>BIT 3</th>
<th>BIT 2</th>
<th>BIT 1</th>
<th>BIT 0 (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>START</td>
<td>SEL2</td>
<td>SEL1</td>
<td>SEL0</td>
<td>UNIBIP</td>
<td>SGLDIF</td>
<td>PD1</td>
<td>PD0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>BIT</th>
<th>NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (MSB)</td>
<td>START</td>
<td>The first logic &quot;1&quot; bit after CS goes low defines the beginning of the control byte.</td>
</tr>
<tr>
<td>6</td>
<td>SEL2</td>
<td>Select which of the input channels are to be used for the conversion (Tables 1 and 2).</td>
</tr>
<tr>
<td>5</td>
<td>SEL1</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>SEL0</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>UNIBIP</td>
<td>1 = unipolar, 0 = bipolar. Selects unipolar or bipolar conversion mode (Table 4).</td>
</tr>
<tr>
<td>2</td>
<td>SGLDIF</td>
<td>1 = single ended, 0 = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referenced to COM. In differential mode, the voltage difference between two channels is measured. See Tables 1 and 2.</td>
</tr>
<tr>
<td>1</td>
<td>PD1</td>
<td>1 = fully operational, 0 = power-down. Selects fully operational or power-down mode.</td>
</tr>
<tr>
<td>0 (LSB)</td>
<td>PD0</td>
<td>1 = external clock mode, 0 = internal clock mode. Selects external or internal clock mode.</td>
</tr>
</tbody>
</table>
**+5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs**

Table 4. Full-Scale and Zero-Scale Voltages

<table>
<thead>
<tr>
<th>UNIPOLAR MODE</th>
<th>BIPOLAR MODE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Positive</td>
</tr>
<tr>
<td>Full Scale</td>
<td>Full Scale</td>
</tr>
<tr>
<td>Zero Scale</td>
<td>0</td>
</tr>
<tr>
<td>VREFIN + COM</td>
<td>+VREFIN/2</td>
</tr>
<tr>
<td>COM</td>
<td>+ COM</td>
</tr>
</tbody>
</table>

In control bytes of SFF (hex), which trigger single-ended, unipolar conversions on CH7 (MAX1112) or CH3 (MAX1113) in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for two clock periods before the most significant bit (MSB) of the 8-bit conversion result is shifted out of DOUT. Varying the analog input alters the output code. A total of 10 clock cycles is required per conversion. All transitions of the SSTRB and DOUT outputs occur on SCLK’s falling edge.

**How to Start a Conversion**

A conversion is started by clocking a control byte into DIN. With CS low, each rising edge on SCLK clocks a bit from DIN into the MAX1112/MAX1113's internal shift register. After CS falls, the first arriving logic “1” bit at DIN defines the MSB of the control byte. Until this first start bit arrives, any number of logic “0” bits can be clocked into DIN with no effect. Table 3 shows the control-byte format. The MAX1112/MAX1113 are compatible with MICROWIRE, SPI, and QSPI devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. MICROWIRE, SPI, and QSPI all transmit a byte and receive a byte at the same time. Using the Typical Operating Circuit (Figure 3), the simplest software interface requires three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the...
8-bit conversion result). Figure 6 shows the MAX1112/ MAX1113 common serial-interface connections.

**Simple Software Interface**

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 50kHz to 500kHz.

1) Set up the control byte for external clock mode and call it TB1. TB1 should be of the format 1XXXX11 binary, where the Xs denote the particular channel and conversion mode selected.

2) Use a general-purpose I/O line on the CPU to pull CS low.

3) Transmit TB1 and, simultaneously, receive a byte and call it RB1. Ignore RB1.

4) Transmit a byte of all zeros ($00$ hex) and, simultaneously, receive byte RB2.

5) Transmit a byte of all zeros ($00$ hex) and, simultaneously, receive byte RB3.

6) Pull CS high.

Figure 7 shows the timing for this sequence. Bytes RB2 and RB3 contain the result of the conversion padded with two leading zeros and six trailing zeros. The total conversion time is a function of the serial-clock frequency and the amount of idle time between 8-bit transfers. Make sure that the total conversion time does not exceed 1ms, to avoid excessive I/H droop.
+5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

**Digital Output**
In unipolar input mode, the output is straight binary (Figure 15). For bipolar inputs, the output is two’s-complement (Figure 16). Data is clocked out at SCLK’s falling edge in MSB-first format.

**Clock Modes**
The MAX1112/MAX1113 can use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the devices. Bit PDO of the control byte programs the clock mode. Figures 8-11 show the timing characteristics common to both modes.

**External Clock**
In external clock mode, the external clock not only shifts data in and out, it also drives the analog-to-digital conversion steps. SSTRB pulses high for two clock periods after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next eight SCLK falling edges (Figure 7). After the eight data bits are clocked out, subsequent clock pulses clock out zeros from the DOUT pin.

SSTRB and DOUT go into a high-impedance state when CS goes high; after the next CS falling edge, SSTRB outputs a logic low. Figure 9 shows the SSTRB timing in external clock mode.

The conversion must complete in 1ms, or droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the serial-clock frequency is less than 50kHz, or if serial-clock interruptions could cause the conversion interval to exceed 1ms.
Internal clock mode frees the µP from the burden of running the SAR conversion clock. This allows the conversion results to be read back at the processor's convenience, at any clock rate up to 2MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB is low for 25µs (typically), during which time SCLK should remain low for best noise performance.

An internal register stores data when the conversion is in progress. SCLK clocks the data out of this register at any time after the conversion is complete. After SSTRB goes high, the second falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figure 10). CS does not need to be held low once a conversion is started. Pulling CS high prevents data from being clocked into the MAX1112/MAX1113 and three-states DOUT, but it does not adversely affect an internal clock-mode conversion already in progress. When internal clock mode is selected, SSTRB does not go into a high-impedance state when CS goes high.

Figure 11 shows the SSTRB timing in internal clock mode. In this mode, data can be shifted in and out of the MAX1112/MAX1113 at clock rates up to 2MHz, provided that the minimum acquisition time, tACQ, is kept above 1µs.
Data Framing

The falling edge of CS does not start a conversion. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on the falling edge of SCLK, after the eighth bit of the control byte (the PDO bit) is clocked into DIN. The start bit is defined as:

The first high bit clocked into DIN with CS low any time the converter is idle, e.g., after VDD is applied.

OR

The first high bit clocked into DIN after the MSB of a conversion in progress is clocked onto the DOUT pin.

If CS is toggled before the current conversion is complete, then the next high bit clocked into DIN is recognized as a start bit; the current conversion is terminated, and a new one is started.

The fastest the MAX1112/MAX1113 can run is 10 clocks per conversion. Figure 12a shows the serial-interface timing necessary to perform a conversion every 10 SCLK cycles in external clock mode.

Many microcontrollers require that conversions occur in multiples of eight SCLK clocks; 16 clocks per conversion is typically the fastest that a microcontroller can drive the MAX1112/MAX1113. Figure 12b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.
+5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

Applications Information

Power-On Reset
When power is first applied, and if SHDN is not pulled low, internal power-on reset circuitry activates the MAX1112/MAX1113 in internal clock mode. SSTRB is high on power-up and, if CS is low, the first logical 1 on DIN is interpreted as a start bit. Until a conversion takes place, DOUT shifts out zeros. No conversions should be performed until the reference voltage has stabilized (see the Wakeup Time specifications in the Timing Characteristics).

Power-Down
When operating at speeds below the maximum sampling rate, the MAX1112/MAX1113's automatic power-down mode can save considerable power by placing the converters in a low-current shutdown state between conversions. Figure 13 shows the average supply current as a function of the sampling rate.

Select power-down with PD1 of the DIN control byte with SHDN high or floating (Table 3). Pull SHDN low at any time to shut down the converters completely. SHDN overrides PD1 of the control byte. Figures 14a and 14b illustrate the various power-down sequences in both external and internal clock modes.

Software Power-Down
Software power-down is activated using bit PD1 of the control byte. When software power-down is asserted, the ADCs continue to operate in the last specified clock mode until the conversion is complete. The ADCs then power down into a low quiescent-current state. In internal clock mode, the interface remains active, and conversion results may be clocked out after the MAX1112/MAX1113 have entered a software power-down.

The first logical 1 on DIN is interpreted as a start bit, which powers up the MAX1112/MAX1113. If the DIN byte contains PD1 = 1, then the chip remains powered up. If PD1 = 0, power-down resumes after one conversion.

Table 5. Hard-Wired Power-Down and Internal Reference State

<table>
<thead>
<tr>
<th>SHDN STATE</th>
<th>DEVICE MODE</th>
<th>INTERNAL REFERENCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Enabled</td>
<td>Disabled</td>
</tr>
<tr>
<td>Floating</td>
<td>Enabled</td>
<td>Enabled</td>
</tr>
<tr>
<td>0</td>
<td>Power-Down</td>
<td>Disabled</td>
</tr>
</tbody>
</table>

Hard-Wired Power-Down
Pulling SHDN low places the converters in hard-wired power-down. Unlike software power-down, the conversion is not completed; it stops coincidentally with SHDN being brought low. SHDN also controls the state of the internal reference (Table 5). Letting SHDN float enables the internal 4.096V voltage reference. When returning to normal operation with SHDN floating, there is a typical delay of approximately 1μs x CLOAD, where CLOAD is the capacitive loading on the SHDN pin. Pulling SHDN high disables the internal reference, which saves power when using an external reference.

External Reference
An external reference between 1V and VDD should be connected directly at the REFIN terminal. The DC input impedance at REFIN is extremely high, consisting of leakage current only (typically 10nA). During a conversion, the reference must be able to deliver up to 20μA average load current and have an output impedance of 1kΩ or less at the conversion clock frequency. If the reference has higher output impedance or is noisy, bypass it close to the REFIN pin with a 0.1μF capacitor.

Figure 13. Average Supply Current vs. Sampling Rate

If an external reference is used with the MAX1112/MAX1113, tie SHDN to VDD to disable the internal reference and decrease power consumption.
+5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

Figure 14a. Power-Down Modes, External Clock Timing Diagram

Figure 14b. Power-Down Modes, Internal Clock Timing Diagram

**Internal Reference**

To use the MAX1112/MAX1113 with the internal reference, connect REFIN to REFOUT. The full-scale range of the MAX1112/MAX1113 with the internal reference is typically 4.096V with unipolar inputs, and ±2.048V with bipolar inputs. The internal reference should be bypassed to AGND with a 1μF capacitor placed as close to the REFIN pin as possible.

**Transfer Function**

Table 4 shows the full-scale voltage ranges for unipolar and bipolar modes. Figure 15 depicts the nominal, unipolar I/O transfer function, and Figure 16 shows the bipolar I/O transfer function when using a 4.096V reference. Code transitions occur at integer LSB values. Output coding is binary, with 1LSB = 16mV (4.096V/256) for unipolar operation and 1LSB = 16mV ((4.096V/2 ± 4.096V/2)/256) for bipolar operation.
+5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

Figure 15. Unipolar Transfer Function

Figure 16. Bipolar Transfer Function

Figure 17. Power-Supply Grounding Connections

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 17 shows the recommended system ground connections. A single-point analog ground (star ground point) should be established at AGND, separate from the logic ground. Connect all other analog grounds and DGND to the star ground. No other digital system ground should be connected to this ground. The ground return to the power supply for the star ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the VDD power supply may affect the comparator in the ADC. Bypass the supply to the star ground with 0.1μF and 1μF capacitors close to the VDD pin of the MAX1112/MAX1113. Minimize capacitor lead lengths for best supply-noise rejection. If the +5V power supply is very noisy, a 100Ω resistor can be connected to form a lowpass filter.
+5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

**Pin Configurations**

**Ordering Information (continued)**

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP. RANGE</th>
<th>PIN-PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX1112EPP</td>
<td>-40°C to +85°C</td>
<td>20 Plastic DIP</td>
</tr>
<tr>
<td>MAX1112EAP</td>
<td>-40°C to +85°C</td>
<td>20 SSOP</td>
</tr>
<tr>
<td>MAX1112VJP</td>
<td>-55°C to +125°C</td>
<td>20 CERDIP**</td>
</tr>
<tr>
<td>MAX1113CPE</td>
<td>0°C to +70°C</td>
<td>16 Plastic DIP</td>
</tr>
<tr>
<td>MAX1113CEE</td>
<td>0°C to +70°C</td>
<td>16 QSOP*</td>
</tr>
<tr>
<td>MAX1113EPE</td>
<td>-40°C to +85°C</td>
<td>16 Plastic DIP</td>
</tr>
<tr>
<td>MAX1113EEE</td>
<td>-40°C to +85°C</td>
<td>16 QSOP*</td>
</tr>
<tr>
<td>MAX1113MJE</td>
<td>-55°C to +125°C</td>
<td>16 CERDIP**</td>
</tr>
</tbody>
</table>

**Chip Information**

TRANSISTOR COUNT: 1996
SUBSTRATE CONNECTED TO DGND

**Contact factory for availability.**
Features

- Compatible with MCS-51™ Products
- 4 Kbytes of In-System Reprogrammable Flash Memory
- Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

Description

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4 Kbytes of Flash Programmable and Erasable Read Only Memory (PEROM). The device is manufactured using Atmel’s high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

Pin Configurations
Block Diagram

Vcc

GND

P0.0 - P0.7
PORT 0 DRIVERS

P2.0 - P2.7
PORT 2 DRIVERS

RAM ADDR
REGISTER

RAM

PORT 0
LATCH

PORT 2
LATCH

FLASH

B
REGISTER

ACC

TMP2

TMP1

ALU

STACK
POINTER

PROGRAM
ADDRESS
REGISTER

BUFFER

PC
INCREMENTER

PROGRAM
COUNTER

DPTR

TIMING
AND
CONTROL

INSTRUCTION
REGISTER

TIMING
AND
CONTROL

INSTRUCTION
REGISTER

PORT 1
LATCH

PORT 1
LATCH

PORT 1
DRIVERS

PORT 3
DRIVERS

P1.0 - P1.7

P3.0 - P3.7

PC

RST

ALE/PROG

EA / VPP

AT89C51
The AT89C51 provides the following standard features: 4 bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

## Pin Description

<table>
<thead>
<tr>
<th>Port Pin</th>
<th>Alternate Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>P3.0</td>
<td>RXD (serial input port)</td>
</tr>
<tr>
<td>P3.1</td>
<td>TXD (serial output port)</td>
</tr>
<tr>
<td>P3.2</td>
<td>INT0 (external interrupt 0)</td>
</tr>
<tr>
<td>P3.3</td>
<td>INT1 (external interrupt 1)</td>
</tr>
<tr>
<td>P3.4</td>
<td>T0 (timer 0 external input)</td>
</tr>
<tr>
<td>P3.5</td>
<td>T1 (timer 1 external input)</td>
</tr>
<tr>
<td>P3.6</td>
<td>WR (external data memory write strobe)</td>
</tr>
<tr>
<td>P3.7</td>
<td>RD (external data memory read strobe)</td>
</tr>
</tbody>
</table>

Port 3 also receives some control signals for Flash programming and verification.

### RST
Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

### ALE/PROG
Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

### PSEN
Program Store Enable is the read strobe to external program memory.

(continued)
When the AT89C51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

- **EA/VPP**
  - External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset.
  - EA should be strapped to Vcc for internal program executions.

This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming, for parts that require 12-volt VPP.

- **XTAL1**
  - Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

- **XTAL2**
  - Output from the inverting oscillator amplifier.

### Oscillator Characteristics

- XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal locking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

### Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware reset is enabled by strapping VPP to Vcc.

### Status of External Pins During Idle and Power Down

<table>
<thead>
<tr>
<th>Mode</th>
<th>Program Memory</th>
<th>ALE</th>
<th>PSEN</th>
<th>PORT0</th>
<th>PORT1</th>
<th>PORT2</th>
<th>PORT3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Idle</td>
<td>Internal</td>
<td>1</td>
<td>1</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
<tr>
<td>Idle</td>
<td>External</td>
<td>1</td>
<td>1</td>
<td>Float</td>
<td>Data</td>
<td>Address</td>
<td>Data</td>
</tr>
<tr>
<td>Power Down</td>
<td>Internal</td>
<td>0</td>
<td>0</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
<tr>
<td>Power Down</td>
<td>External</td>
<td>0</td>
<td>0</td>
<td>Float</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
</tbody>
</table>
ware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Power Down Mode

In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before Vcc is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below.

When lock bit 1 is programmed, the logic level at the EA pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of EA be in agreement with the current logic level at that pin in order for the device to function properly.

Lock Bit Protection Modes

<table>
<thead>
<tr>
<th>Program Lock Bits</th>
<th>Protection Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>LB1 LB2 LB3</td>
<td></td>
</tr>
<tr>
<td>1 U U U</td>
<td>No program lock features.</td>
</tr>
<tr>
<td>2 P U U</td>
<td>MOV C instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the Flash is disabled.</td>
</tr>
<tr>
<td>3 P P U</td>
<td>Same as mode 2, also verify is disabled.</td>
</tr>
<tr>
<td>4 P P P</td>
<td>Same as mode 3, also external execution is disabled.</td>
</tr>
</tbody>
</table>

Programming the Flash

The AT89C51 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage (Vcc) program enable signal. The low voltage programming mode provides a convenient way to program the AT89C51 inside the user's system, while the high-voltage programming mode is compatible with conventional third party Flash or EPROM programmers.

The AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

<table>
<thead>
<tr>
<th>Vpp = 12 V</th>
<th>Vpp = 5 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top-Side Mark</td>
<td>AT89C51</td>
</tr>
<tr>
<td>xxxx</td>
<td>xxxxx</td>
</tr>
<tr>
<td>ywww</td>
<td>yyyyy</td>
</tr>
<tr>
<td>Signature</td>
<td>(030H)=1EH</td>
</tr>
<tr>
<td></td>
<td>(031H)=51H</td>
</tr>
<tr>
<td></td>
<td>(032H)=FFH</td>
</tr>
</tbody>
</table>

The AT89C51 code memory array is programmed by-byte in either programming mode. To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.

Programming Algorithm: Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figures 3 and 4. To program the AT89C51, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise EA/Vpp to 12 V for the high-voltage programming mode.
5. Pulse ALE/PROG once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89C51 features Data Polling to indicate the end of a write cycle. During a write cycle, an at-
Programming the Flash (Continued)

A tempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/BSY output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/PROG low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

- (030H) = 1EH indicates manufactured by Atmel
- (031H) = 51H indicates 89C51
- (032H) = FFH indicates 12 V programming
- (032H) = 05H indicates 5 V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

<table>
<thead>
<tr>
<th>Flash Programming Modes</th>
<th>RST</th>
<th>PSEN</th>
<th>ALE/PROG</th>
<th>EA/VPP</th>
<th>P2.6</th>
<th>P2.7</th>
<th>P3.6</th>
<th>P3.7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write Code Data</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V(1)</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>Read Code Data</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>Write Lock Bit - 1</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>Write Lock Bit - 2</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>Write Lock Bit - 3</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>Chip Erase</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>Read Signature Byte</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
</tbody>
</table>

Notes: 1. The signature byte at location 032H designates whether Vpp = 12 V or Vpp = 5 V should be used to enable programming.
2. Chip Erase requires a 10 ms PROG pulse.

AT89C51
Flash Programming and Verification Characteristics

\[ T_A = 21^\circ C \text{ to } 27^\circ C, \quad V_{CC} = 5.0 \pm 10\% \]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{PP} )</td>
<td>Programming Enable Voltage</td>
<td>11.5</td>
<td>12.5</td>
<td>V</td>
</tr>
<tr>
<td>( I_{PP} )</td>
<td>Programming Enable Current</td>
<td>1.0</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( t/CLCL )</td>
<td>Oscillator Frequency</td>
<td>4</td>
<td>24</td>
<td>MHz</td>
</tr>
<tr>
<td>( t_{AVGL} )</td>
<td>Address Setup to PROG Low</td>
<td>48t_{CLCL}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{GHAX} )</td>
<td>Address Hold After PROG</td>
<td>48t_{CLCL}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{DVGL} )</td>
<td>Data Setup to PROG Low</td>
<td>48t_{CLCL}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{GHDX} )</td>
<td>Data Hold After PROG</td>
<td>48t_{CLCL}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{EHSH} )</td>
<td>P2.7 (ENABLE) High to Vpp</td>
<td>48t_{CLCL}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{SHGL} )</td>
<td>Vpp Setup to PROG Low</td>
<td>10</td>
<td>( \mu s )</td>
<td></td>
</tr>
<tr>
<td>( t_{GHSL} )</td>
<td>Vpp Hold After PROG</td>
<td>10</td>
<td>( \mu s )</td>
<td></td>
</tr>
<tr>
<td>( t_{GLGH} )</td>
<td>PROG Width</td>
<td>1</td>
<td>110</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( t_{AVQV} )</td>
<td>Address to Data Valid</td>
<td>48t_{CLCL}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{ELQV} )</td>
<td>ENABLE Low to Data Valid</td>
<td>48t_{CLCL}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{EHQV} )</td>
<td>Data Float After ENABLE</td>
<td>0</td>
<td>48t_{CLCL}</td>
<td></td>
</tr>
<tr>
<td>( t_{GHBL} )</td>
<td>PROG High to BUSY Low</td>
<td>1.0</td>
<td>( \mu s )</td>
<td></td>
</tr>
<tr>
<td>( t_{WC} )</td>
<td>Byte Write Cycle Time</td>
<td>2.0</td>
<td>ms</td>
<td></td>
</tr>
</tbody>
</table>

Note: 1. Only used in 12-volt programming mode.
Absolute Maximum Ratings*

- Operating Temperature: -55°C to +125°C
- Storage Temperature: -65°C to +150°C
- Voltage on Any Pin with Respect to Ground: -1.0 V to +7.0 V
- Maximum Operating Voltage: 6.6 V
- DC Output Current: 15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

\[ V_T = -40°C \text{ to } 85°C, \ V_{CC} = 5.0 \ V \pm 20\% \] (unless otherwise noted)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL</td>
<td>Input Low Voltage (Except EA)</td>
<td>-0.5</td>
<td>0.2 \ V_{CC} - 0.1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VIH</td>
<td>Input High Voltage (Except XTAL1, RST)</td>
<td>0.2 \ V_{CC} + 0.9</td>
<td>\ V_{CC} + 0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>Output Low Voltage (Ports 1, 2, 3)</td>
<td>\ I_{OL} = 1.6 \ mA</td>
<td>0.45</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOLT</td>
<td>Output Low Voltage (Ports 0, ALE, PSEN)</td>
<td>\ I_{OL} = 3.2 \ mA</td>
<td>0.45</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>Output High Voltage (Ports 1, 2, 3, ALE, PSEN)</td>
<td>\ I_{OH} = -60 \ \mu A, \ V_{CC} = 5 \ V \pm 10%</td>
<td>2.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOH1</td>
<td>Output High Voltage (Port 0 in External Bus Mode)</td>
<td>\ I_{OH} = -800 \ \mu A, V_{CC} = 5 \ V \pm 10%</td>
<td>2.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IIL</td>
<td>Logical 0 Input Current (Ports 1, 2, 3)</td>
<td>\ V_{IN} = 0.45 \ V</td>
<td>-50</td>
<td>\mu A</td>
<td></td>
</tr>
<tr>
<td>ITL</td>
<td>Logical 1 to 0 Transition Current (Ports 1, 2, 3)</td>
<td>\ V_{IN} = 2 \ V</td>
<td>-650</td>
<td>\mu A</td>
<td></td>
</tr>
<tr>
<td>IU</td>
<td>Input Leakage Current (Ports 0, EA)</td>
<td>0.45 &lt; \ V_{IN} &lt; \ V_{CC}</td>
<td>±10</td>
<td>\mu A</td>
<td></td>
</tr>
<tr>
<td>RRST</td>
<td>Reset Pulldown Resistor</td>
<td>50</td>
<td>300</td>
<td>\Omega</td>
<td></td>
</tr>
<tr>
<td>CIO</td>
<td>Pin Capacitance</td>
<td>Test Freq. = 1 MHz, \ T_A = 25°C</td>
<td>10</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>Power Supply Current</td>
<td>Active Mode, 12 MHz</td>
<td>20</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Idle Mode, 12 MHz</td>
<td>5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Power Down Mode (2)</td>
<td>V_{CC} = 6 \ V</td>
<td>100</td>
<td>\mu A</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 3 \ V</td>
<td>40</td>
<td>\mu A</td>
<td></td>
</tr>
</tbody>
</table>

Notes: 1. Under steady state (non-transient) conditions, \ I_{OL} must be externally limited as follows:
- Maximum \ I_{OL} per port pin: 10 mA
- Maximum \ I_{OL} per 8-bit port: Port 0: 26 mA
- Ports 1, 2, 3: 15 mA

2. Minimum \ V_{CC} for Power Down is 2 V.
**A.C. Characteristics**

(Under Operating Conditions; Load Capacitance for Port 0, ALE/PROG, and PSEN = 100 pF; Load Capacitance for all other outputs = 80 pF)

---

**External Program and Data Memory Characteristics**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>12 MHz Oscillator</th>
<th>16 to 24 MHz Oscillator</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/tCLCL</td>
<td>Oscillator Frequency</td>
<td>Min</td>
<td>Max</td>
<td>MHz</td>
</tr>
<tr>
<td>tLHLL</td>
<td>ALE Pulse Width</td>
<td>127</td>
<td>24</td>
<td>ns</td>
</tr>
<tr>
<td>tAVLL</td>
<td>Address Valid to ALE Low</td>
<td>28</td>
<td>tCLCL-13</td>
<td>ns</td>
</tr>
<tr>
<td>tLLAX</td>
<td>Address Hold After ALE Low</td>
<td>48</td>
<td>tCLCL-20</td>
<td>ns</td>
</tr>
<tr>
<td>tLLUIV</td>
<td>ALE Low to Valid Instruction In</td>
<td>233</td>
<td>3tCLCL-65</td>
<td>ns</td>
</tr>
<tr>
<td>tLLPL</td>
<td>ALE Low to PSEN Low</td>
<td>43</td>
<td>tCLCL-13</td>
<td>ns</td>
</tr>
<tr>
<td>tPLPH</td>
<td>PSEN Pulse Width</td>
<td>205</td>
<td>3tCLCL-20</td>
<td>ns</td>
</tr>
<tr>
<td>tLUV</td>
<td>PSEN Low to Valid Instruction In</td>
<td>145</td>
<td>3tCLCL-45</td>
<td>ns</td>
</tr>
<tr>
<td>tPXIX</td>
<td>Input Instruction Hold After PSEN</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>tPXIZ</td>
<td>Input Instruction Float After PSEN</td>
<td>59</td>
<td>tCLCL-10</td>
<td>ns</td>
</tr>
<tr>
<td>tPXAV</td>
<td>PSEN to Address Valid</td>
<td>75</td>
<td>tCLCL-8</td>
<td>ns</td>
</tr>
<tr>
<td>tAVIV</td>
<td>Address to Valid Instruction In</td>
<td>312</td>
<td>5tCLCL-55</td>
<td>ns</td>
</tr>
<tr>
<td>tPLAZ</td>
<td>PSEN Low to Address Float</td>
<td>10</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>tRLRH</td>
<td>RD Pulse Width</td>
<td>400</td>
<td>6tCLCL-100</td>
<td>ns</td>
</tr>
<tr>
<td>tWLWH</td>
<td>WR Pulse Width</td>
<td>400</td>
<td>6tCLCL-100</td>
<td>ns</td>
</tr>
<tr>
<td>tRLDV</td>
<td>RD Low to Valid Data In</td>
<td>252</td>
<td>5tCLCL-90</td>
<td>ns</td>
</tr>
<tr>
<td>tRHDX</td>
<td>Data Hold After RD</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>tRHDZ</td>
<td>Data Float After RD</td>
<td>97</td>
<td>2tCLCL-28</td>
<td>ns</td>
</tr>
<tr>
<td>tLLDV</td>
<td>ALE Low to Valid Data In</td>
<td>517</td>
<td>8tCLCL-150</td>
<td>ns</td>
</tr>
<tr>
<td>tAVDV</td>
<td>Address to Valid Data In</td>
<td>585</td>
<td>9tCLCL-165</td>
<td>ns</td>
</tr>
<tr>
<td>tLLWL</td>
<td>ALE Low to RD or WR Low</td>
<td>200</td>
<td>3tCLCL-50</td>
<td>ns</td>
</tr>
<tr>
<td>tAVWL</td>
<td>Address to RD or WR Low</td>
<td>203</td>
<td>4tCLCL-75</td>
<td>ns</td>
</tr>
<tr>
<td>tGWMX</td>
<td>Data Valid to WR Transition</td>
<td>23</td>
<td>tCLCL-20</td>
<td>ns</td>
</tr>
<tr>
<td>tGWMH</td>
<td>Data Valid to WR High</td>
<td>433</td>
<td>7tCLCL-120</td>
<td>ns</td>
</tr>
<tr>
<td>tWHOX</td>
<td>Data Hold After WR</td>
<td>33</td>
<td>tCLCL-20</td>
<td>ns</td>
</tr>
<tr>
<td>tRLAZ</td>
<td>RD Low to Address Float</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>tWHLH</td>
<td>RD or WR High to ALE High</td>
<td>43</td>
<td>tCLCL-20</td>
<td>ns</td>
</tr>
</tbody>
</table>

---

*AT89C51*
External Program Memory Read Cycle

External Data Memory Read Cycle
External Data Memory Cycle

External Clock Drive Waveforms

External Clock Drive

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/τCLCL</td>
<td>Oscillator Frequency</td>
<td>0</td>
<td>24</td>
<td>MHz</td>
</tr>
<tr>
<td>τCLCL</td>
<td>Clock Period</td>
<td>41.6</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>τCHCX</td>
<td>High Time</td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>τCLCX</td>
<td>Low Time</td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>τCLCH</td>
<td>Rise Time</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>τCHCL</td>
<td>Fall Time</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>
Serial Port Timing: Shift Register Mode Test Conditions

(\(V_{CC} = 5.0 \, V \pm 20\%; \text{ Load Capacitance} = 80 \, \text{pF}\))

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>12 MHz Osc</th>
<th>Variable Oscillator</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{XLXL})</td>
<td>Serial Port Clock Cycle Time</td>
<td>1.0</td>
<td>12tCLCL</td>
</tr>
<tr>
<td>(t_{QVXH})</td>
<td>Output Data Setup to Clock Rising Edge</td>
<td>700</td>
<td>10tCLCL-133</td>
</tr>
<tr>
<td>(t_{XHQX})</td>
<td>Output Data Hold After Clock Rising Edge</td>
<td>50</td>
<td>2tCLCL-33</td>
</tr>
<tr>
<td>(t_{XHDX})</td>
<td>Input Data Hold After Clock Rising Edge</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>(t_{XHDV})</td>
<td>Clock Rising Edge to Input Data Valid</td>
<td>700</td>
<td>10tCLCL-133</td>
</tr>
</tbody>
</table>

Shift Register Mode Timing Waveforms

AC Testing Input/Output Waveforms

\[V_{CC} - 0.5V\]
\[0.2 \, V_{CC} + 0.9V\]
\[0.2 \, V_{CC} - 0.1V\]

Note: 1. AC Inputs during testing are driven at \(V_{CC} - 0.5\, V\) for a logic 1 and \(0.45\, V\) for a logic 0. Timing measurements are made at \(V_{IH}\) min. for a logic 1 and \(V_{IL}\) max. for a logic 0.

Float Waveforms

Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded \(V_{OH}/V_{OL}\) level occurs.
BIODATA

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NIRM : 96.7.003.31073.54422

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Agama : Katolik
Alamat : Jl. Sawahan Templek IV/21, Sby

Riwayat Pendidikan:

➢ Tahun 1989 Lulus SDK Don Bosco Surabaya.
➢ Tahun 1995 Lulus SMAK St. Louis I Surabaya.

Selama kuliah, aktif sebagai:

➢ Anggota Senat Mahasiswa Fakultas Teknik.
➢ Anggota Unit Kegiatan Mahasiswa Bidang Kerohanian.
➢ Ketua dan anggota Paduan Suara Mahasiswa Cantate Domino.
➢ Asisten Praktikum Pengukuran Besaran Listrik di Laboratorium Pengukuran.
➢ Asisten Praktikum Sistem Instrumentasi Elektronika di Laboratorium Pengukuran.