LAMPIRAN
Program Alat_Uji_Respon_Filter;
(* Name/NRP : Jimmy Yang/513095064 *)
Abstrak : program ini digunakan untuk mengetahui respon filter, adapat
filter yang akan diuji adalah low pass, highpass, bandpass dan
notch filter. Dengan template dalam diagram bode akan memudahkan
kita untuk mengetahui respon dari filter tersebut, batas frekuensi
yang hendak diukur antara 20 Hz - 20 KHz. *)

uses crt, dos, graph;

type arr = array [0..200] of word;

const pa = $300;   (* alamat FFI port A yang dipakai *)
pow_ppi = $303;   (* elemen control word dari FFI *)
pow_pit = $307;   (* elemen control word dari PIT *)
pit = $144;      (* inisialisasi PIT *)
pit0 = $324;     (* PITO/Counter0 yang dipakai *)
adc = $328;      (* alamat pengaktifan ADC *)
dac = $32C;      (* alamat pengaktifan DAC *)
 sampel = $12;    (* jumlah pencolokan *)
 vpin = $4095;    (* besar tegangan input sebanyak 4095 data *)
fmax = $3493;    (* frekuensi maksimum dari sweep function generator *)
j = -5937.135783; lsb = 4.8832E-3;
Gray10 : FillPatternType = (2AA, 4AA, 4AA, 4AA, 4AA, 4AA, 4AA, 4AA);

var Gdmode, Gdmask, DataMax, DataMin : integer;
    input : array [0..4095] of integer;
    til : file of complex;
    Vppout, gein : arr;
    fout, yjl, jyl : word;
    p, n, x, y : word;
    filter, tombol : char;
    sampling : boolean;
    rev : pointer;
    plot : complex;
    leg : real;

procedure InisialisasiVariabel;
begin
    portw[dec] := $0488+round(teg/lsb);
    sampling := false;
    DataMax := $5000;
    DataMin := $5000;
    fout := 0;
    n := 0;
    p := 0;
    jyl := 0;
end;

procedure AreaLPF;
(* Untuk membuat area Lowpass untuk titik yang akan ditampilkan kelayar monitor *)
begin
    SetFillPattern(Gray10, black); (*rectangle*)
    Bar(55, 69, 579, 369); (*XY axis*)
    SetColor(yellow);
    line(50, 40, 50, 399); (*x, y*)
    line(50, 310, 600, 310); (*50 x*)
    SetColor(white);
    for y:=0 to 16 do line(52, 53+(y*16), 54, 53+(y*16)); (*grs kol sb: y*)
    for y:=0 to 26 do line(50+(y*20), 313, 50+(y*20), 300); (*grs kol sb x*)
    SetColor(darkgray);
    for x:=0 to 7 do line(55, 53+(x*32), 570, 53+(x*32)); (*hor line*)
    for x:=0 to 12 do line(90+(x*40), 55, 90+(x*40), 305); (*ver line*)
    SetColor(white);
    outtextxy(13, 29, 'Amplitudo');
    outtextxy(20, 50, '9');
    outtextxy(20, 82, '7');
    outtextxy(20, 114, '6');
    outtextxy(20, 146, '5');
    outtextxy(20, 178, '4');
procedure AreaHpf;  
(Untuk memainkat area Highpass untuk titik yang akan ditampilkan kamera monitor)
begin
  SetFillPattern(Gray18,black);  
  Bez(50,49,570,290);  
  setcolor(yellow);  
  line(50,40,50,309);  
  line(50,310,600,319);  
  setcolor(yellow);  
  for y:=0 to 15 do line(52,53+(y*16), 54,53+(y*16));  
  for y:=0 to 26 do line(50+(y*23),319, 50+(y*23),309);  
  setcolor(darkgray);  
  for x:=0 to 7 do line(55,53+(x*32), 570,53+(x*32));  
  for x:=0 to 12 do line(90+(x*40),55, 90+(x*40),309);  
  setcolor(white);  
  outtextxy(10,20, 'Amplitude');  
  outtextxy(20,50, '9');  
  outtextxy(20,33, '7');  
  outtextxy(20,114,' 6');  
  outtextxy(20,146, '5');  
  outtextxy(20,178, '4');  
  outtextxy(20,210, '3');  
  outtextxy(20,242, '2');  
  outtextxy(20,274, '1');  
  outtextxy(20,306, '0');  
  outtextxy(140,315, '1');  
  outtextxy(140,315, '2');  
  outtextxy(140,315, '3');  
  outtextxy(140,315, '4');  
  outtextxy(140,315, '5');  
  outtextxy(540,315, '6 kHz');  
  outtextxy(250,369,'HIGHPASS FILTER');  
end;

procedure AreaBpf;  
(Untuk memainkat area Bandpass untuk titik yang akan ditampilkan kamera monitor)
begin
  SetFillPattern(Gray19,black);  
  Bez(50,50,570,360);  
  setcolor(yellow);  
  line(50,40,50,309);  
  line(50,310,600,319);  
  setcolor(yellow);  
  for y:=0 to 15 do line(52,53+(y*16), 54,53+(y*16));  
  for y:=0 to 26 do line(50+(y*23),319, 50+(y*23),309);  
  setcolor(darkgray);  
  for x:=0 to 7 do line(55,53+(x*32), 570,53+(x*32));  
  for x:=0 to 12 do line(90+(x*40),55, 90+(x*40),309);  
  setcolor(white);  
  outtextxy(10,20, 'Amplitude');  
  outtextxy(20,50, '9');  
  outtextxy(20,33, '7');  
  outtextxy(20,114,' 6');  
  outtextxy(20,146, '5');  
  outtextxy(20,178, '4');  
  outtextxy(20,210, '3');
procedure AreaMatch:
    (* Untuk membuat area Match untuk titik yang akan ditampilkan kelayar monitor *)
    begin
        SetFillPattern(Gray10, black); (* rectangle *)
        Bar(50, 60, 570, 360);
        setcolor(yellow);
        Line(50, 60, 570, 360); (* sb y *)
        Line(50, 315, 600, 315); (* sb x *)
        setcolor(yellow);
        for y:=0 to 15 do line(52, 53+(y*.16), 54, 53+(y*.16)); {grs kl sl: y}
        for y:=0 to 26 do line(50+(y*.29), 310, 50+(y*.29), 330); {grs kl ss: x}
        setcolor(darkgray);
        for x:=0 to 7 do line(55, 53+(x*.32), 570, 53+(x*.32)); (* hor line *)
        for x:=0 to 12 do line(95+(x*.40), 55, 95+(x*.40), 335); (* ver line *)
        setcolor(white);
        outtextxy[10, 50, 'Amplitude' ];
        outtextxy[20, 50, ' ' ];
        outtextxy[20, 92, ' ' ];
        outtextxy[20, 114, ' ' ];
        outtextxy[20, 146, ' ' ];
        outtextxy[20, 178, ' ' ];
        outtextxy[20, 210, ' ' ];
        outtextxy[20, 242, ' ' ];
        outtextxy[20, 274, ' ' ];
        outtextxy[20, 306, ' ' ];
        outtextxy[60, 315, ' ' ];
        outtextxy[140, 315, ' ' ];
        outtextxy[220, 315, ' ' ];
        outtextxy[300, 315, ' ' ];
        outtextxy[380, 315, ' ' ];
        outtextxy[460, 315, ' ' ];
        outtextxy[540, 315, '8 MHz' ];
        outtextxy[250, 360, 'BANDPASS FILTER' ];
    end;

procedure InitializeGraph:
    (* Untuk mengaktifkan mode grafik pada bahasa pemrograman pascal dan mode resolusi yang digunakan yaitu 640x480 pixel *)
    begin
        grdriver:= detect;
        gmode := VGAHi;
        Initgraph(grDriver, grMode, 'd:\tp\bg1');
    end;

procedure Initialize_PIT:
    (* Untuk membagi input clock yang dimasukkan ke PIT dan menghasilkan clock dengan frekuensi yang dikenal. Alamat I/O untuk PIT 306H-30BH. Control Word = 14H *)
    begin
        port[pwm_pit]: = ox_pit; (* Mode 2 untuk Counter0 PIT 3253 *)
        port[pit0] := 55; (* pembagi clock *)
    end;
procedure Baca_adc; interrupt;
(Untuk mengkonversi data analog menjadi data digital dan alamat I/O yang digunakan
untuk ADC yaitu 508E. Interrupt yang digunakan yaitu IRQ5 yang menginterupsi setiap
$12 mikro sampel yang diambil)
begin
sampling:= false;
input[n]:= (-portw[adc] and $FF); (myiuang bit 12-15)
if not input[n] and $80=0 then input[n]:= -2048+(input[n] and $FF);
Inc[n];
if n=0 then begin
n:= 0;
sampling:= true;
port[$21]:= port[$21] or $20; (disable IRQ5 8259)
end;
port[$21]:= $20; (end of Interrupt)
if input[n]<datamin then datamin:= input[n];
end;

procedure Hpf;
begin
portw[pa]:= $01;
yl:= 200; (start harga frekuensi awal)
InitialisasiGraph;
Initialisasi_PTF;
Getintvec($0E, rev); (menyimpan alamat IRQ5 ke rev)
Setintvec($0D, Baca_adc); (set alamat IRQ5)
port[$21]:= port[$21] and $2F; (enable IRQ5)
AreaPlot;
yl:= 0;
repeat
if sampling=true then begin
Inc[yyl];
Vppout[yyl]:= datamax-datamin;
Gain[yyl]:=-round(200*ln(vppout[yyl]/vppin)/ln(10));
datamax:= -5000;
datamin:= +5000;
for:= yyl*yl; tef:= (1+max-out)/yl;
portw[adc]:= 2048+round(ter/12);
if Gain[yyl]<2.4 then
putpixel(45+yyl*3, 55+(Gain[yyl]), white);
port[$21]:= port[$21] and $2F; (enable IRQ5 8259)
end;
delay(5);
if keypressed then tombol:=readkey;
until (yl&ls0) or (tombol=$27);
tombol:= readkey;
Closegraph;
Setintvec($0D, rev);
end;
Listing Program

begin
  inc([jyl]);
  vppout([jyl]) := datamax - datamin;
  gain([jyl]) := -round(200*ln(vppout([jyl])/vppin)/ln(10));
  datamax := -5000;
  datamin := +5000;
  fout := jyl*jyl;
  teg := -((fmax-fout)/j);
  port[dac] := 2048+round(teg/128);
  if (gain([jyl])<2600 and (jyl<1) and (jyl<2) and (jyl<3) and (jyl<4)) then
    putpixel (45*jyl*5, $5+gain([jyl]), white);
    port[$21] := port[$21] and $DF; { enable IRQ5 $259}
end;

procedure Epf;
begin
  port[pal] := $03;
  jyl := 100;
  InisialisasiGraph;
  Inisialisasi_FIT;
  Getintvec($0E, rev);
  Setintvec($0E, $99, adc);
  port[$21] := port[$21] and $DF; { enable IRQ5 $259}
  AreaEpf;
  jyl := 0;
  repeat
    if sampling=true then
      begin
        inc([jyl]);
        vppout([jyl]) := datamax - datamin;
        gain([jyl]) := -round(200*ln(vppout([jyl])/vppin)/ln(10));
        datamax := -5000;
        datamin := +5000;
        fout := jyl*jyl;
        teg := -((fmax-fout)/j);
        port[dac] := 2048+round(teg/128);
        if gain([jyl])<230 then
          putpixel (45*jyl*5, $5+gain([jyl]), white);
          port[$21] := port[$21] and $DF; { enable IRQ5 $259}
      end;
      delay(5);
      if Keypressed then tombol:=readkey;
      until (jyl=175) or (tombol=$27);
      tombol:= readkey;
      Closegraph;
      Setintvec($0E, rev);
  end;

procedure Notch;
begin
  port[pal] := $04;
  jyl := 100;
  InisialisasiGraph;
  Inisialisasi_FIT;
  Getintvec($0E, rev);
  Setintvec($0E, $99, adc);
  port[$21] := port[$21] and $DF; { enable IRQ5 $259}
  AreaNotch;
  jyl := 0;
  repeat
    if sampling=true then
      begin
        inc([jyl]);
        (Ubah_frek);
        vppout([jyl]) := datamax - datamin;
        gain([jyl]) := -round(200*ln(vppout([jyl])/vppin)/ln(10));
        datamax := -5000;
        datamin := +5000;
        fout := jyl*jyl;
        teg := -((fmax-fout)/j);
        port[dac] := 2048+round(teg/128);
        if gain([jyl])<230 then
          putpixel (45*jyl*5, $5+gain([jyl]), white);
          port[$21] := port[$21] and $DF; { enable IRQ5 $259}
      end;
      delay(5);
      if Keypressed then tombol:=readkey;
      until (jyl=175) or (tombol=$27);
      tombol:= readkey;
      Closegraph;
      Setintvec($0E, rev);
  end;
datamin := +5000;
font := yyl*yyil;
teg := -1//fmax-font/j;
port[dac] := 2048+round(teg/lac);
if:gain[yyil]<300|and(yyil<1) end(yyil<2|end(yyil<3|end(yyil<4) then
putpixel (45+yyil*5),30+gain[yyil],white);
port[21]:= port[21] and $DF; (enable IAP5 $259)
end;
delay/5;
if keypressed then tombol:=readkey;
until (yyil=105) or (tombol=27);
tombol:= readkey;
closegraph;
Setintvec($9C,rev);
end;

procedure Menu;
begin
  textcolor(lighblue);
  writeln;
  writeln('

Filih Jenis Penuh Filter ');
  writeln;
  textcolor(14);
  writeln;
  write(' * Lowpass Filter, taken tombol!');
  textcolor(14+blink); writeln(':*');
  textcolor(14);
  write(' * Highpass Filter, taken tombol!');
  textcolor(14+blink); writeln(' H');
  textcolor(14);
  write(' * Bandpass Filter, taken tombol!');
  textcolor(14+blink); writeln(' B');
  textcolor(14);
  write(' * Notch Filter, taken tombol!');
  textcolor(14+blink); writeln(' N ');
  textcolor(14);
  gotoxy (4,12); writeln(' Pilihan anda :');
  gotoxy (3,12); readin (filter);
  port[pow_ppl]:= cw_ppl;
case upcase [filter] of
  'I': Lpf; 'H': Hpf; 'B': Bpf; 'N': Notch;
end;
end;

begin
  clrscr;
  Inisialisasi Variabel;
  Menu;
end.
Data Book

~I~INI

500ksps, 12-Bit ADCs

with Track/Hold and Reference

General Description

The MAX120 and MAX122 complete, BICMOS, sampling 12-bit analog-to-digital converters (ADCs) combine an on-chip track/hold (T/H) and a low-drift voltage reference with fast conversion speeds and low power consumption. The 12-bit 350ns acquisition time combined with the MAX120's 1.6μs conversion time results in throughput rates as high as 500ksps. Throughput rates of 333ksps are possible with the 2.6μs conversion time of the MAX122.

The MAX120/MAX122 accept analog input voltages from -5V to +5V. The only external components needed are decoupling capacitors for the power-supply and reference voltages. The MAX120 operates with clocks in the 0.1MHz to 8MHz frequency range. The MAX122 accepts 0.1MHz to 5MHz clock frequencies.

The MAX120/MAX122 employ a standard microprocessor (μP) interface. Three-state data outputs are configured to operate with 12-bit data buses. Data-access and bus-release timing specifications are compatible with most popular μPs without resorting to wait states. In addition, the MAX120/MAX122 can interface directly to a first-in, first-out (FIFO) buffer, virtually eliminating μP interrupt overhead. All logic inputs and outputs are TTL/CMOS compatible. For applications requiring a serial interface, refer to the new MAX121.

Applications

Digital-Signal Processing
Audio and Telecom Processing
Speech Recognition and Synthesis
High-Speed Data Acquisition
Spectrum Analysis
Data Logging Systems

Features

♦ 12-Bit Resolution
♦ No Missing Codes Over Temperature
♦ 20ppm/°C -5V Internal Reference
♦ 1.6μs Conversion Time/500ksps Throughput (MAX120)
♦ 2.6μs Conversion Time/333ksps Throughput (MAX122)
♦ Low Noise and Distortion: 70 dB Min SINAD; -115 dB THD (MAX122)
♦ Low Power Dissipation: 210mW
♦ Separate Track/Hold Control Input
♦ Continuous-Conversion Mode Available
♦ ±5V Input Range, Overvoltage Tolerant to ±15V
♦ 24-Pin Narrow DIP, Wide SO and SSOP Packages

Ordering Information

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP. RANGE</th>
<th>PACKAGE</th>
<th>RE (LODs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX120CG</td>
<td>0°C to +70°C</td>
<td>24 Narrow Plastic DIP</td>
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<td>MAX120CWG</td>
<td>0°C to +70°C</td>
<td>24 Wide SO</td>
<td>+1</td>
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<tr>
<td>MAX120CAG</td>
<td>0°C to +70°C</td>
<td>24 SSOP</td>
<td>+1</td>
</tr>
<tr>
<td>MAX120CD</td>
<td>0°C to +70°C</td>
<td>Die*</td>
<td>+1</td>
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<td>MAX120ENG</td>
<td>-40°C to +85°C</td>
<td>24 Narrow Plastic DIP</td>
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<td>MAX120EGW</td>
<td>-40°C to +85°C</td>
<td>24 Wide SO</td>
<td>+1</td>
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</tbody>
</table>

Ordering Information continued on last page.

*Contact factory for die specifications

Functional Diagram

Call toll free 1-800-998-8800 for free samples or literature.
**500ksps, 12-Bit ADCs**

**with Track/Hold and Reference**

**ABSOLUTE MAXIMUM RATINGS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc to DGND</td>
<td></td>
<td></td>
<td>-0.3V to +6V</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Vss to DGND</td>
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<td></td>
<td>+0.3V to -1.7V</td>
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<td>AIN to AGND</td>
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<td></td>
<td>±1.5V</td>
<td></td>
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<tr>
<td>AGND to DGND</td>
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<td></td>
<td>±0.2V</td>
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<td></td>
<td>0.3V to (Vcc + 0.3V)</td>
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<tr>
<td>Continuous Power Dissipation (TA = +70°C)</td>
<td></td>
<td></td>
<td>1000mW</td>
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<td>106mW</td>
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<td>SO (derate 11.76mW/°C above +70°C)</td>
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<td>941mW</td>
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<tr>
<td>SSOP (derate 800mW/°C above +70°C)</td>
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<td>640mW</td>
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<tr>
<td>Narrow CERDIP (derate 12.50mW/°C above +70°C)</td>
<td></td>
<td></td>
<td>167mW</td>
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<tr>
<td>MAX12_C_</td>
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<td>Operating Temperature Ranges</td>
<td>-40°C to +85°C</td>
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<tr>
<td>MAX12_E_</td>
<td></td>
<td></td>
<td>-40°C to +85°C</td>
<td></td>
<td></td>
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<tr>
<td>MAX12_MRG</td>
<td></td>
<td></td>
<td>-40°C to +125°C</td>
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<tr>
<td>MAX12_CB</td>
<td></td>
<td>Storage Temperature Range</td>
<td>-40°C to +125°C</td>
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<td></td>
<td></td>
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</tbody>
</table>

**ELECTRICAL CHARACTERISTICS**

(Vcc = +4.75V to +5.25V, VSS = -0.6V to -15.75V, IR = 8mA for MAX120 and 5mA for MAX122, TA = TMIN to TMAX unless otherwise noted.)

**PARAMETER** | **SYMBOL** | **CONDITIONS** | **MIN** | **TYP** | **MAX** | **UNITS**
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</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>RES</td>
<td>MAX12AC/AE</td>
<td>12</td>
<td>13/4</td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>Differential Nonlinearity (Note 1)</td>
<td>DNL</td>
<td>MAX120C/EB</td>
<td>12</td>
<td></td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>Integral Nonlinearity (Note 1)</td>
<td>INL</td>
<td>MAX120C/EB</td>
<td>13</td>
<td></td>
<td></td>
<td>LSB</td>
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<tr>
<td>Bipolar Zero Error (Note 1)</td>
<td></td>
<td>MAX12AC/AE</td>
<td>±0.005</td>
<td></td>
<td></td>
<td>LSB/C</td>
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<tr>
<td>Full-Scale Error (Notes 1, 2)</td>
<td>FS</td>
<td>Including reference, adjusted for bipolar zero error, TA = +25°C</td>
<td>±1</td>
<td></td>
<td></td>
<td>ppm/V</td>
</tr>
<tr>
<td>Full-Scale Temperature Drift</td>
<td></td>
<td>Excluding reference</td>
<td>±1/4</td>
<td>±3/4</td>
<td></td>
<td>ppm/V/°C</td>
</tr>
<tr>
<td>Power-Supply Rejection Ratio (Change in FS, Note 3)</td>
<td>PSRR</td>
<td>Vcc only, 5V ±5%</td>
<td>±1/4</td>
<td>±1</td>
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<td>LSB</td>
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<td>Vss only, -12V ±10%</td>
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<td>±1</td>
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<td>Vss only, -15V ±5%</td>
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<td>±1/4</td>
<td>±1</td>
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<td>Full-Power Input Bandwidth</td>
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<td>Output Voltage</td>
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<td>External Load Regulation</td>
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<td>Temperature Drift (Note 5)</td>
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<th>Min</th>
<th>Typ</th>
<th>Max</th>
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<tr>
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<td>RES</td>
<td>MAX12C</td>
<td>12</td>
<td>13/4</td>
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<td>Bits</td>
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<td>Differential Nonlinearity (Note 1)</td>
<td>DNL</td>
<td>MAX120C/EB</td>
<td>12</td>
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<td>LSB</td>
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<td>MAX120C/EB</td>
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<td>Bipolar Zero Error (Note 1)</td>
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<td>MAX12AC/AE</td>
<td>±0.005</td>
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<td>LSB/C</td>
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<td>Full-Scale Error (Notes 1, 2)</td>
<td>FS</td>
<td>Including reference, adjusted for bipolar zero error, TA = +25°C</td>
<td>±1</td>
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<td>ppm/V</td>
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<td>Excluding reference</td>
<td>±1/4</td>
<td>±3/4</td>
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<td>ppm/V/°C</td>
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<td>Power-Supply Rejection Ratio (Change in FS, Note 3)</td>
<td>PSRR</td>
<td>Vcc only, 5V ±5%</td>
<td>±1/4</td>
<td>±1</td>
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<td>LSB</td>
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<tr>
<td>Vss only, -12V ±10%</td>
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<td>±1/4</td>
<td>±1</td>
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<tr>
<td>Vss only, -15V ±5%</td>
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<td>±1/4</td>
<td>±1</td>
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<td>ANALOG INPUT</td>
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<td>Inrush Capacitance (Note 4)</td>
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<td>Full-Power Input Bandwidth</td>
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<td>Temperature Drift (Note 5)</td>
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</table>
500ksps, 12-Bit ADCs with Track/Hold and Reference

**ELECTRICAL CHARACTERISTICS (continued)**

(VDD = +4.75V to +5.25V, VSS = -10.8V to -15.75V, fCLK = 8MHz for MAX120 and 5MHz for MAX122, TMIN to TMAX, unless otherwise noted.)

<table>
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<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
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<th>MAX</th>
<th>UNITS</th>
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<tr>
<td>Dynamic Performance</td>
<td>SINAD</td>
<td>MAX120, MAX122</td>
<td>70</td>
<td>72</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MAX120BC/BE/BM</td>
<td>69</td>
<td></td>
<td></td>
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<tr>
<td>Total Harmonic Distortion (first five harmonics)</td>
<td>THD</td>
<td>MAX120</td>
<td>0.82</td>
<td>0.77</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MAX122</td>
<td>0.85</td>
<td>0.78</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MAX122AC/AE</td>
<td>0.77</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MAX122BC/BE/BM</td>
<td>0.75</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Spurious-Free Dynamic Range</td>
<td>SFDR</td>
<td>MAX120</td>
<td>77</td>
<td>86</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MAX122</td>
<td>78</td>
<td>86</td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

**CONVERSION TIME**

| Synchronous Conversion Time | tCONV | MAX120 | 1.63 | | | us |
| | tCLK | MAX122 | 2.63 | | | |

**DIGITAL INPUTS (CLKIN, CONVST, RD, CS)**

| Input Voltage | VIL | 2.4 | V |
| Input Current | ISINK | 16mA | |
| Input Current | ISOURCE | 1mA | |

**DIGITAL OUTPUTS (INT/BUSY, D11-DO)**

| Output Voltage | VOD | 0.4 | V |
| Leakage Current | IOL | 0.5 | mA |
| Output Current | IOH | 10 | pA |

**POWER REQUIREMENTS**

| Positive Supply Voltage | VDD | Guaranteed by supply rejection test | 4.75 | 5.25 | | V |
| Negative Supply Voltage | VSS | Guaranteed by supply rejection test | -10.80 | -15.75 | | V |
| Positive Supply Current (Note 6) | IDD | VDD = 5.25V, VSS = -15.75V, AIN = 0V | 9 | 15 | | mA |
| Negative Supply Current (Note 6) | ISS | VDD = 5.25V, VSS = -15.75V, AIN = 0V | 14 | 20 | | mA |
| Power Dissipation (Note 6) | PDISSIP | VDD = 5V, VSS = -12V, AIN = 0V | 210 | 315 | | mW |

**Notes:**

1. These tests are performed at VDD = 5V, VSS = -15V. Operation over supply is guaranteed by supply rejection test.
2. Ideal full-scale transition is 8V - 3.3V, 8V - 4.996V adjusted for offset error.
3. Supply rejection defined as change in full-scale transition voltage with the specified change in supply voltage = (VFS at nominal supply ± tolerance) expressed in LSBs.
4. For design guidance only; not tested.
5. Temperature drift defined as the change in output voltage from +25°C to TMIN or TMAX. It is calculated as
   
   \[ TC = (VREF/VREF0) \times 107 \]

6. CS = RD = CONVST = 0V, MODE = 5V
500ksps, 12-Bit ADCs with Track/Hold and Reference

TIMING CHARACTERISTICS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>TA = +25°C</th>
<th>MAX12_CE</th>
<th>MAX12_M</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS to RD Setup Time</td>
<td>C5</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>CS to RD Hold Time</td>
<td>DTH</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>CDRVFST Pulse Width</td>
<td>CW</td>
<td>30</td>
<td>30</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>RD Pulse Width</td>
<td>RW</td>
<td>10A</td>
<td>10A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data-Access Time</td>
<td>DDA</td>
<td>C1 = 100pF</td>
<td>40 75</td>
<td>100</td>
<td>120 ns</td>
</tr>
<tr>
<td>Bus-Reinquish Time</td>
<td>DTH</td>
<td>30 50</td>
<td>65</td>
<td>81 ns</td>
<td></td>
</tr>
<tr>
<td>RD or CDRVFST to BUSY</td>
<td>C10</td>
<td>C1 = 50pF</td>
<td>30 75</td>
<td>100</td>
<td>120 ns</td>
</tr>
<tr>
<td>CLkin to BUSY or INT</td>
<td>C1</td>
<td>C1 = 50pF</td>
<td>70 110</td>
<td>150</td>
<td>180 ns</td>
</tr>
<tr>
<td>CLkin to BUSY Low</td>
<td>CA</td>
<td>In mode 5</td>
<td>45 95</td>
<td>120</td>
<td>150 ns</td>
</tr>
<tr>
<td>RD to RD High</td>
<td>C1</td>
<td>C1 = 50pF</td>
<td>30 50</td>
<td>75</td>
<td>91 ns</td>
</tr>
<tr>
<td>BUSY or INT to Data Valid</td>
<td>RAD</td>
<td>C1(Data) = 100pF</td>
<td>20</td>
<td>30</td>
<td>26 ns</td>
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<td>Acquisition Time (Note 8)</td>
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<td>350</td>
<td>350</td>
<td>400</td>
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<tr>
<td>Aperture Delay (Note 8)</td>
<td>IAP</td>
<td>10</td>
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<tr>
<td>Aperture Jitter (Note 8)</td>
<td>IAJ</td>
<td>30</td>
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</table>

Note 7: Control inputs specified with \( V_{CC} = +5V \), \( V_{SS} = -12V \) to \(-15V \). 100% tested, \( TA = -40°C \) to \(+85°C \) unless otherwise noted. \( \text{(Note 7)} \)

Note 8: For design guidance only, not tested.

### Pin Description

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>MODE</td>
<td>Mode Input - hard wire to set operational mode</td>
</tr>
<tr>
<td>2</td>
<td>VSS</td>
<td>Negative Power Supply -12V or -15V</td>
</tr>
<tr>
<td>3</td>
<td>VDD</td>
<td>Positive Power Supply +5V</td>
</tr>
<tr>
<td></td>
<td>AN</td>
<td>Sampling Analog Input ±5V bipolar input range</td>
</tr>
<tr>
<td>5</td>
<td>VREF</td>
<td>-5V Reference Output - bypass to AGND with 22μF and 0.1μF</td>
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</table>
500ksps, 12-Bit ADCs with Track/Hold and Reference

Pin Description (continued)

<table>
<thead>
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<th>NAME</th>
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<tr>
<td>6</td>
<td>AGND</td>
<td>Analog Ground</td>
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<tr>
<td>7-11</td>
<td>D11-D0</td>
<td>Three-State Data Outputs D11 (MSB) to D0 (LSB)</td>
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<tr>
<td>12</td>
<td>DGND</td>
<td>Digital Ground</td>
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<tr>
<td>20</td>
<td>CONVST</td>
<td>Convert Start Input initiates conversions on its falling edge</td>
</tr>
<tr>
<td>21</td>
<td>CI/KIN</td>
<td>Clock Input Drive with TTL-compatible clock from 0.1MHz to 8MHz (MAX120), 0.1MHz to 5MHz (MAX122)</td>
</tr>
<tr>
<td>22</td>
<td>NT/BUSY</td>
<td>Interrupt or Busy Output indicates converter status. If MODE is connected to VCC, configure for an INT output. If MODE is open or connected to DGND, configure for a BUSY output. See operational diagrams.</td>
</tr>
<tr>
<td>23</td>
<td>CS</td>
<td>Chip Select Input - active low. When RD is low, enables the three-state outputs. If CONVST and RD are low, a conversion is initiated on the falling edge of CS.</td>
</tr>
<tr>
<td>24</td>
<td>RD</td>
<td>Read Input - active low. When CS is low, RD enables the three-state outputs. If CONVST and CS are low, a conversion is initiated on the falling edge of RD.</td>
</tr>
</tbody>
</table>

Detailed Description

ADC Operation

The MAX120/MAX122 use successive approximation and input T/H circuitry to convert an analog signal to a series of 12-bit digital output codes. The control logic interfaces easily to most PICs, requiring only a few passive components for most applications. The T/H does not require an external capacitor. Figure 3 shows the MAX120/MAX122 in the simplest operational configuration.

Analog Input Track/Hold

Figure 4 shows the equivalent input circuit, illustrating the sampling architecture of the ADC's analog comparator. An internal buffer charges the hold capacitor to minimize the required acquisition time between conversions. The analog input appears as a 6kΩ resistor in parallel with a 10pF capacitor.

Between conversions, the buffer input is connected to AGND through the input resistance. When a conversion starts, the buffer input disconnects from AGND, thus sampling the input. At the end of the conversion, the buffer input reconnects to AGND, and the hold capacitor once again charges to the input voltage.

The T/H is in tracking mode whenever a conversion is NOT in progress. Hold mode starts approximately 10ns after a conversion is initiated. Variation in this delay from one conversion to the next (aperture jitter) is typically 30ps. Figures 7 through 11 detail the T/H mode and interface timing for the various interface modes.
500ksps, 12-Bit ADCs with Track/Hold and Reference

**Internal Reference**

The MAX120/MAX122 -5.0V Zener reference biases the internal DAC. The reference output is available at the VREF pin and must be bypassed to the AGND pin with a 0.1µF ceramic capacitor in parallel with a 22µF or greater electrolytic capacitor. The electrolytic capacitor's equivalent series resistance (ESR) must be 100mΩ or less to properly compensate the reference output buffer. Sanyo's organic semiconductor works well.

**Digital Interface**

**External Clock**

The MAX120/MAX122 require a TTL-compatible clock for proper operation. The MAX120 accepts clocks in the 0.1MHz to 8MHz frequency range when operating in modes 1-4 (see Operating Modes section). The maximum clock frequency is limited to 6MHz when operating in mode 5. The MAX122 requires a 0.1MHz to 5MHz clock for operation in all five modes. The minimum clock frequency for both the MAX120 and MAX122 is limited to 0.1MHz, due to the T/Hs droop rate.

**Clock and Control Synchronization**

If the clock and convert start inputs (CONVST or RD) and CS (see Operating Modes section) are not synchronized, the conversion time can vary from 13 to 14 clock cycles. The successive approximation register (SAR) always changes state on the CLkin input's rising edge. To ensure a fixed conversion time, refer to Figure 5 and the following guidelines.

For a conversion time of 13 clock cycles, the convert start input(s) should go low at least 50ns before CLKin's next rising edge. For a conversion time of 14 clock cycles, the convert start input(s) should go low within 10ns of CLKin's next rising edge. If the convert start input(s) go low from 10ns to 50ns before CLKin's next rising edge, the number of clock cycles required is undefined and can be either 13 or 14. For best analog performance, synchronize the convert start inputs with the clock input.
500ksps, 12-Bit ADCs with Track/Hold and Reference

Full-control mode is for μPs with or without wait-state capability. Stand-alone mode (mode 2) and continuous-conversion mode (mode 5) are for systems without μPs, or for μP-based systems where the ADC and the μP are linked through first-in, first-out (FIFO) buffers or direct memory access (DMA) ports. Slow-memory mode (mode 3) is intended for μPs that can be forced into a wait state during the ADC's conversion time. ROM mode (mode 4) is for μPs that cannot be forced into a wait state.

In all five operating modes, the start of a conversion is controlled by one of three digital inputs: CONVST, RD, or CS. Figure 12 shows the logic equivalent for the conversion circuitry. In any operating mode, CONVST must be low for a conversion to occur. Once the conversion is in progress, it cannot be restarted.

Read operations are controlled by RD and CS. Both of these digital inputs must be low to read output data. The INT/BUSY output indicates the converter's status and determines when the data from the most recent conversion is available. The MODE input configures the INT/BUSY output as follows.

If MODE = Vpp, INT/BUSY functions as an INTERRUPT output. In this configuration, INT/BUSY goes low when the conversion is complete and returns high after the conversion data has been read.

If MODE is left open or tied to DGND, INT/BUSY functions as a BUSY output. In this case, INT/BUSY goes low at the start of a conversion and remains low until the conversion is complete and the data is available at D0-D11.
500ksps, 12-Bit ADCs with Track/Hold and Reference

**Initialization After Power-Up**
On power-up, the first MAX120/MAX122 conversion is valid if the following conditions are met:
1) Allow 14 clock cycles for the internal T/H to enter the track mode, plus a minimum of 350ns in the track mode for the data-acquisition time.
2) Make sure the reference voltage has settled. Allow 0.5ms for each 1μF of reference bypass capacitance (11ms for a 22μF capacitor).

**Operating Modes**

**Mode 1: (Full-Control Mode)**
Figure 7 shows the timing diagram for full-control mode (mode 1). In this mode, the μP controls the conversion-start and data-read operations independently.
A falling edge on CONVST places the T/H into hold mode and starts a conversion in the SAR. The conversion is complete in 13 or 14 clock cycles as discussed in the Clock and Control Synchronization section. A change in the INT/BUSY output state signals the end of a conversion as follows:
- If MODE = VDD, the end of conversion is signaled by the INT/BUSY output falling edge.
- If MODE = OPEN or DGND, the INT/BUSY output goes low while the conversion is in progress and returns high when the conversion is complete.

When the conversion is complete, the data can be read without initiating a new conversion by pulling RD and CS low and leaving CONVST high. To start a new conversion without reading data, RD and CS should remain high while CONVST is driven low. To simultaneously read data and initiate a new conversion, CONVST, RD, and CS should all be pulled low. Note: Allow at least 350ns for T/H acquisition time between the end of one conversion and the beginning of the next.

**Mode 2: Stand-Alone Operation (MODE = OPEN, RD = CS = DGND)**
For systems that do not use or require full-bus interfacing, the MAX120/MAX122 can be operated in stand-alone mode directly linked to memory through DMA ports or a FIFO buffer. In stand-alone mode, a conversion is initiated by a falling edge on CONVST. The data outputs are always enabled; data changes at the end of a conversion as indicated by a rising edge on INT/BUSY. See Figure 8 for stand-alone mode timing.

**Mode 3: Slow-Memory Mode (CONVST = GND, MODE = OPEN)**
Taking RD and CS low places the T/H into hold mode and starts a conversion. INT/BUSY remains low while the conversion is in progress and can be used as a wait input to the μP. Data from the previous conversion appears on the data bus until the conversion end is indicated by INT/BUSY. See Figure 9 for slow-memory mode timing.
500ksps, 12-Bit ADCs with Track/Hold and Reference

**Applications Information**

**Using FIFO Buffers**

Using FIFO memory to buffer blocks of data from the MAX120 reduces µP interrupt overhead time by enabling the µP to process data while the MAX120, unassisted, writes conversion results to the FIFO. To retrieve a block of data, the µP reads from the FIFO via a read-interrupt cycle. Read and write operations for the FIFO are completely asynchronous. Figure 13 shows the MAX120 operating in continuous-conversion mode (mode 5), writing data directly into the two IDT7200256 × 9 FIFO buffers at the rate of 428ksps. The µP is interrupted to read the accumulated data by the FIFO shelf-full (HF) flag approximately three times per millisecond. For operation at 500ksps, use an 8MHz clock, and pulse CONVST at 500kHz. The full flag (FF) indicates that the FIFO is full. If the flag is ignored, data may be lost. If necessary, conversions can be inhibited by pulling CS, RD, or CONVST high. The FIFO's read cycle time is at least 15ns, satisfying most system speed requirements. The RESET input resets all data in the FIFO to zero.

**Mode 4: ROM Mode (MODE = OPEN, CONVST = GND)**

In ROM mode, the MAX120/MAX122 behave like a fast-access memory location and avoid placing the µP into a wait state. Pulling RD and CS low places the T/H in hold mode, starts a conversion, and reads data from the previous conversion. Data from the first read in a sequence is often disregarded when this interface mode is used. A second read access is the first conversion's result and also starts a new conversion. The time between successive read operations must be longer than the sum of the T/H acquisition time and the MAX120/MAX122 conversion time. See Figure 10 for ROM-mode timing.

**Mode 5: Continuous-Conversion Mode (CONVST = RD = CS = MODE = GND)**

For systems that do not use or require full-bus interfacing, the MAX120/MAX122 can operate in continuous-conversion mode, directly linked to memory through DMA ports or a FIFO buffer. In this mode, conversions are performed continuously at the rate of one conversion for every 14 clock cycles, which includes 2 clock cycles for the T/H acquisition time. To satisfy the 350ns minimum acquisition time requirement within 2 clock cycles, the MAX120's maximum clock frequency is 6MHz when operating in mode 5.

The data outputs are always enabled and 'new' data appears on the output bus at the end of a conversion as indicated by the INT/BUSY output rising edge. The MODE input should be hard-wired to GND. Pulling CS, RD, or CONVST high stops conversions. See Figure 11 for continuous-conversion mode timing.
500ksps, 12-Bit ADCs with Track/Hold and Reference

Figura 13. Using MAX120 with FIFO Memory

For synchronous operation, the CONVST pin may be used to initiate conversions, as described in the Operating Modes section (Mode 2: Stand-Alone Operation).

Digital-Bus Noise

If the ADC's data bus is active during a conversion, coupling from the data pins to the ADC comparator can cause errors. Using slow-memory mode (mode 3) avoids this problem by placing the pins in a wait state during the conversion. If the data bus is active during the conversion in either mode 1 or 4, use three-state drivers to isolate the bus from the ADC.

In ROM mode (mode 4), considerable digital noise is generated in the ADC when RD or CS go high, disabling the output buffers after a conversion is started. This noise can cause errors if it occurs at the same instant the SAR latches a comparator decision. To avoid this problem, RD and CS should be active for less than 1 clock cycle if this is not possible; RD or CS should go high coinciding with CLKIN's falling edge, since the comparator output is always latched at CLKIN's rising edge.

Layout, Grounding, and Bypassing

For best system performance, use printed circuit boards with separate analog and digital ground planes. Wire-wrap boards are not recommended. The two ground planes should be tied together at the low-impedance power-supply source, as shown in Figure 14. The board layout should ensure that digital and analog signal lines are kept separate from each other as much as possible. Do not run analog and digital (especially clock) lines parallel to one another.

The ADC's high-speed comparator is sensitive to high-frequency noise in the VDD and VSS power supplies. Bypass these supplies to the analog ground plane with 0.1μF and 10μF bypass capacitors. Minimize capacitor lead lengths for best noise rejection. If the +5V power supply is very noisy, connect a 51Ω resistor, as shown in Figure 14. Figure 15 shows the negative power-supply (VSS) rejection vs. frequency. Figure 16 shows the positive power-supply (VDD) rejection vs. frequency, with and without the optional 5Ω resistor.

MAXIM
500ksps, 12-Bit ADCs with Track/Hold and Reference

**Gain and Offset Adjustment**

Figure 17 plots the bipolar input/output transfer function for the MAX120/MAX122. Code transitions occur halfway between successive integer LSB values. Output coding is twos-complement binary with 1LSB = 2.44mV (10V/4096).

In applications where gain (full-scale range) adjustment is required, Figure 18's circuit can be used. If both offset and gain (full-scale range) need adjustment, either of the circuits in Figures 19 and 20 can be used. Offset should be adjusted before gain for either of these circuits.

To adjust bipolar offset with Figure 19's circuit, apply +1/2LSB (0.61mV) to the noninverting amplifier input and adjust R4 for output-code flicker between 0000 0000 0000 and 0000 0000 0001. For full scale, apply FS - 1/2 LSB (2.4988V) to the amplifier input and adjust R2 so the output code flickers between 0111 1111 1110 and 0111 1111 1111. There may be some interaction between these adjustments. The MAX120/MAX122 transfer function used in conjunction with Figure 19's circuit is the same as Figure 17, except the full-scale range is reduced to 2.5V.

To adjust bipolar offset with Figure 20's circuit, apply -1/2LSB (-1.22mV) at VIN and adjust R5 for output-code flicker between 0000 0000 0000 and 0000 0000 0001. For gain adjustment, apply FS + 1/2 LSB (-4.9951V) at VIN and adjust R1 so the output code flickers between 0111 1111 1110 and 0111 1111 1111. As with Figure 20's circuit, the offset and gain adjustments may interact. Figure 21 plots the transfer function for Figure 20's circuit.

**Dynamic Performance**

High-speed sampling capability and 500ksps throughput (333ksps for the MAX122) make the MAX120/MAX122 ideal for wideband-signal processing. To support these and other related applications, fast fourier transform (FFT) test techniques are used to guarantee the ADC's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low-distortion sine wave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm, which determines its spectral content.
ADCs have traditionally been evaluated by specifications such as zero and full-scale error, integral nonlinearity (INL), and differential nonlinearity (DNL). Such parameters are widely accepted for specifying performance with DC and slowly varying signals, but are less useful in signal processing applications where the ADC's impact on the system transfer function is the main concern. The significance of various DC errors does not translate well to the dynamic case, so different tests are required.

**Signal-to-Noise Ratio and Effective Number of Bits**

The theoretical minimum ADC noise is caused by quantization error and is a direct result of the ADC's resolution.

\[
\text{SNR} = (6.02N + 1.76) \text{dB}
\]

where \(N\) is the number of bits of resolution. A perfect 12-bit ADC can, therefore, do no better than 74dB. An FFT plot shows the output level in various spectral bands. Figure 22 shows the result of sampling a pure 100kHz sinusoid at a 500ksps rate with the MAX120. By transposing the equation that converts resolution to SNR, we can, from the measured SINAD, determine the effective resolution (or effective number of bits) the ADC provides.

\[
N = \frac{(\text{SINAD} - 1.76)}{6.02}
\]

Figure 22 shows the effective number of bits as a function of the input frequency for the MAX120. The MAX122 performs similarly.
500ksps, 12-Bit ADCs with Track/Hold and Reference

where \( V_1 \) is the fundamental RMS amplitude, and \( V_2 \) to \( V_N \) are the amplitudes of the 2nd through Nth harmonics. The THD specification in the Electrical Characteristics table includes the 2nd through 5th harmonics.

**Intermodulation Distortion**

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearities produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequency \( f_a \) and \( f_b \) are applied to the ADC input, nonlinearities in the ADC transfer function create distortion products at sum and difference frequencies of \( m f_a \pm n f_b \), where \( m \) and \( n \) can be 0, 1, 2, 3, etc. THD includes those distortion products with \( m \) or \( n \) equal to zero. Intermodulation distortion consists of all distortion products for which neither \( m \) nor \( n \) equal zero. For example, the 2nd-order IMD terms include \((fa + fb)\) and \((fa - fb)\) while the 3rd-order IMD terms include \((2fa + fb), (2fa - fb), (fa + 2fb), \) and \((fa - 2fb)\).

If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd-order IMD products can be expressed by the following formula:

\[
\text{IMD} (fa \pm fb) = 20 \log \left( \frac{\text{amplitude at } (fa \pm fb)}{\text{amplitude at } fa} \right)
\]
500ksps, 12-Bit ADCs with Track/Hold and Reference

Spurious-Free Dynamic Range
Spurious-free dynamic range is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually the next largest spectral component occurs at some harmonic of the input frequency. However, if the ADC is exceptionally linear it may occur only at a random peak in the ADC's noise floor.

Ordering Information (continued)

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* Contact factory for dice specifications
† MAX120 EV kit can be used to evaluate the MAX122, when ordering the EV kit, ask for a free sample of the MAX122.
500ksps, 12-Bit ADCs with Track/Hold and Reference

Package Information

**MAX120/MAX122**

24-PIN PLASTIC DUAL-IN-LINE (NARROW) PACKAGE

**MAX120**

24-PIN PLASTIC SMALL-OUTLINE PACKAGE
500ksps, 12-Bit ADCs with Track/Hold and Reference

Package Information (continued)

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24-PIN PLASTIC SHRINK SMALL-OUTLINE PACKAGE

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.
# BIODATA

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<tr>
<th>Nama</th>
<th>Jimmy Yang</th>
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<td>Agama</td>
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<tr>
<td>Alamat</td>
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</table>

**Riwayat Pendidikan:**

- Tahun 1989 Lulus SD. YPPI I Surabaya.
- Tahun 1992 Lulus SMP YPPI II Surabaya.
- Tahun 1995 Lulus SMA YPPI I Surabaya.

**Selama kuliah, aktif sebagai:**

- Anggota Senat Mahasiswa Fakultas Teknik.
- Asisten Praktikum Dasar Elektronika di Laboratorium Elektronika.
- Asisten Praktikum Elektronika Analog di Laboratorium Elektronika.
- Asisten Praktikum Sistem Intrumentasi Elektronika di Laboratorium Pengukuran.